TEXAS INSTRUMENTS

25-07453

OPA172, OPA2172, OPA4172

SBOS618H – DECEMBER 2013 – REVISED SEPTEMBER 2015

OPAx172 36-V, Single-Supply, 10-MHz, Rail-to-Rail Output Operational Amplifiers

1 Features

- Wide Supply Range:
  +4.5 V to +36 V, ±2.25 V to ±18 V
- Low Offset Voltage: ±0.2 mV
- Low Offset Drift: ±0.3 µV/°C
- Gain Bandwidth: 10 MHz
- Low Input Bias Current: ±8 pA
- Low Quiescent Current: 1.6 mA per Amplifier
- Low Noise: 7 nV/√Hz
- EMI and RFI Filtered Inputs
- Input Range Includes the Negative Supply
- Input Range Operates to Positive Supply
- Rail-to-Rail Output
- High Common-Mode Rejection: 120 dB
- Industry-Standard Packages:
  - SOIC-8, VSSOP-8, SOIC-14, TSSOP-14
- *micro*Packages: Single in SC70, SOT-23, Dual in WSON-8

2 Applications

- Tracking Amplifier in Power Modules
- Merchant Power Supplies
- Transducer Amplifiers
- Bridge Amplifiers
- Temperature Measurements
- Strain Gauge Amplifiers
- Precision Integrators
- Test Equipment

3 Description

The OPA172, OPA2172 and OPA4172 (OPAx172) are a family of 36-V, single-supply, low-noise operational amplifiers capable of operating on supplies ranging from +4.5 V (±2.25 V) to +36 V (±18 V). This latest addition of high-voltage CMOS operational amplifiers, in conjunction with the OPAx171 and OPAx170, provide a family of bandwidth, noise, and power options to meet the needs of a wide variety of applications. The OPAx172 are available in micropackages, and offer low offset, drift, and quiescent current. These devices also offer wide bandwidth, fast slew rate, and high output current drive capability. The single, dual, and quad versions all have identical specifications for maximum design flexibility.

Unlike most op amps, which are specified at only one supply voltage, the OPAx172 family is specified from +4.5 V to +36 V. Input signals beyond the supply rails do not cause phase reversal. The input can operate 100 mV below the negative rail and within 2 V of the top rail during normal operation. Note that these devices can operate with full rail-to-rail input 100 mV beyond the top rail, but with reduced performance within 2 V of the top rail.

The OPAx172 series of op amps are specified from –40°C to +125°C.

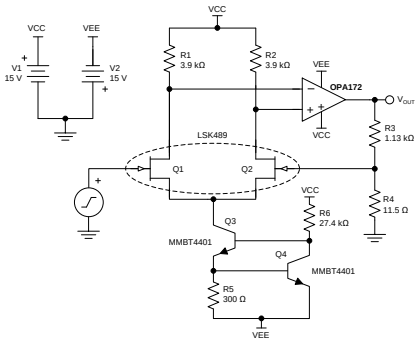
Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
OPA172	SC70 (5)	2.00 mm × 1.25 mm
	SOT-23 (5)	2.90 mm × 1.60 mm
	SOIC (8)	4.90 mm × 3.91 mm
OPA2172	SOIC (8)	4.90 mm × 3.91 mm
	VSSOP (8)(2)	3.00 mm × 3.00 mm
	WSON (8)	3.00 mm × 3.00 mm
OPA4172	SOIC (14)	8.65 mm × 3.91 mm
	TSSOP (14)	4.40 mm × 5.00 mm

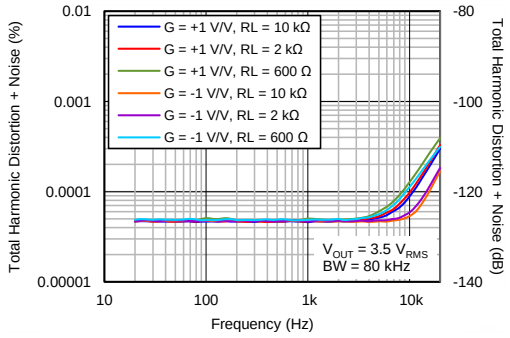
(1) For all available packages, see the package option addendum at the end of the data sheet.

(2) The VSSOP package is the same as the MSOP package.

JFET-Input Low-Noise Amplifier



Superior THD Performance



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- Added DRG package to OPA2172 device ... 1
- Added WSON to last *Features* bullet ... 1
- Added OPA2172 WSON row to *Device Information* table ... 1
- Added WSON-8 to OPA2172 row of *Device Comparison* table ... 4
- Added DRG pinout drawing ... 5
- Added DRG column to OPA2172 and OPA4172 *Pin Functions* table ... 6
- Added DRG column to OPA2172 *Thermal Information* table ... 8

Changes from Revision F (June 2015) to Revision G — **Page**

- Added input bias current (I_B) values for DGK and PW packages. ... 8

Changes from Revision E (December 2014) to Revision F — **Page**

- Changed device status to Production Data from Mixed Status ... 1
- Changed OPA2172 DGK and OPA4172 PW packages to Production Data ... 1
- Added OPA2172 VSSOP and OPA4172 TSSOP rows to *Device Information* table ... 1
- Deleted footnote from *Device Comparison* table ... 4
- Deleted footnote from OPA2172 DGK and OPA4172 PW pin out drawings ... 5
- Added OPA2172 DGK thermal information ... 8

Changes from Revision D (September 2014) to Revision E **Page**

- Changed OPA2172 D package from product preview to production data ... 1
- Changed *Device Information* table ... 1
- Changed *Device Comparison* table note (1) to show preview packages ... 4
- Added note 2 to pin configurations to show preview packages and deleted previous note ... 5
- Changed *Handling Ratings* table to *ESD Ratings* table ... 7

Changes from Revision C (July 2014) to Revision D **Page**

- Changed low-noise features bullet value from 6 nV/√Hz to 7 ... 1
- Changed MSOP to VSSOP in features bullet ... 1
- Added packages and new note 2 to *Device Information* table ... 1
- Changed OPAx172 voltage noise density from 6 nV/√Hz to 7 in *Device Family Comparison* table ... 4
- Changed OPA4172 package from DGK to PW in *Pin Functions* table ... 6
- Added OPA2172 *Thermal Information* table ... 8
- Changed input voltage noise value in *Electrical Characteristics* from 1.2 μV_{PP} to 2.5 μV_{PP} ... 8
- Changed input voltage noise density value at 100 Hz in *Electrical Characteristics* from 8.6 nV/√Hz to 12 ... 8
- Changed input voltage noise density value at 1 kHz in *Electrical Characteristics* from 6 nV/√Hz to 7 ... 8
- Changed voltage output swing values in the *Electrical Characteristics* ... 9
- Changed Figure 13 ... 12
- Changed Figure 14 ... 12
- Added new note to *Applications and Implementation* section ... 24

Changes from Revision B (May 2014) to Revision C **Page**

- Changed OPA4172 D package (SOIC-14) from product preview to production data ... 1
- Added OPA4172-D Thermal information ... 8
- Added Channel separation parameter to the *Electrical Characteristics* ... 8
- Added Channel Separation vs Frequency plot ... 16

Changes from Revision A (April 2014) to Revision B **Page**

- Changed DCK (SC70) package from product preview to production data ... 1

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- Changed document format to meet latest data sheet standards; added *Handling Ratings Recommended Operating Conditions*, and *Device and Documentation Support* sections, and moved existing sections ... 1
- Changed DCK package pin names from IN+ and IN– to +IN and –IN, respectively ... 5
- Changed DBV package from product preview to production data ... 5
- Changed Figure 9 ... 11
- Added *Functional Block Diagram* section ... 18
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5 Device Comparison

Device Comparison

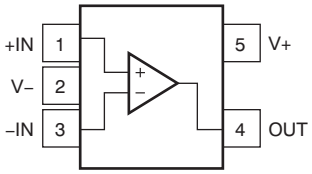
DEVICE	PACKAGE
OPA172 (single)	SC70-5, SOT-23-5, SOIC-8
OPA2172 (dual)	SOIC-8, VSSOP-8, WSON-8
OPA4172 (quad)	SOIC-14, TSSOP-14

Device Family Comparison

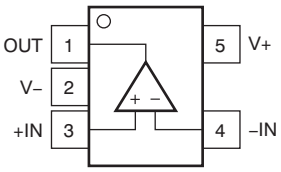
DEVICE	QUIESCENT CURRENT (I_Q)	GAIN BANDWIDTH PRODUCT (GBP)	VOLTAGE NOISE DENSITY (e_n)
OPAx172	1600 µA	10 MHz	7 nV/$\sqrt{Hz}$
OPAx171	475 µA	3.0 MHz	14 nV/$\sqrt{Hz}$
OPAx170	110 µA	1.2 MHz	19 nV/$\sqrt{Hz}$

6 Pin Configuration and Functions

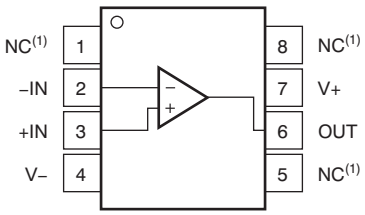
DCK Package: OPA172
SC70-5
Top View



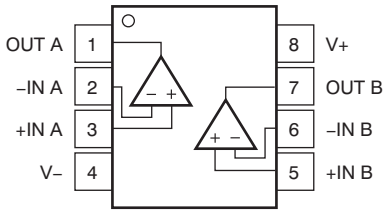
DBV Package: OPA172
SOT-23-5
Top View



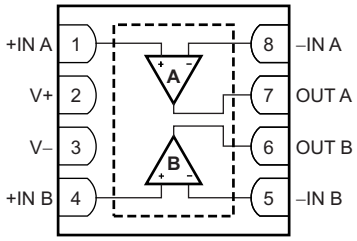
D Package: OPA172
SOIC-8
Top View



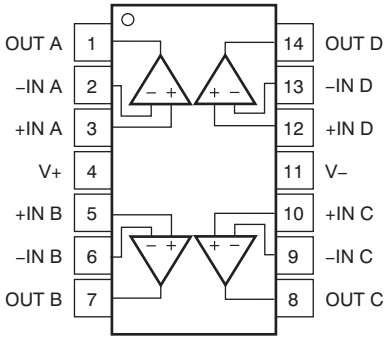
D and DGK Packages: OPA2172
SOIC-8 and VSSOP-8
Top View



DRG Package: OPA2172
WSON-8
Top View



D and PW Packages: OPA4172
SO-14 and TSSOP-14
Top View



(1) No internal connection.

Pin Functions: OPA172

PIN				I/O	DESCRIPTION
	OPA172				
NAME	D (SOIC)	DBV (SOT)	DCK (SC70)		
+IN	3	3	1	I	Noninverting input
–IN	2	4	3	I	Inverting input
NC	1, 5, 8	—	—	—	No internal connection
OUT	6	1	4	O	Output
V+	7	5	5	—	Positive (highest) power supply
V–	4	2	2	—	Negative (lowest) power supply

Pin Functions: OPA2172 and OPA4172

PIN				I/O	DESCRIPTION
	OPA2172		OPA4172		
NAME	D (SOIC), DGK (VSSOP)	DRG (WSON)	D (SOIC), PW (TSSOP)		
+IN A	3	1	3	I	Noninverting input, channel A
+IN B	5	4	5	I	Noninverting input, channel B
+IN C	—	—	10	I	Noninverting input, channel C
+IN D	—	—	12	I	Noninverting input, channel D
–IN A	2	8	2	I	Inverting input, channel A
–IN B	6	5	6	I	Inverting input, channel B
–IN C	—	—	9	I	Inverting input,,channel C
–IN D	—	—	13	I	Inverting input, channel D
OUT A	1	7	1	O	Output, channel A
OUT B	7	6	7	O	Output, channel B
OUT C	—	—	8	O	Output, channel C
OUT D	—	—	14	O	Output, channel D
V+	8	2	4	—	Positive (highest) power supply
V–	4	3	11	—	Negative (lowest) power supply

7 Specifications

7.1 Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
Supply voltage, V_S				±20 (+40, single supply)	V
Signal input pins	Voltage(2)	Common-mode	(V–) – 0.5	(V+) + 0.5	V
		Differential(3)		±0.5	
	Current			±10	mA
Output short circuit(4)				Continuous	
Temperature	Operating		–55	+150	°C
	Junction			+150	
	Storage, T_{stg}		–65	+150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Transient conditions that exceed these voltage ratings must be current limited to 10 mA or less.
(3) Refer to the *Electrical Overstress* section for more information.
(4) Short-circuit to ground, one amplifier per package.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±4000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Supply voltage (V+ – V–)	4.5 (±2.25)		36 (±18)	V
Specified temperature	–40		125	°C

7.4 Thermal Information: OPA172

THERMAL METRIC(1)		OPA172			UNIT
		D (SOIC)	DBV (SOT-23)	DCK (SC70)	
		8 PINS	5 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	126.5	227.9	285.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	80.6	115.7	60.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	67.1	65.9	78.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	31.0	10.7	0.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	66.6	65.3	77.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.5 Thermal Information: OPA2172

THERMAL METRIC(1)		OPA2172			UNIT
		D (SOIC)	DGK (VSSOP)	DRG (WSON)	
		8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	116.1	158	63.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	69.8	48.6	63.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	56.6	78.7	36.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	22.5	3.9	1.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	56.1	77.3	36.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	6.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.6 Thermal Information: OPA4172

THERMAL METRIC(1)		OPA4172		UNIT
		D (SOIC)	PW (TSSOP)	
		14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	82.7	111.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	42.3	40.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	37.3	54.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	8.9	3.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	37	53.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.7 Electrical Characteristics

At T_A = +25°C, V_S = ±2.25 V to ±18 V, V_{CM} = V_{OUT} = V_S / 2, and R_L = 10 kΩ connected to V_S / 2, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage				±0.2	±1	mV
		T_A = –40°C to +125°C				±1.15	
dV_{OS}/dT	Drift	T_A = –40°C to +125°C	OPA172, OPA4172		±0.3	±1.5	µV/°C
			OPA2172			±1.8	
PSRR	vs power supply	T_A = –40°C to +125°C			±1	±3	µV/V
	Channel separation, dc	At dc			5		µV/V
INPUT BIAS CURRENT							
I_B	Input bias current				±8	±15	pA
		T_A = –40°C to +125°C				±14	nA
		T_A = –40°C to +125°C	OPA2172IDGK			±18	
			OPA41721PW				
I_{OS}	Input offset current				±2	±15	pA
		T_A = –40°C to +125°C	OPA172, OPA4172			±1	nA
			OPA2172			±3	
NOISE							
E_n	Input voltage noise	f = 0.1 Hz to 10 Hz			2.5		μV_{PP}
e_n	Input voltage noise density	f = 100 Hz			12		$nV/\sqrt{Hz}$
		f = 1 kHz			7		
i_n	Input current noise density	f = 1 kHz			1.6		$fA/\sqrt{Hz}$

Electrical Characteristics (continued)

At T_A = +25°C, V_S = ±2.25 V to ±18 V, V_{CM} = V_{OUT} = V_S / 2, and R_L = 10 kΩ connected to V_S / 2, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
INPUT VOLTAGE							
V_{CM}	Common-mode voltage range(1)			(V–) – 0.1 V		(V+) – 2 V	V
CMRR	Common-mode rejection ratio	V_S = ±2.25 V, (V–) – 0.1 V < V_{CM} < (V+) – 2 V, T_A = –40°C to +125°C		90	104		dB
		V_S = ±18 V, (V–) – 0.1 V < V_{CM} < (V+) – 2 V, T_A = –40°C to +125°C		110	120		
INPUT IMPEDANCE							
	Differential				100 || 4		MΩ || pF
	Common-mode				6 || 4		10^{13}Ω || pF
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	(V–) + 0.35 V < V_O < (V+) – 0.35 V, R_L = 10 kΩ, T_A = –40°C to +125°C	OPA172, OPA4172	110	130		dB
			OPA2172	107	115		
		(V–) + 0.5 V < V_O < (V+) – 0.5 V, R_L = 2 kΩ, T_A = –40°C to +125°C	OPA172, OPA4172		116		
			OPA2172		107		
FREQUENCY RESPONSE							
GBP	Gain bandwidth product				10		MHz
SR	Slew rate	G = +1			10		V/µs
t_S	Settling time	To 0.1%, V_S = ±18 V, G = +1, 10-V step			2		µs
		To 0.01% (12 bit), V_S = ±18 V, G = +1, 10-V step			3.2		
	Overload recovery time	V_{IN} × Gain > V_S			200		ns
THD+N	Total harmonic distortion + noise	V_S = +36 V, G = +1, f = 1 kHz, V_O = 3.5 V_{RMS}			0.00005%		
OUTPUT							
V_O	Voltage output swing from rail	V_S = +36 V	R_L = 10 kΩ		70	90	mV
			R_L = 2 kΩ		330	400	
		V_S = +36 V, T_A = –40°C to +125°C	R_L = 10 kΩ		95	120	
			R_L = 2 kΩ		470	530	
		V_S = +4.5V	R_L = 10 kΩ		10	20	
			R_L = 2 kΩ		40	50	
		V_S = +4.5 V, T_A = –40°C to +125°C	R_L = 10 kΩ		10	25	
			R_L = 2 kΩ		55	70	
I_{SC}	Short-circuit current				±75		mA
C_{LOAD}	Capacitive load drive			See *Typical Characteristics*			pF
Z_O	Open-loop output impedance	f = 1 MHz, I_O = 0 A			60		Ω
POWER SUPPLY							
V_S	Specified voltage range			+4.5		+36	V
I_Q	Quiescent current per amplifier	I_O = 0 A			1.6	1.8	mA
		I_O = 0 A, T_A = –40°C to +125°C				2	
TEMPERATURE							
	Specified range			–40		+125	°C

(1) The input range can be extended beyond (V+) – 2 V up to (V+) + 0.1 V. See the *Typical Characteristics* and *Application Information* sections for additional information.

7.8 Typical Characteristics: Table of Graphs

Table 1. List of Typical Characteristics

DESCRIPTION	FIGURE
Offset Voltage Production Distribution	Figure 1
Offset Voltage Drift Distribution	Figure 2
Offset Voltage vs Temperature (V_S = ±18 V)	Figure 3
Offset Voltage vs Common-Mode Voltage (V_S = ±18 V)	Figure 4
Offset Voltage vs Common-Mode Voltage (Upper Stage)	Figure 5
Offset Voltage vs Power Supply	Figure 6
I_B vs Common-Mode Voltage	Figure 7
Input Bias Current vs Temperature	Figure 8
Output Voltage Swing vs Output Current (Maximum Supply)	Figure 9
CMRR and PSRR vs Frequency (Referred-to Input)	Figure 10
CMRR vs Temperature	Figure 11
PSRR vs Temperature	Figure 12
0.1-Hz to 10-Hz Noise	Figure 13
Input Voltage Noise Spectral Density vs Frequency	Figure 14
THD+N Ratio vs Frequency	Figure 15
THD+N vs Output Amplitude	Figure 16
Quiescent Current vs Temperature	Figure 17
Quiescent Current vs Supply Voltage	Figure 18
Open-Loop Gain and Phase vs Frequency	Figure 19
Closed-Loop Gain vs Frequency	Figure 20
Open-Loop Gain vs Temperature	Figure 21
Open-Loop Output Impedance vs Frequency	Figure 22
Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)	Figure 23, Figure 24
Positive Overload Recovery	Figure 25, Figure 26
Negative Overload Recovery	Figure 27, Figure 28
Small-Signal Step Response (10 mV)	Figure 29, Figure 30
Small-Signal Step Response (100 mV)	Figure 31, Figure 32
Large-Signal Step Response (1 V)	Figure 33, Figure 34
Large-Signal Settling Time (10-V Positive Step)	Figure 35
Large-Signal Settling Time (10-V Negative Step)	Figure 36
No Phase Reversal	Figure 37
Short-Circuit Current vs Temperature	Figure 38
Maximum Output Voltage vs Frequency	Figure 39
EMIRR vs Frequency	Figure 40
Channel Separation vs Frequency	Figure 41

7.9 Typical Characteristics

At V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF, unless otherwise noted.

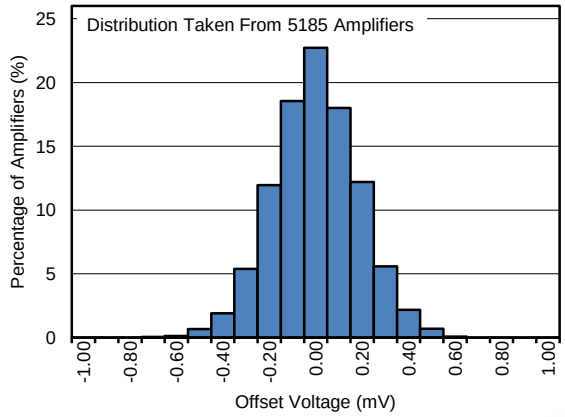


Figure 1. Offset Voltage Production Distribution

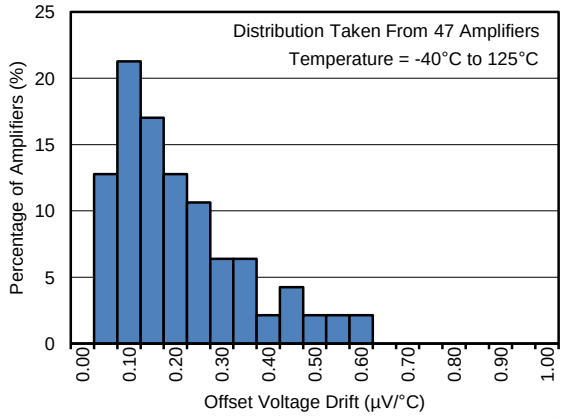


Figure 2. Offset Voltage Drift Production Distribution

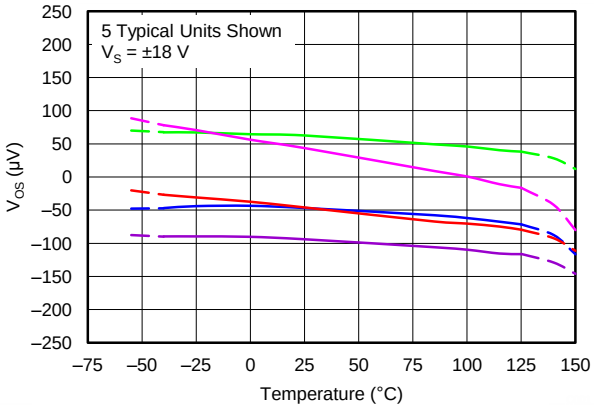


Figure 3. Offset Voltage vs Temperature (V_S = ±18 V)

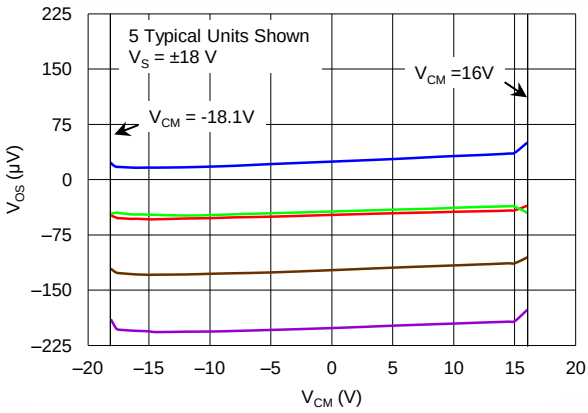


Figure 4. Offset Voltage vs Common-Mode Voltage (V_S = ±18 V)

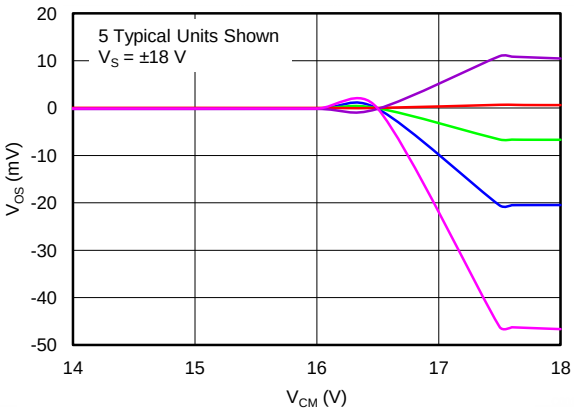


Figure 5. Offset Voltage vs Common-Mode Voltage (Upper Stage)

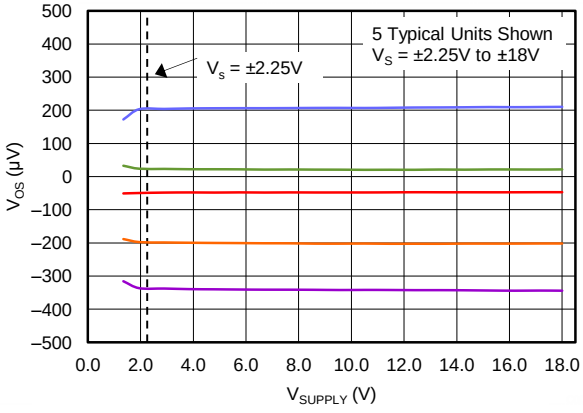


Figure 6. Offset Voltage vs Power Supply

Typical Characteristics (continued)

At V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF, unless otherwise noted.

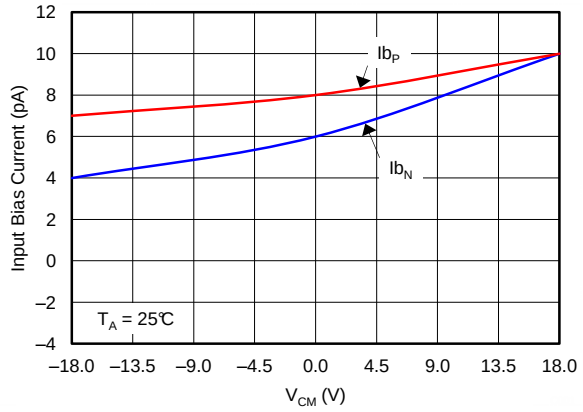


Figure 7. Input Bias Current vs Common-Mode Voltage

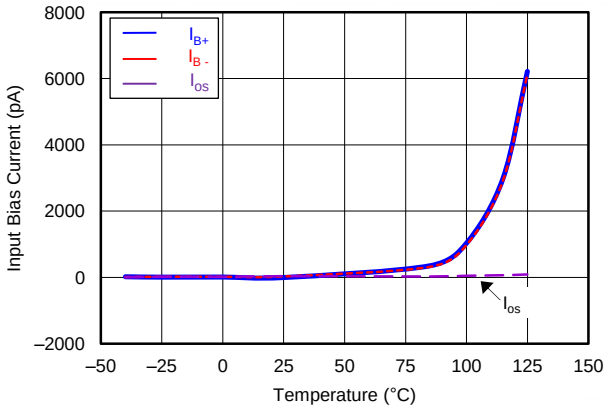


Figure 8. Input Bias Current vs Temperature

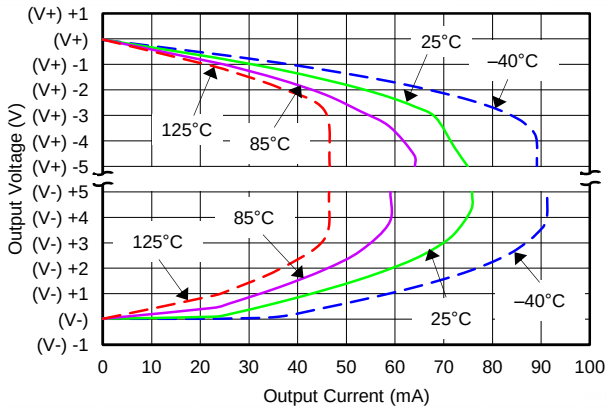


Figure 9. Output Voltage Swing vs Output Current (Maximum Supply)

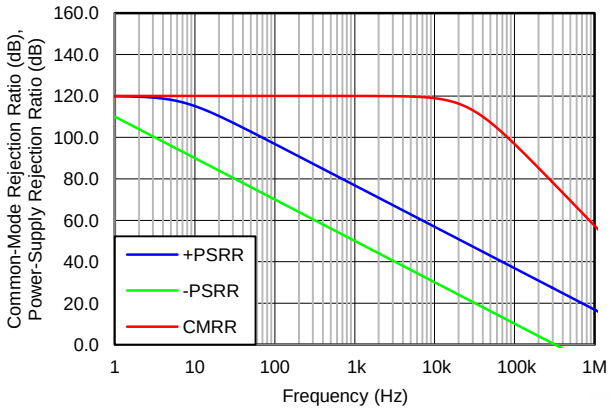


Figure 10. CMRR and PSRR vs Frequency (Referred-To-Input)

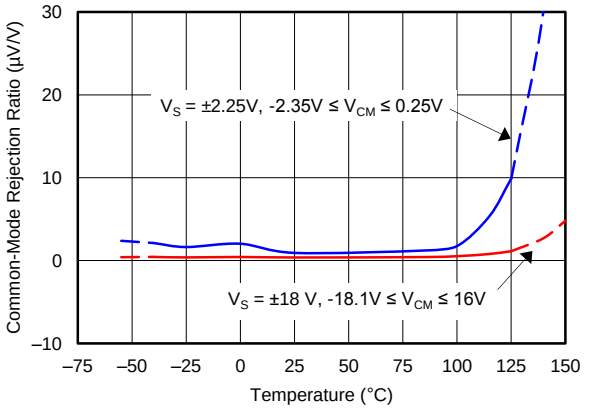


Figure 11. CMRR vs Temperature

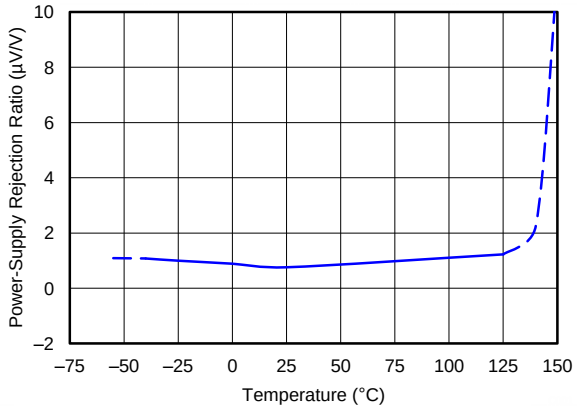


Figure 12. PSRR vs Temperature

Typical Characteristics (continued)

At V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF, unless otherwise noted.

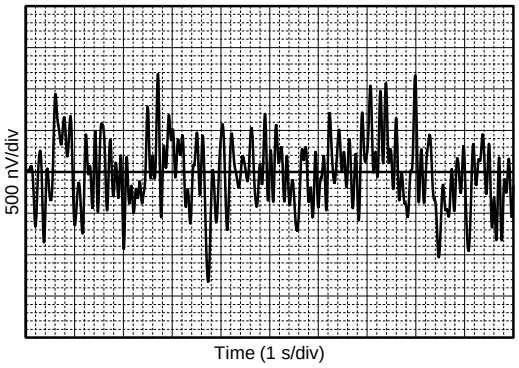


Figure 13. 0.1-Hz to 10-Hz Noise

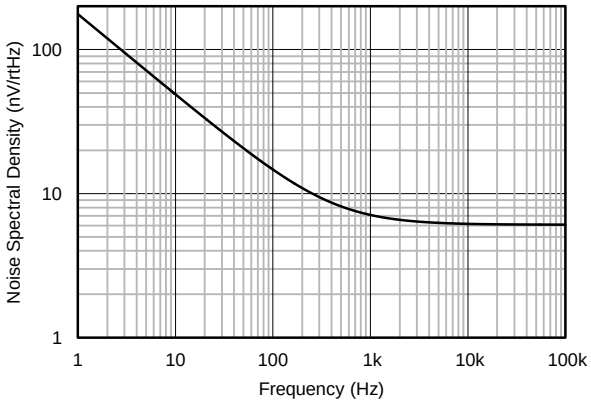


Figure 14. Input Voltage Noise Spectral Density vs Frequency

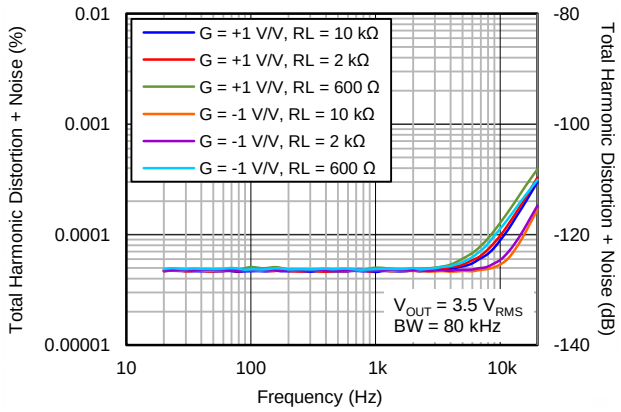


Figure 15. THD+N Ratio vs Frequency

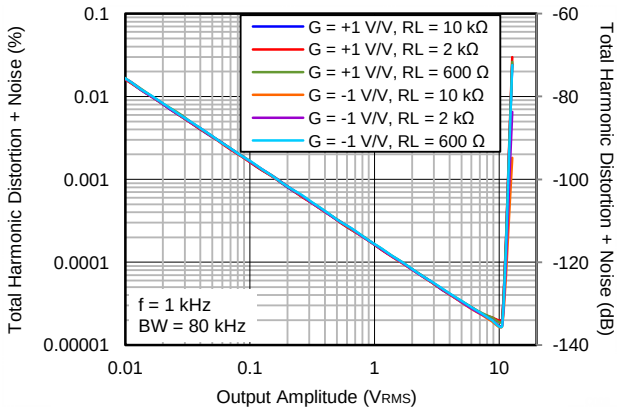


Figure 16. THD+N vs Output Amplitude

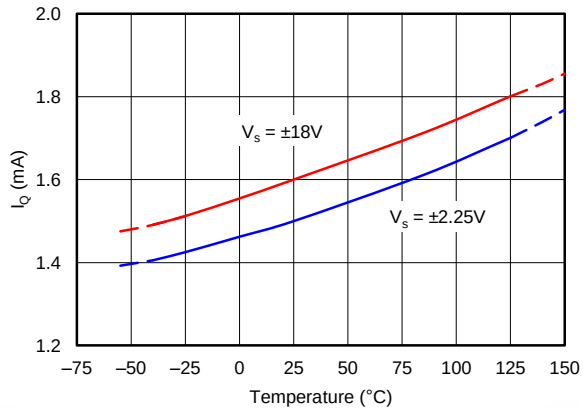


Figure 17. Quiescent Current vs Temperature

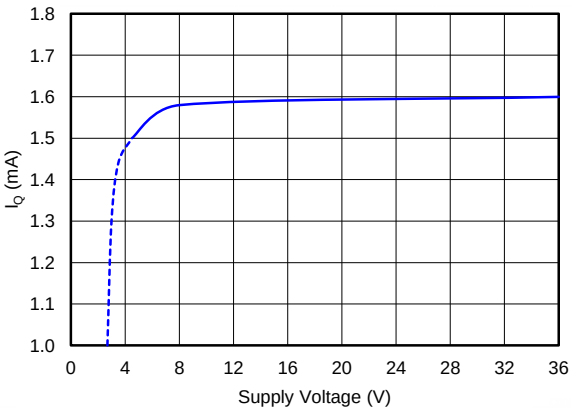


Figure 18. Quiescent Current vs Supply Voltage

Typical Characteristics (continued)

At V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF, unless otherwise noted.

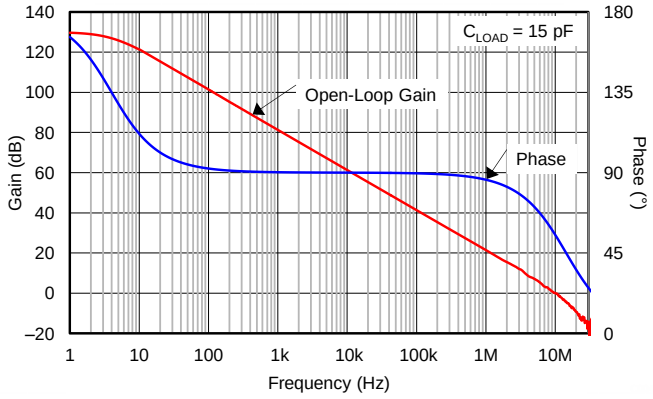


Figure 19. Open-Loop Gain and Phase vs Frequency

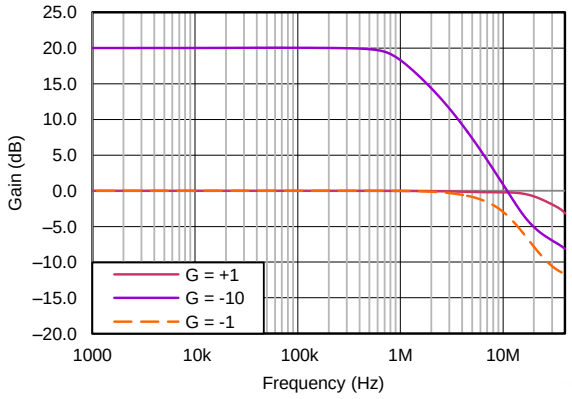


Figure 20. Closed-Loop Gain vs Frequency

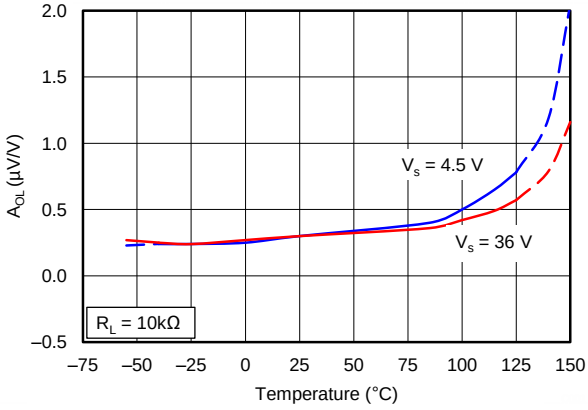


Figure 21. Open-Loop Gain vs Temperature

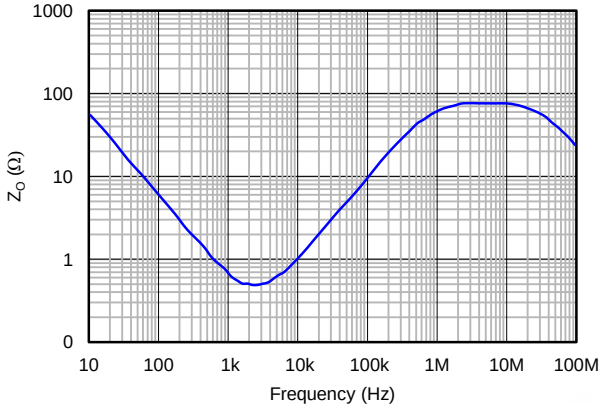


Figure 22. Open-Loop Output Impedance vs Frequency

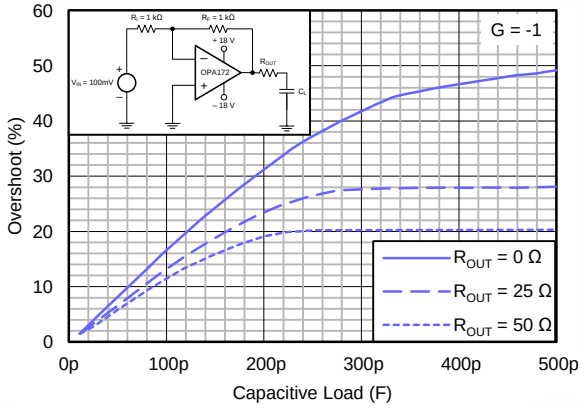


Figure 23. Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)

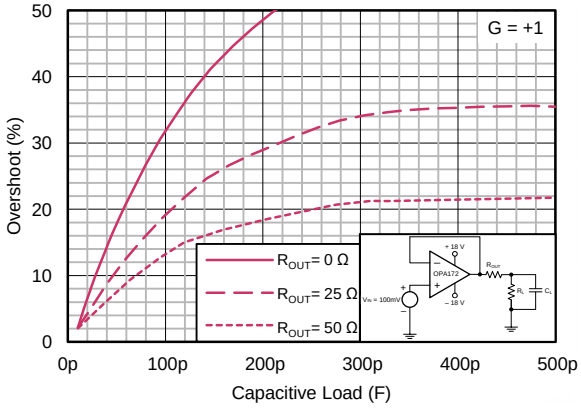


Figure 24. Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)

Typical Characteristics (continued)

At V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF, unless otherwise noted.

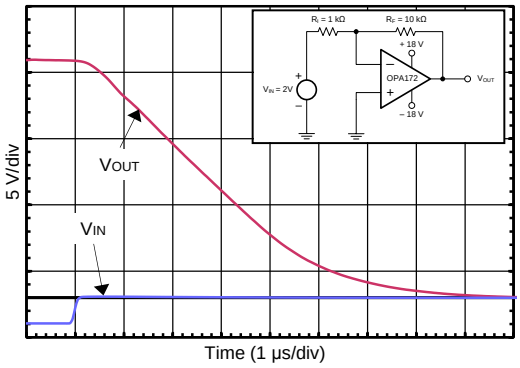


Figure 25. Positive Overload Recovery

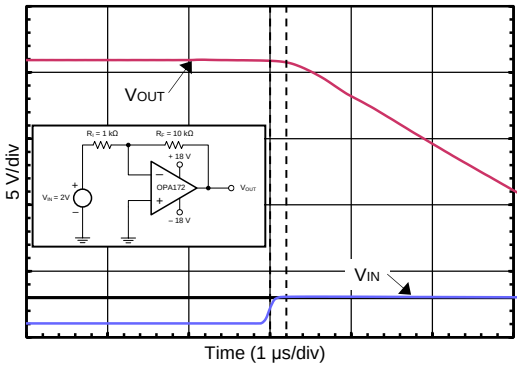


Figure 26. Positive Overload Recovery (Zoomed In)

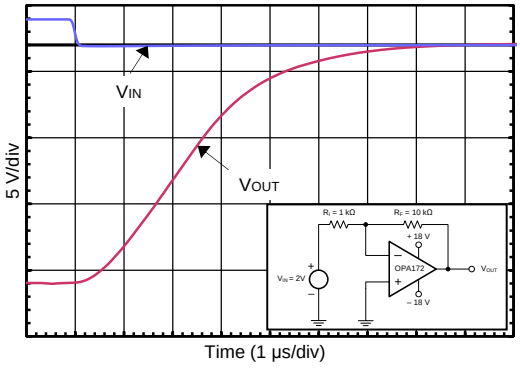


Figure 27. Negative Overload Recovery

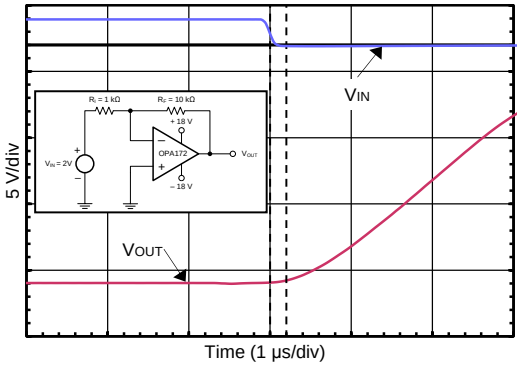


Figure 28. Negative Overload Recovery (Zoomed In)

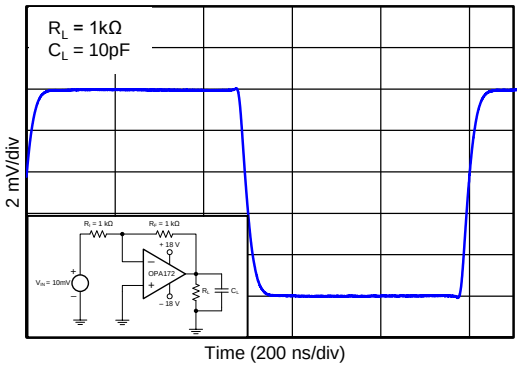


Figure 29. Small-Signal Step Response (10 mV, G = –1)

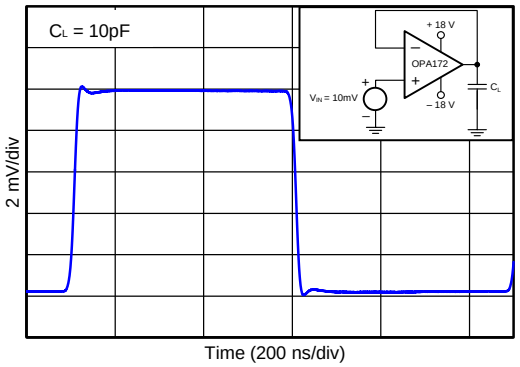


Figure 30. Small-Signal Step Response (10 mV, G = +1)

Typical Characteristics (continued)

At V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF, unless otherwise noted.

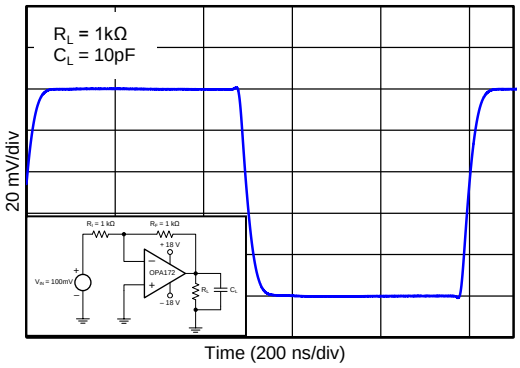


Figure 31. Small-Signal Step Response (100 mV, G = –1)

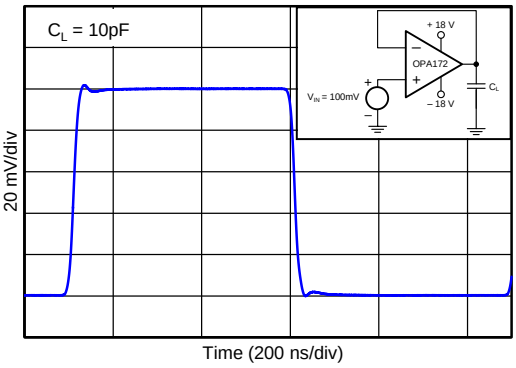


Figure 32. Small-Signal Step Response (100 mV, G = +1)

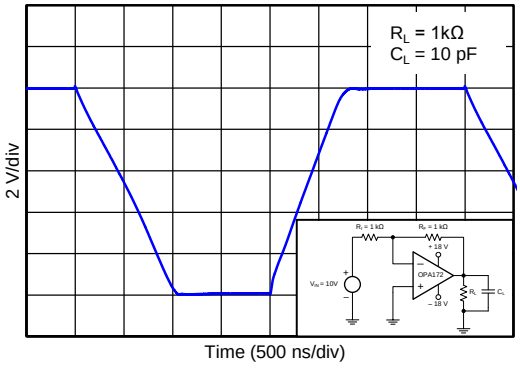


Figure 33. Large-Signal Step Response (10 V, G = –1)

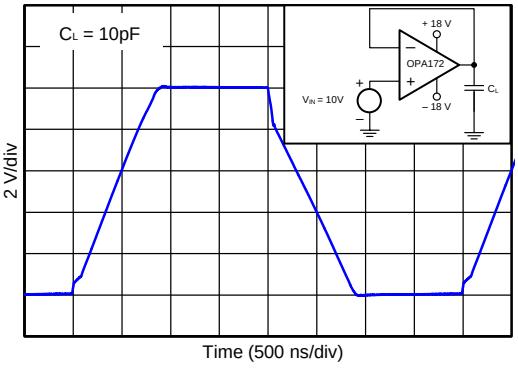


Figure 34. Large-Signal Step Response (10 V, G = +1)

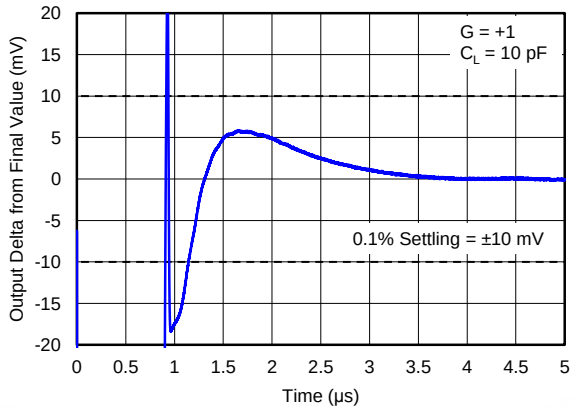


Figure 35. Large-Signal Settling Time (10-V Positive Step)

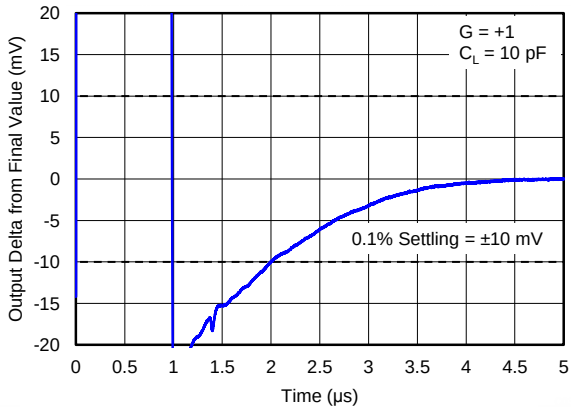


Figure 36. Large-Signal Settling Time (10-V Negative Step)

Typical Characteristics (continued)

At V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF, unless otherwise noted.

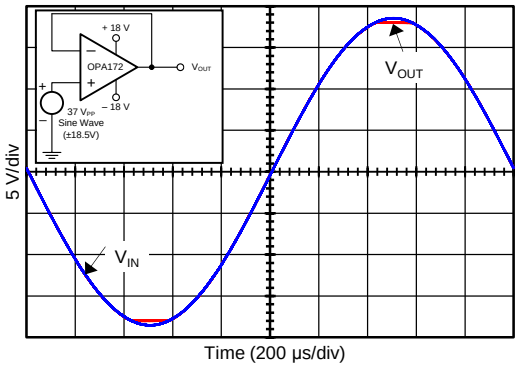


Figure 37. No Phase Reversal

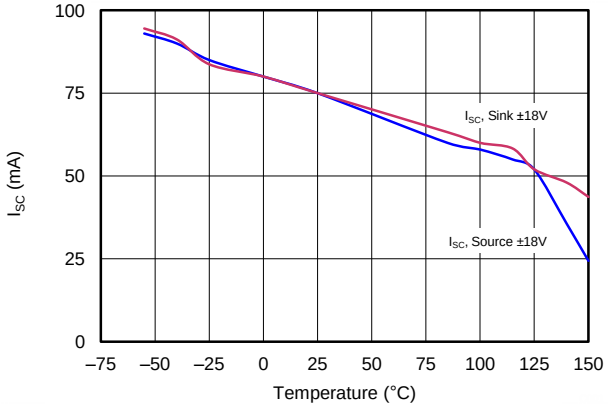


Figure 38. Short-Circuit Current vs Temperature

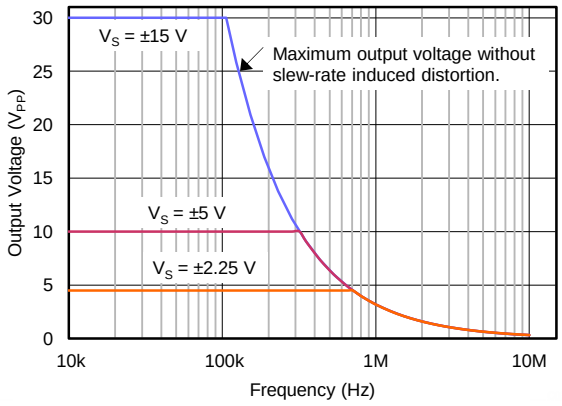


Figure 39. Maximum Output Voltage vs Frequency

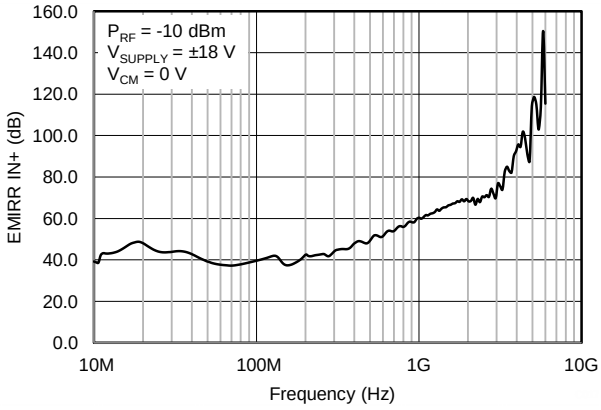


Figure 40. EMIRR vs Frequency

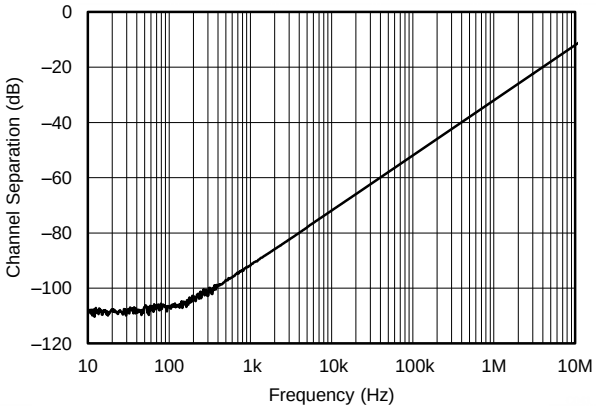


Figure 41. Channel Separation vs Frequency

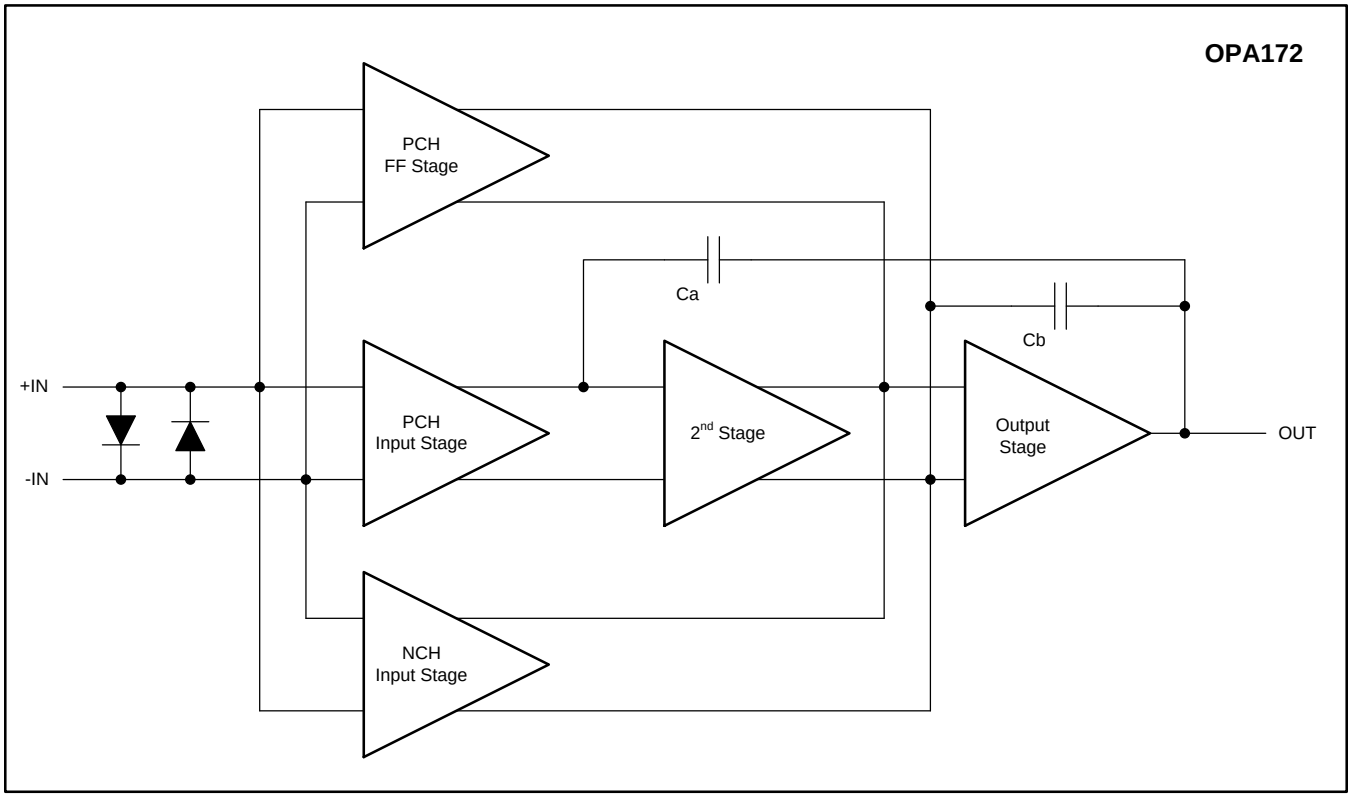
8 Detailed Description

8.1 Overview

The OPAx172 family of operational amplifiers provide high overall performance, making them ideal for many general-purpose applications. The excellent offset drift of only 1.5 µV/°C (max) provides excellent stability over the entire temperature range. In addition, the device offers very good overall performance with high CMRR, PSRR, A_{OL}, and superior THD.

The *Functional Block Diagram* section shows the simplified diagram of the OPA172 design. The design topology is a highly-optimized, three-stage amplifier with an active-feedforward gain stage.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 EMI Rejection

The OPAx172 uses integrated electromagnetic interference (EMI) filtering to reduce the effects of EMI from sources such as wireless communications and densely-populated boards with a mix of analog signal chain and digital components. EMI immunity can be improved with circuit design techniques; the OPAx172 benefits from these design improvements. Texas Instruments has developed the ability to accurately measure and quantify the immunity of an operational amplifier over a broad frequency spectrum extending from 10 MHz to 6 GHz. Figure 42 shows the results of this testing on the OPAx172. Table 2 shows the EMIRR IN+ values for the OPAx172 at particular frequencies commonly encountered in real-world applications. Applications listed in Table 2 can be centered on or operated near the particular frequency shown. Detailed information can also be found in Application Report SBOA128, *EMI Rejection Ratio of Operational Amplifiers*, available for download from www.ti.com.

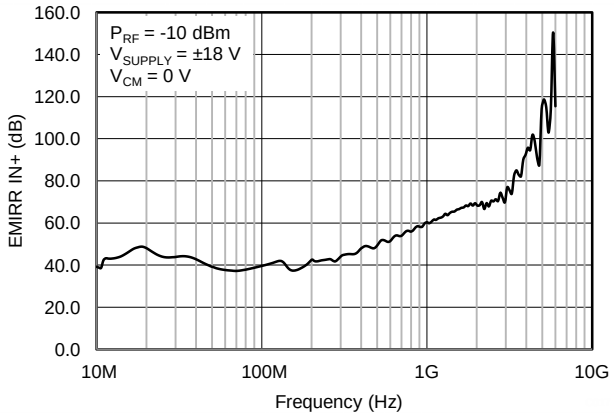


Figure 42. EMIRR Testing

Table 2. OPAx172 EMIRR IN+ for Frequencies of Interest

FREQUENCY	APPLICATION OR ALLOCATION	EMIRR IN+
400 MHz	Mobile radio, mobile satellite, space operation, weather, radar, ultrahigh frequency (UHF) applications	47.6 dB
900 MHz	Global system for mobile communications (GSM) applications, radio communication, navigation, GPS (to 1.6 GHz), GSM, aeronautical mobile, UHF applications	58.5 dB
1.8 GHz	GSM applications, mobile personal communications, broadband, satellite, L-band (1 GHz to 2 GHz)	68 dB
2.4 GHz	802.11b, 802.11g, 802.11n, Bluetooth®, mobile personal communications, industrial, scientific and medical (ISM) radio band, amateur radio and satellite, S-band (2 GHz to 4 GHz)	69.2 dB
3.6 GHz	Radiolocation, aero communication and navigation, satellite, mobile, S-band	82.9 dB
5.0 GHz	802.11a, 802.11n, aero communication and navigation, mobile communication, space and satellite operation, C-band (4 GHz to 8 GHz)	114 dB

8.3.2 Phase-Reversal Protection

The OPAx172 family has internal phase-reversal protection. Many op amps exhibit a phase reversal when the input is driven beyond the linear common-mode range. This condition is most often encountered in noninverting circuits when the input is driven beyond the specified common-mode voltage range, causing the output to reverse into the opposite rail. The input of the OPAx172 prevents phase reversal with excessive common-mode voltage. Instead, the appropriate rail limits the output voltage. This performance is shown in Figure 43.

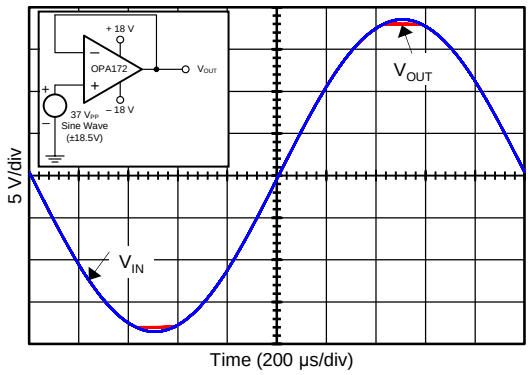


Figure 43. No Phase Reversal

8.3.3 Capacitive Load and Stability

The dynamic characteristics of the OPAx172 are optimized for commonly-used operating conditions. The combination of low closed-loop gain and high capacitive loads decreases the phase margin of the amplifier and may lead to gain peaking or oscillations. As a result, heavier capacitive loads must be isolated from the output. The simplest way to achieve this isolation is to add a small resistor (for example, R_{OUT} = 50 Ω) in series with the output. Figure 44 and Figure 45 show graphs of small-signal overshoot versus capacitive load for several values of R_{OUT}. Refer to Application Bulletin SBOA015 (AB-028), *Feedback Plots Define Op Amp AC Performance*, available for download from www.ti.com, for details of analysis techniques and application circuits.

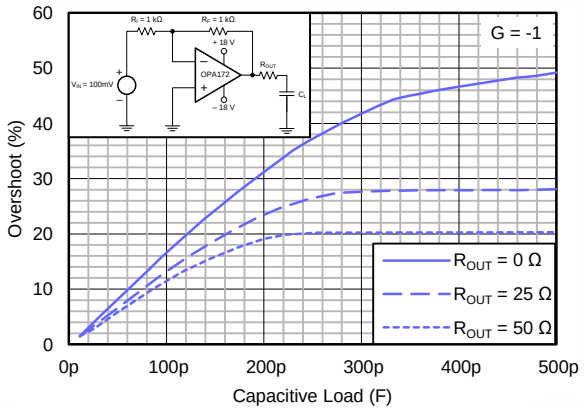


Figure 44. Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)

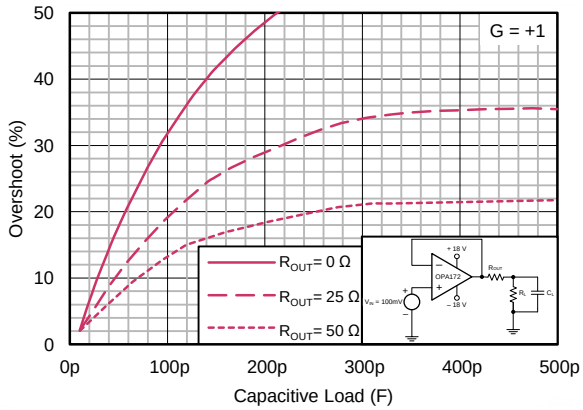


Figure 45. Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)

8.4 Device Functional Modes

8.4.1 Common-Mode Voltage Range

The input common-mode voltage range of the OPAx172 series extends 100 mV below the negative rail and within 2 V of the top rail for normal operation.

This device can operate with full rail-to-rail input 100 mV beyond the top rail, but with reduced performance within 2 V of the top rail. The typical performance in this range is summarized in Table 3.

Table 3. Typical Performance Range (V_S = ±18 V)

PARAMETER	MIN	TYP	MAX	UNIT
Input Common-Mode Voltage	(V+) – 2		(V+) + 0.1	V
Offset voltage		5		mV
Offset voltage vs temperature (T_A = –40°C to +125°C)		10		µV/°C
Common-mode rejection		70		dB
Open-loop gain		60		dB
Gain bandwidth product (GBP)		4		MHz
Slew rate		4		V/µs
Noise at f = 1 kHz		22		nV/√Hz

8.4.2 Electrical Overstress

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress. These questions tend to focus on the device inputs, but may involve the supply voltage terminals or even the output terminal. Each of these different terminal functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the terminal. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

A good understanding of this basic ESD circuitry and its relevance to an electrical overstress event is helpful. Figure 46 illustrates the ESD circuits contained in the OPAx172 (indicated by the dashed line area). The ESD protection circuitry involves several current-steering diodes connected from the input and output terminals and routed back to the internal power-supply lines, where the diodes meet at an absorption device internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.

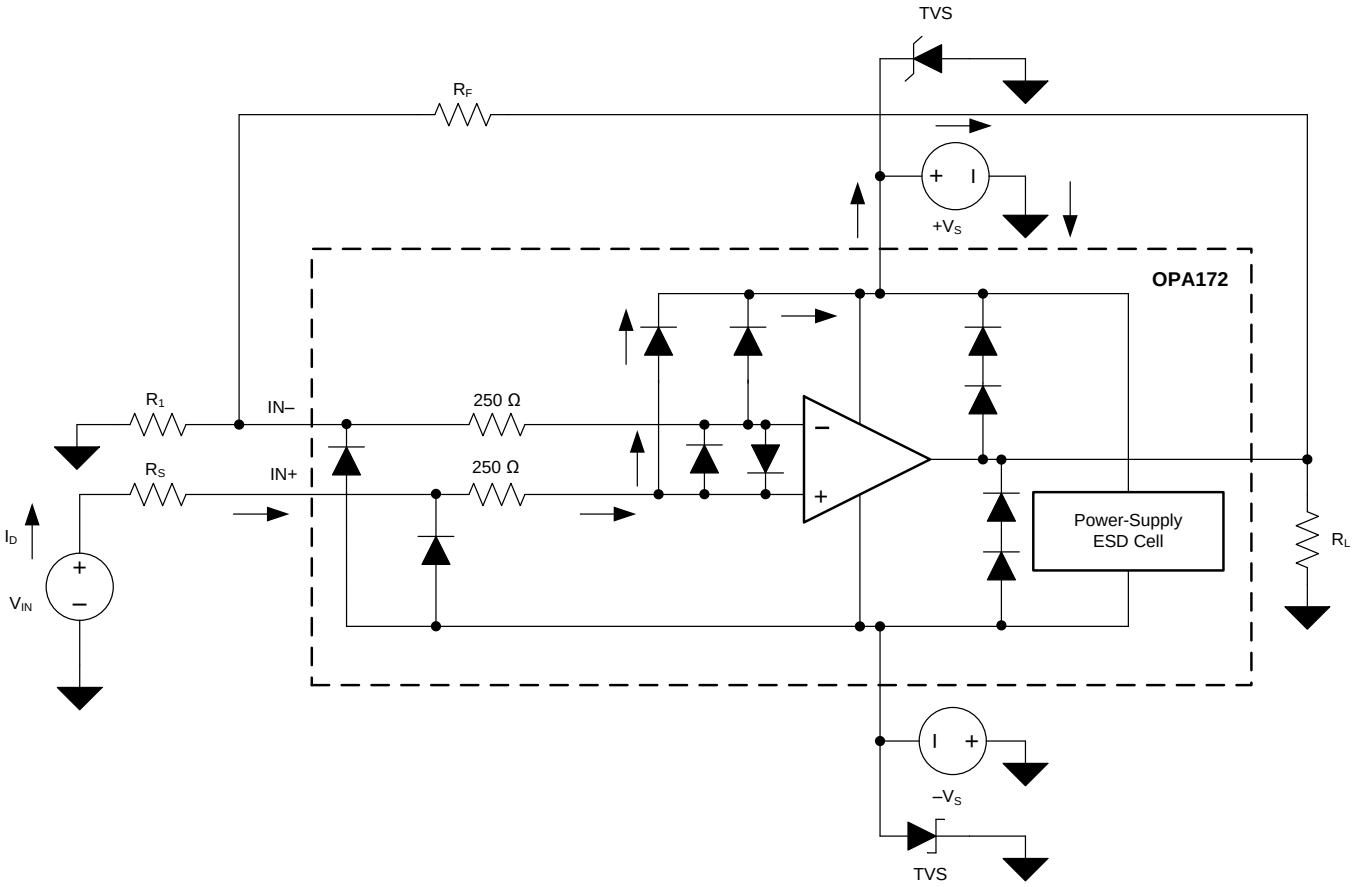


Figure 46. Equivalent Internal ESD Circuitry Relative to a Typical Circuit Application

An ESD event produces a short-duration, high-voltage pulse that is transformed into a short-duration, high-current pulse while discharging through a semiconductor device. The ESD protection circuits are designed to provide a current path around the operational amplifier core to prevent damage. The energy absorbed by the protection circuitry is then dissipated as heat.

When an ESD voltage develops across two or more amplifier device terminals, current flows through one or more steering diodes. Depending on the path that the current takes, the absorption device may activate. The absorption device has a trigger, or threshold voltage, that is above the normal operating voltage of the OPAx172 but below the device breakdown voltage level. When this threshold is exceeded, the absorption device quickly activates and clamps the voltage across the supply rails to a safe level.

When the operational amplifier connects into a circuit (as shown in Figure 46), the ESD protection components are intended to remain inactive and do not become involved in the application circuit operation. However, circumstances may arise where an applied voltage exceeds the operating voltage range of a given terminal. If this condition occurs, there is a risk that some internal ESD protection circuits can turn on and conduct current. Any such current flow occurs through steering-diode paths and rarely involves the absorption device.

Figure 46 shows a specific example where the input voltage (V_{IN}) exceeds the positive supply voltage ($+V_S$) by 500 mV or more. Much of what happens in the circuit depends on the supply characteristics. If $+V_S$ can sink the current, one of the upper input steering diodes conducts and directs current to $+V_S$. Excessively high current levels can flow with increasingly higher V_{IN}. As a result, the data sheet specifications recommend that applications limit the input current to 10 mA.

If the supply is not capable of sinking the current, V_{IN} can begin sourcing current to the operational amplifier, and then take over as the source of positive supply voltage. The danger in this case is that the voltage can rise to levels that exceed the operational amplifier absolute maximum ratings.

Another common question involves what happens to the amplifier if an input signal is applied to the input while the power supplies $+V_S$ or $–V_S$ are at 0 V. Again, this question depends on the supply characteristic while at 0 V, or at a level below the input-signal amplitude. If the supplies appear as high impedance, then the input source supplies the operational amplifier current through the current-steering diodes. This state is not a normal bias condition; most likely, the amplifier will not operate normally. If the supplies are low impedance, then the current through the steering diodes can become quite high. The current level depends on the ability of the input source to deliver current, and any resistance in the input path.

If there is any uncertainty about the ability of the supply to absorb this current, add external zener diodes to the supply terminals; see Figure 46. Select the zener voltage so that the diode does not turn on during normal operation. However, the zener voltage must be low enough so that the zener diode conducts if the supply terminal begins to rise above the safe-operating, supply-voltage level.

The OPAx172 input terminals are protected from excessive differential voltage with back-to-back diodes; see Figure 46. In most circuit applications, the input protection circuitry has no effect. However, in low-gain or G = 1 circuits, fast-ramping input signals can forward-bias these diodes because the output of the amplifier cannot respond rapidly enough to the input ramp. If the input signal is fast enough to create this forward-bias condition, limit the input signal current to 10 mA or less. If the input signal current is not inherently limited, an input series resistor can be used to limit the input signal current. This input series resistor degrades the low-noise performance of the OPAx172. Figure 46 illustrates an example configuration that implements a current-limiting feedback resistor.

8.4.3 Overload Recovery

Overload recovery is defined as the time it takes for the op amp output to recover from the saturated state to the linear state. The output devices of the op amp enter the saturation region when the output voltage exceeds the rated operating voltage, either due to the high input voltage or the high gain. After the device enters the saturation region, the charge carriers in the output devices need time to return back to the normal state. After the charge carriers return back to the equilibrium state, the device begins to slew at the normal slew rate. Thus, the propagation delay in case of an overload condition is the sum of the overload recovery time and the slew time. The overload recovery time for the OPAx172 is approximately 200 ns.

9 Applications and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The OPAx172 family of amplifiers is specified for operation from 4.5 V to 36 V (±2.25 V to ±18 V). Many of the specifications apply from –40°C to +125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the *Typical Characteristics*.

9.2 Typical Applications

The following application examples highlight only a few of the circuits where the OPAx172 can be used.

9.2.1 Capacitive Load Drive Solution Using an Isolation Resistor

The OPA172 can be used capacitive loads such as cable shields, reference buffers, MOSFET gates, and diodes. The circuit uses an isolation resistor (R_{ISO}) to stabilize the output of an op amp. R_{ISO} modifies the open-loop gain of the system to ensure the circuit has sufficient phase margin.

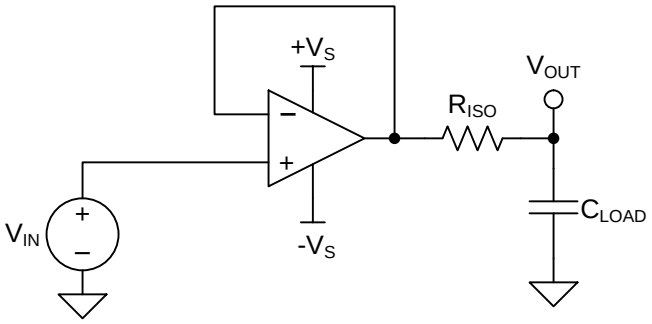


Figure 47. Unity-Gain Buffer with R_{ISO} Stability Compensation

9.2.1.1 Design Requirements

The design requirements are:

- Supply voltage: 30 V (±15 V)
- Capacitive loads: 100 pF, 1000 pF, 0.01 µF, 0.1 µF, and 1 µF
- Phase margin: 45° and 60°

Typical Applications (continued)

9.2.1.2 Detailed Design Procedure

Figure 47 depicts a unity-gain buffer driving a capacitive load. Equation 1 shows the transfer function for the circuit in Figure 47. Not depicted in Figure 47 is the open-loop output resistance of the op amp, R_o.

$$T(s) = \frac{1 + C_{LOAD} \times R_{ISO} \times s}{1 + (R_o + R_{ISO}) \times C_{LOAD} \times s} \quad (1)$$

The transfer function in Equation 1 has a pole and a zero. The frequency of the pole (f_p) is determined by (R_o + R_{ISO}) and C_{LOAD}. Components R_{ISO} and C_{LOAD} determine the frequency of the zero (f_z). A stable system is obtained by selecting R_{ISO} such that the rate of closure (ROC) between the open-loop gain (A_{OL}) and 1 / β is 20 dB per decade. Figure 48 shows the concept. Note that the 1 / β curve for a unity-gain buffer is 0 dB.

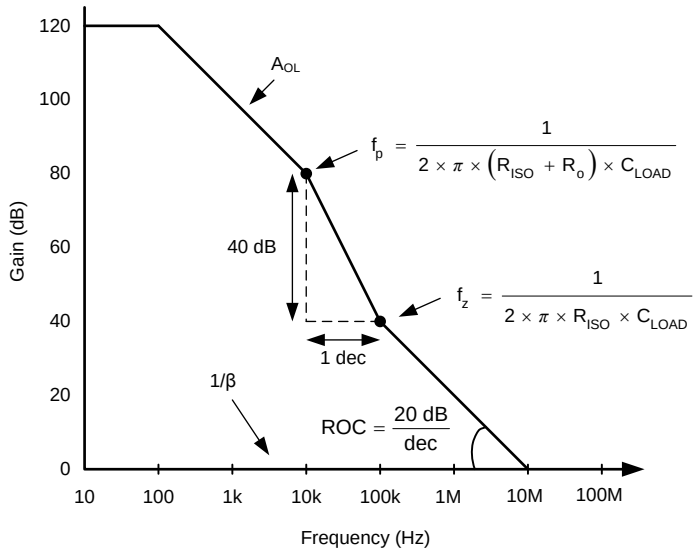


Figure 48. Unity-Gain Amplifier with R_{ISO} Compensation

ROC stability analysis is typically simulated. The validity of the analysis depends on multiple factors, especially the accurate modeling of R_o. In addition to simulating the ROC, a robust stability analysis includes a measurement of overshoot percentage and ac gain peaking of the circuit using a function generator, oscilloscope, and gain and phase analyzer. Phase margin is then calculated from these measurements. Table 4 shows the overshoot percentage and ac gain peaking that correspond to phase margins of 45° and 60°. For more details on this design and other alternative devices that can be used in place of the OPA172, refer to the precision design, *Capacitive Load Drive Solution using an Isolation Resistor* (TIPD128).

Table 4. Phase Margin versus Overshoot and AC Gain Peaking

PHASE MARGIN	OVERSHOOT	AC GAIN PEAKING
45°	23.3%	2.35 dB
60°	8.8%	0.28 dB

9.2.1.3 Application Curve

The OPA172 meets the supply voltage requirements of 30 V. The OPA172 is tested for various capacitive loads and R_{ISO} is adjusted to get an overshoot corresponding to Table 4. The results of the these tests are summarized in Figure 49.

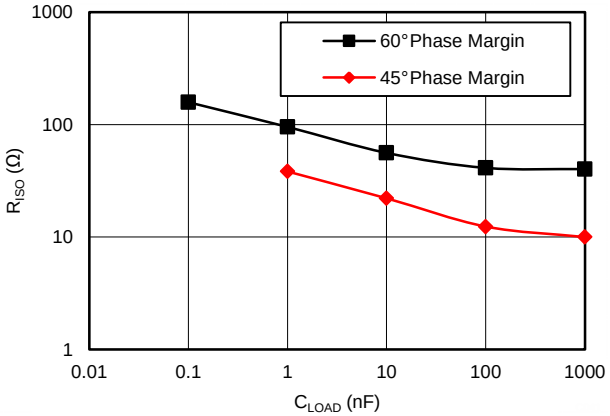


Figure 49. R_{ISO} vs C_{LOAD}

9.2.2 Bidirectional Current Source

The improved Howland current-pump topology shown in Figure 50 provides excellent performance because of the extremely tight tolerances of the on-chip resistors of the INA132. By buffering the output using an OPA172, the output current the circuit is able to deliver is greatly extended.

The circuit dc transfer function is shown in Equation 2:

$$I_{OUT} = V_{IN} / R1 \quad (2)$$

The OPA172 can also be used as the feedback amplifier because the low bias current minimizes error voltages produced across R1. However, for improved performance, select a FET-input device with extremely low offset, such as the OPA192, OPA140, or OPA188 as the feedback amplifier.

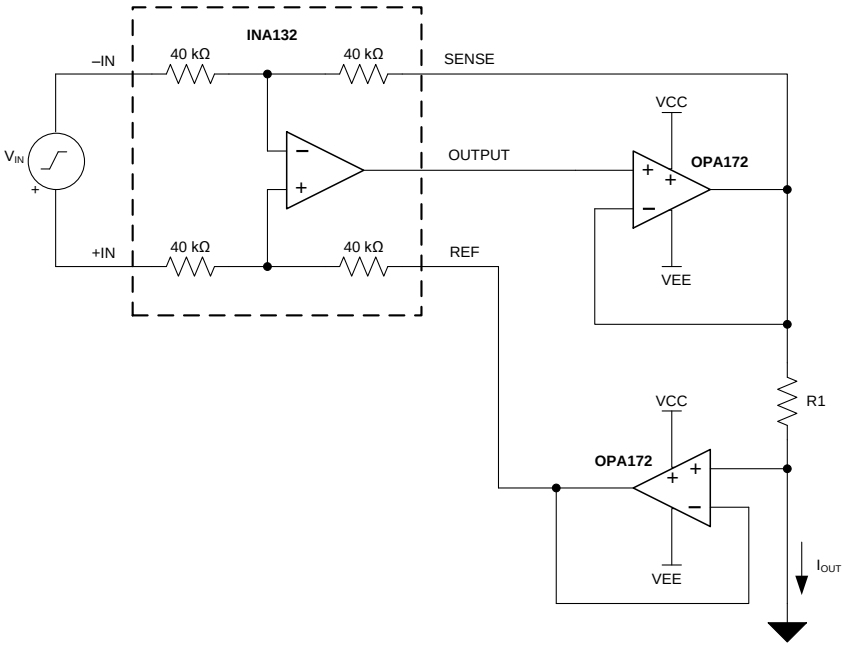


Figure 50. Bidirectional Current Source

9.2.3 JFET-Input Low-Noise Amplifier

Figure 51 shows a low-noise composite amplifier built by adding a low noise JFET pair (Q1 and Q2) as an input preamplifier for the OPA172. Transistors Q3 and Q4 form a 2-mA current sink that biases each JFET with 1 mA of drain current. Using 3.9-kΩ drain resistors produces a gain of approximately 10 in the input amplifier, making the extremely-low, broadband-noise spectral density of the JFET pair, Q1 and Q2, the dominant noise source of the amplifier. The output impedance of the input differential amplifier is large enough that a FET-input amplifier such as the OPA172 provides superior noise performance over bipolar-input amplifiers.

The gain of the composite amplifier is given by Equation 3:

$$A_V = (1 + R3 / R4) \quad (3)$$

The resistances shown are standard 1% resistor values that produce a gain of approximately 100 (99.26) with 68° of phase margin. Gains less than 10 may require additional compensation methods to provide stability. Select low resistor values to minimize the resistor thermal noise contribution to the total output noise.

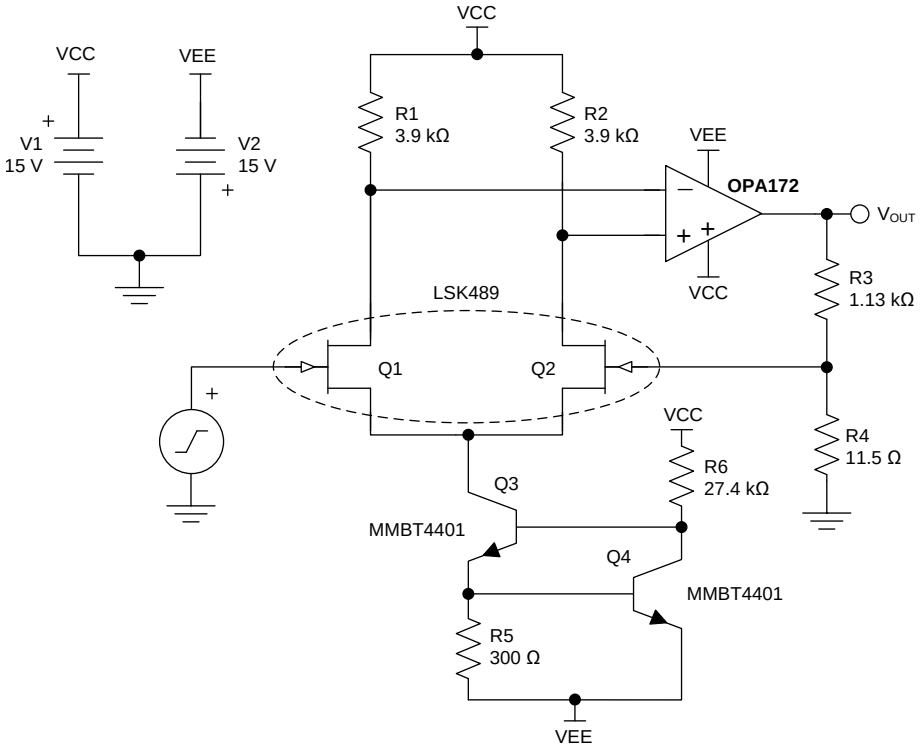


Figure 51. JFET-Input Low-Noise Amplifier

10 Power-Supply Recommendations

The OPA172 is specified for operation from 4.5 V to 36 V (±2.25 V to ±18 V); many specifications apply from –40°C to +125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the *Typical Characteristics*.

CAUTION

Supply voltages larger than 40 V can permanently damage the device; see the *Absolute Maximum Ratings*.

Place 0.1-µF bypass capacitors close to the power-supply terminals to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see the *Layout* section.

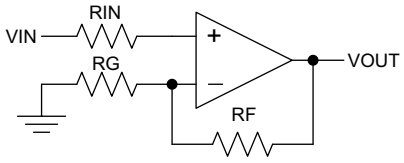
11 Layout

11.1 Layout Guidelines

For best operational performance of the device, use good printed circuit board (PCB) layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and op amp itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds paying attention to the flow of the ground current. For more detailed information refer to SLOA089, *Circuit Board Layout Techniques*.
- In order to reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular as opposed to in parallel with the noisy trace is preferable.
- Place the external components as close to the device as possible. As shown in Figure 52, keeping RF and RG close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

11.2 Layout Example



(Schematic Representation)

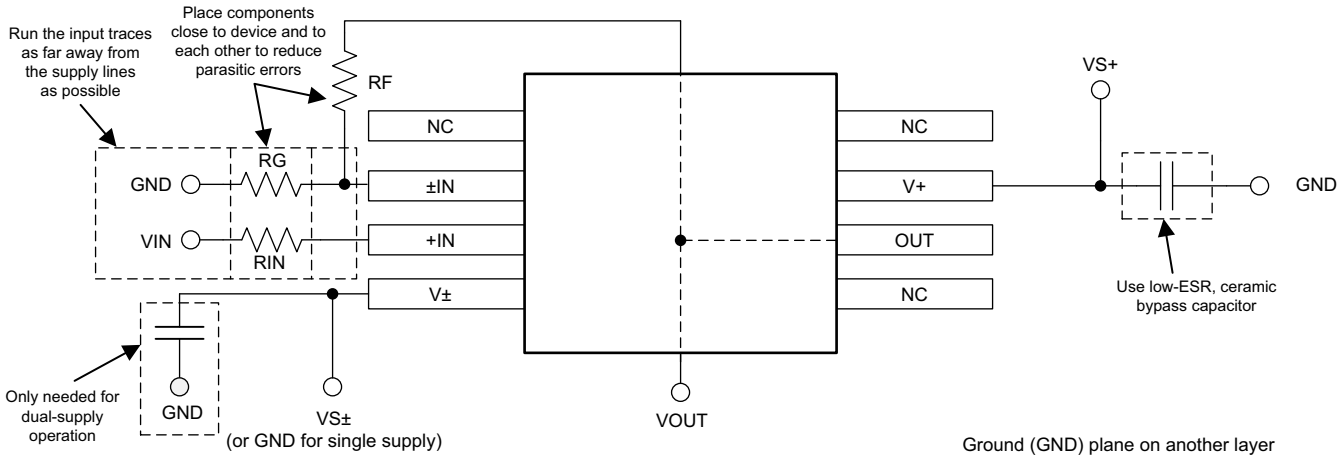


Figure 52. Operational Amplifier Board Layout for Noninverting Configuration

12 Device and Documentation Support

12.1 Device Support

12.1.1 Development Support

12.1.1.1 TINA-TI™ (Free Software Download)

TINA™ is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI is a free, fully-functional version of the TINA software, preloaded with a library of macro models in addition to a range of both passive and active models. TINA-TI provides all the conventional dc, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a free download from the Analog eLab Design Center, TINA-TI offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

NOTE

These files require that either the TINA software (from DesignSoft™) or TINA-TI software be installed. Download the free TINA-TI software from the TINA-TI folder.

12.2 Documentation Support

12.2.1 Related Documentation

SBOA015 (AB-028) — *Feedback Plots Define Op Amp AC Performance*.

SLOA089 — *Circuit Board Layout Techniques*.

SLOD006 — *Op Amps for Everyone*.

SBOA128 — *EMI Rejection Ratio of Operational Amplifiers*.

TIPD128 — *Capacitive Load Drive Solution using an Isolation Resistor*.

12.3 Related Links

Table 5 lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 5. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
OPA172	Click here	Click here	Click here	Click here	Click here
OPA2172	Click here	Click here	Click here	Click here	Click here
OPA4172	Click here	Click here	Click here	Click here	Click here

12.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.5 Trademarks

E2E is a trademark of Texas Instruments.
TINA-TI is a trademark of Texas Instruments, Inc and DesignSoft, Inc.
Bluetooth is a registered trademark of Bluetooth SIG, Inc.
TINA, DesignSoft are trademarks of DesignSoft, Inc.
All other trademarks are the property of their respective owners.

12.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA172ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA172	Samples
OPA172IDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OUWQ	Samples
OPA172IDBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OUWQ	Samples
OPA172IDCKR	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	SIU	Samples
OPA172IDCKT	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	SIU	Samples
OPA172IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA172	Samples
OPA2172ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	O2172A	Samples
OPA2172IDGK	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	OVJQ	Samples
OPA2172IDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	OVJQ	Samples
OPA2172IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	O2172A	Samples
OPA2172IDRGR	ACTIVE	SON	DRG	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OP2172	Samples
OPA2172IDRGT	ACTIVE	SON	DRG	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OP2172	Samples
OPA4172ID	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	OPA4172	Samples
OPA4172IDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	OPA4172	Samples
OPA4172IPW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA4172	Samples
OPA4172IPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA4172	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

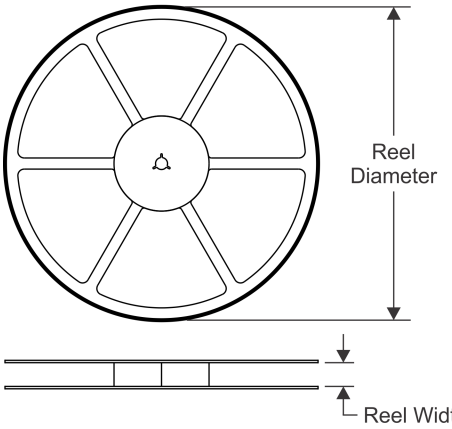
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

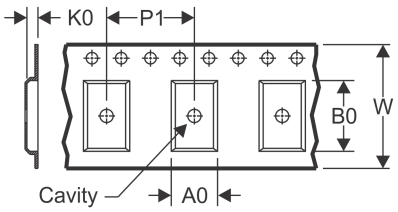
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

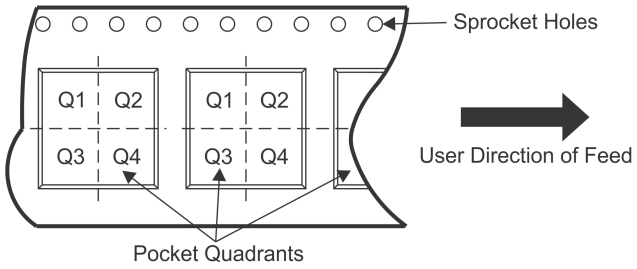


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

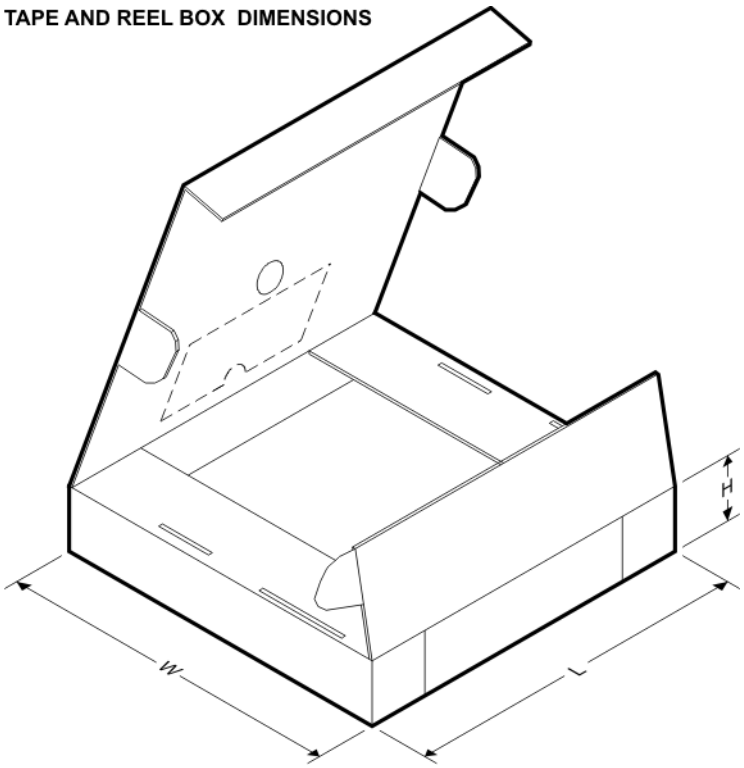
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA172IDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
OPA172IDBVT	SOT-23	DBV	5	250	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
OPA172IDCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
OPA172IDCKT	SC70	DCK	5	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
OPA172IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA2172IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2172IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA2172IDRGR	SON	DRG	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
OPA2172IDRGT	SON	DRG	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
OPA4172IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
OPA4172IPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

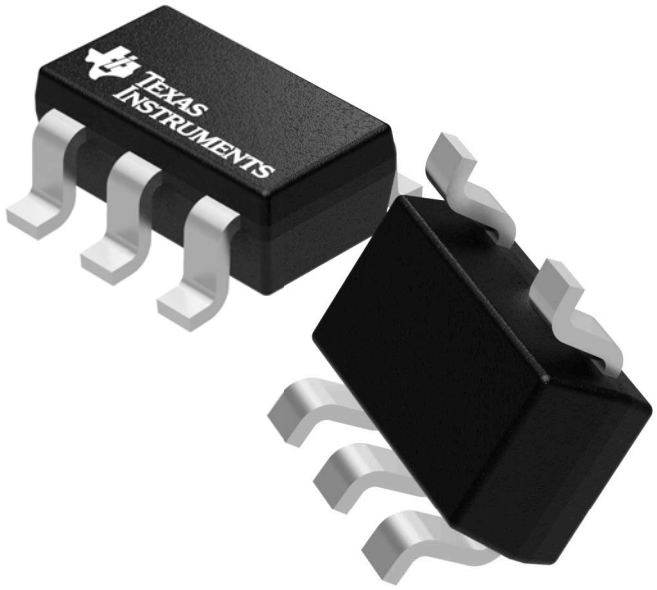


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA172IDBVR	SOT-23	DBV	5	3000	223.0	270.0	35.0
OPA172IDBVT	SOT-23	DBV	5	250	223.0	270.0	35.0
OPA172IDCKR	SC70	DCK	5	3000	180.0	180.0	18.0
OPA172IDCKT	SC70	DCK	5	250	180.0	180.0	18.0
OPA172IDR	SOIC	D	8	2500	367.0	367.0	35.0
OPA2172IDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
OPA2172IDR	SOIC	D	8	2500	367.0	367.0	35.0
OPA2172IDRGR	SON	DRG	8	3000	367.0	367.0	35.0
OPA2172IDRGT	SON	DRG	8	250	210.0	185.0	35.0
OPA4172IDR	SOIC	D	14	2500	367.0	367.0	38.0
OPA4172IPWR	TSSOP	PW	14	2000	367.0	367.0	35.0

DBV 5 SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



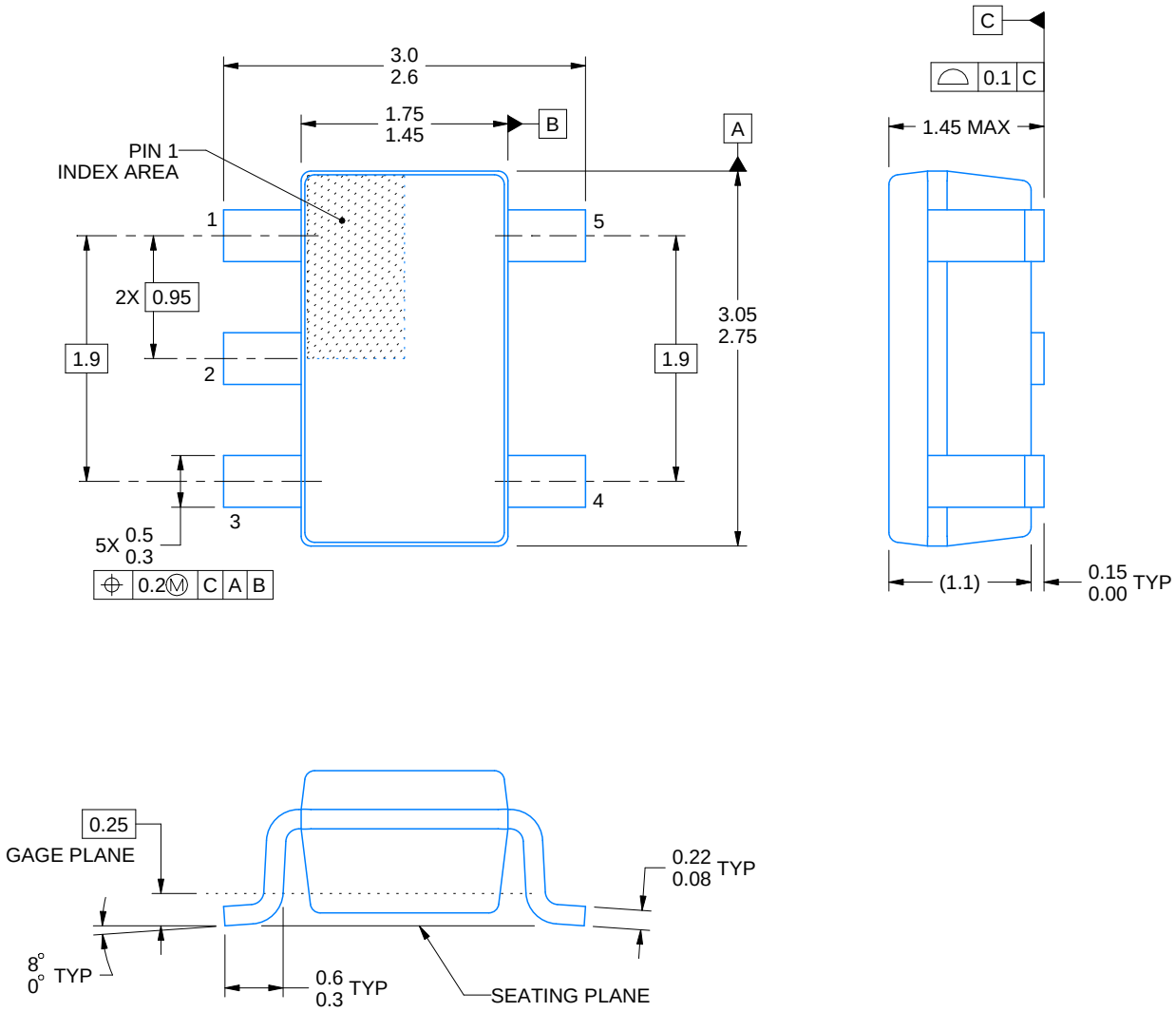
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

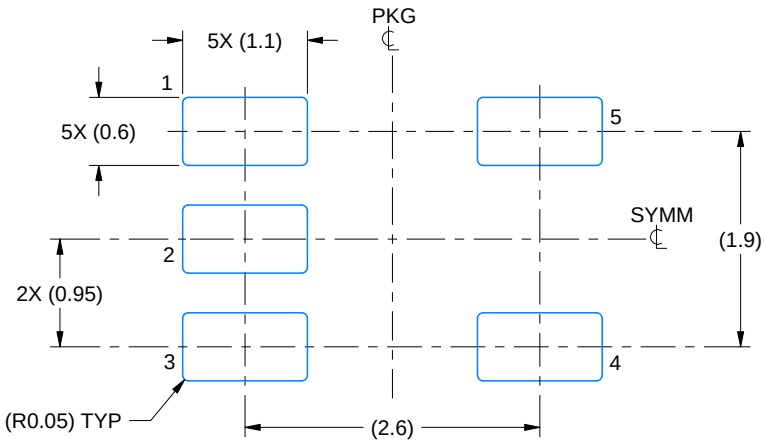
SMALL OUTLINE TRANSISTOR



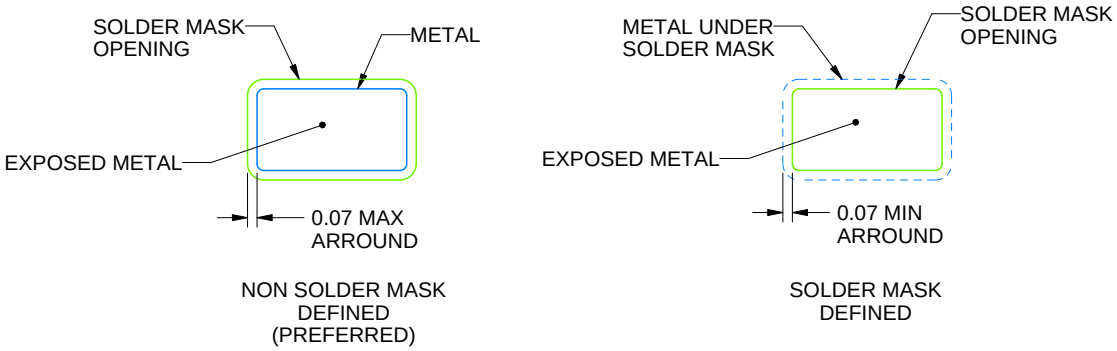
4214839/C 04/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

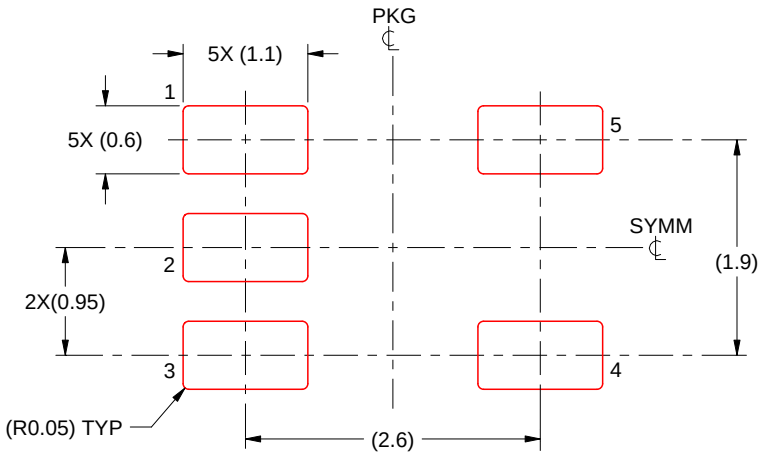


SOLDER MASK DETAILS

4214839/C 04/2017

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



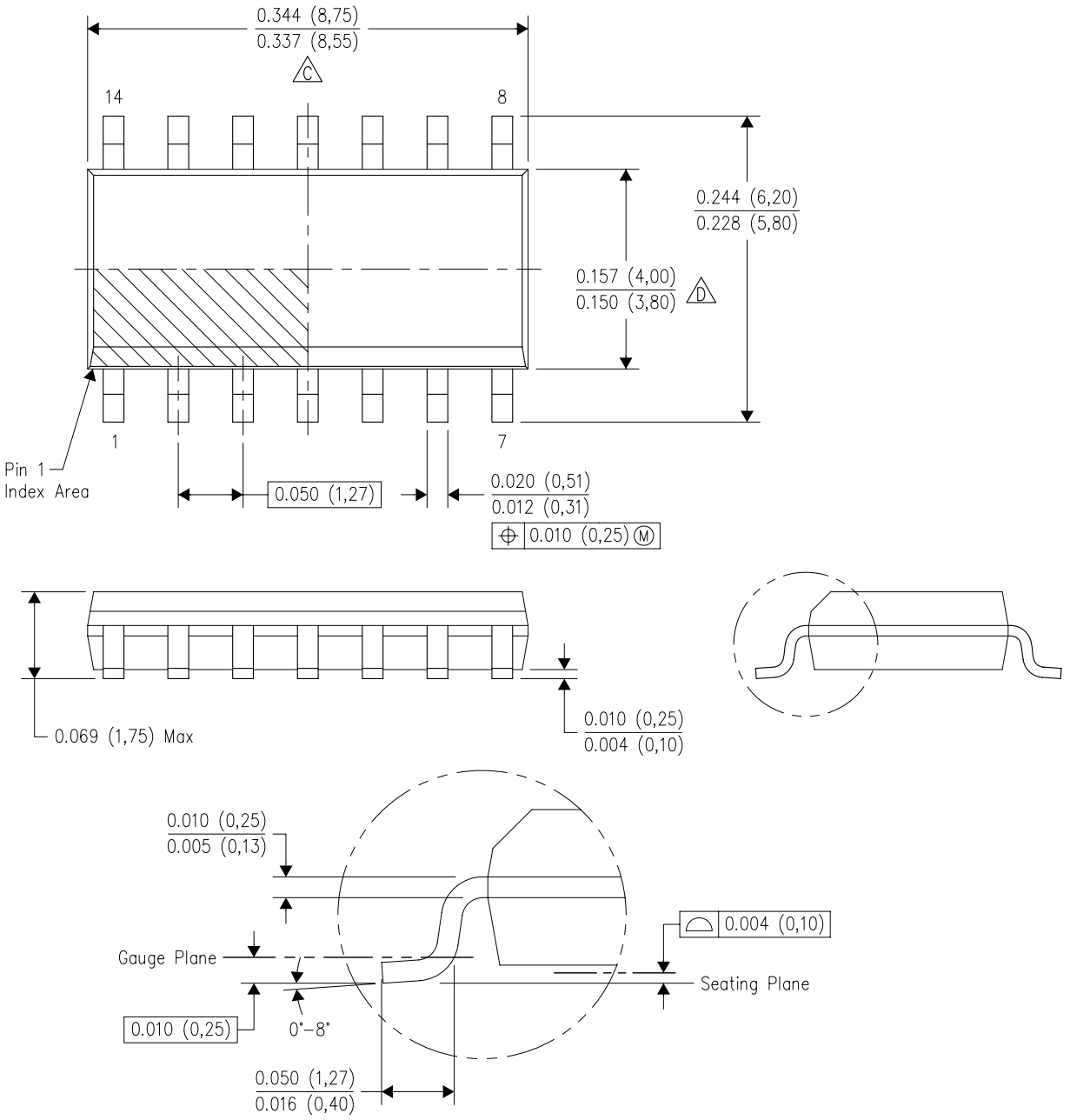
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/C 04/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

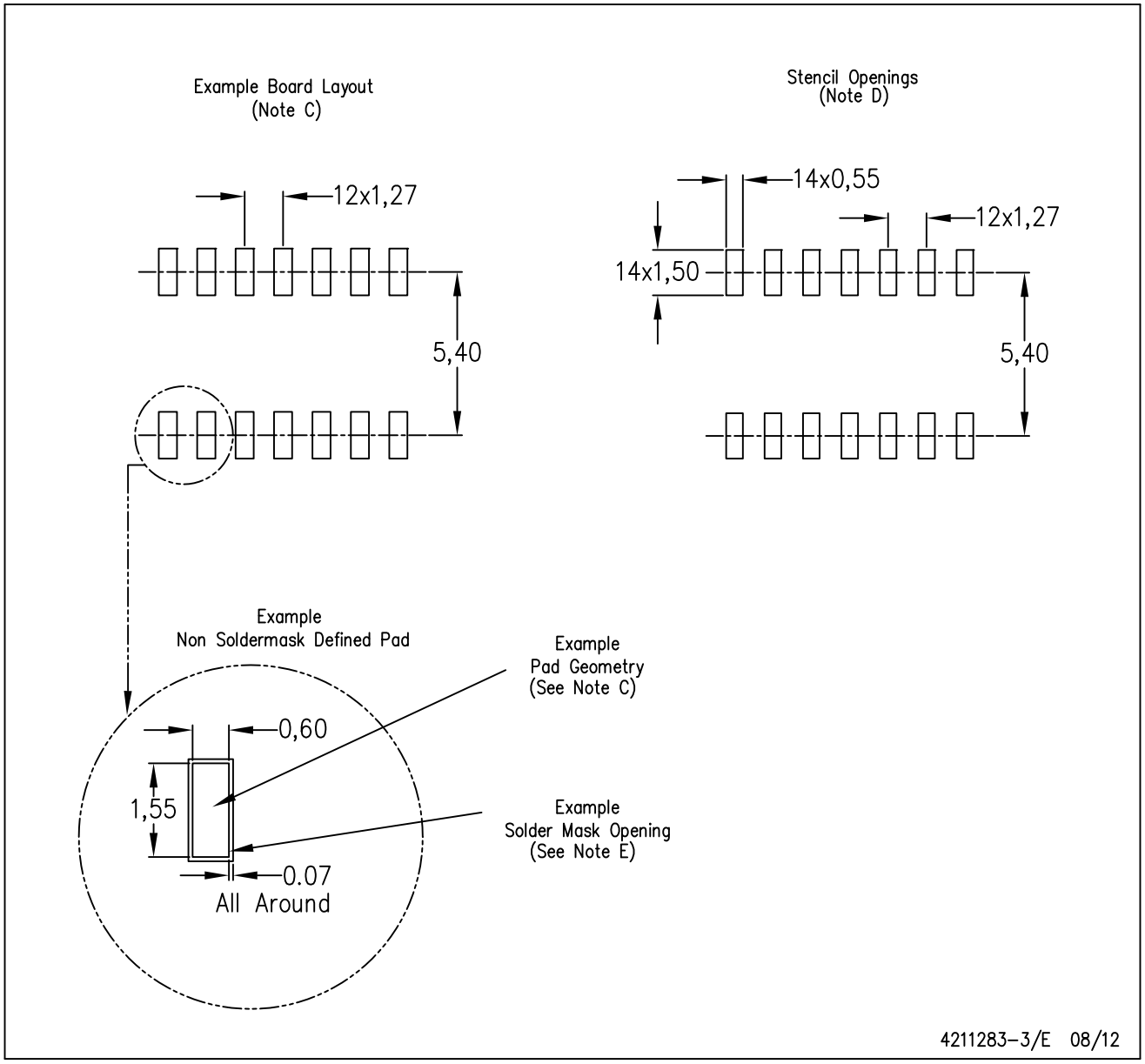
D (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040047–5/M 06/11

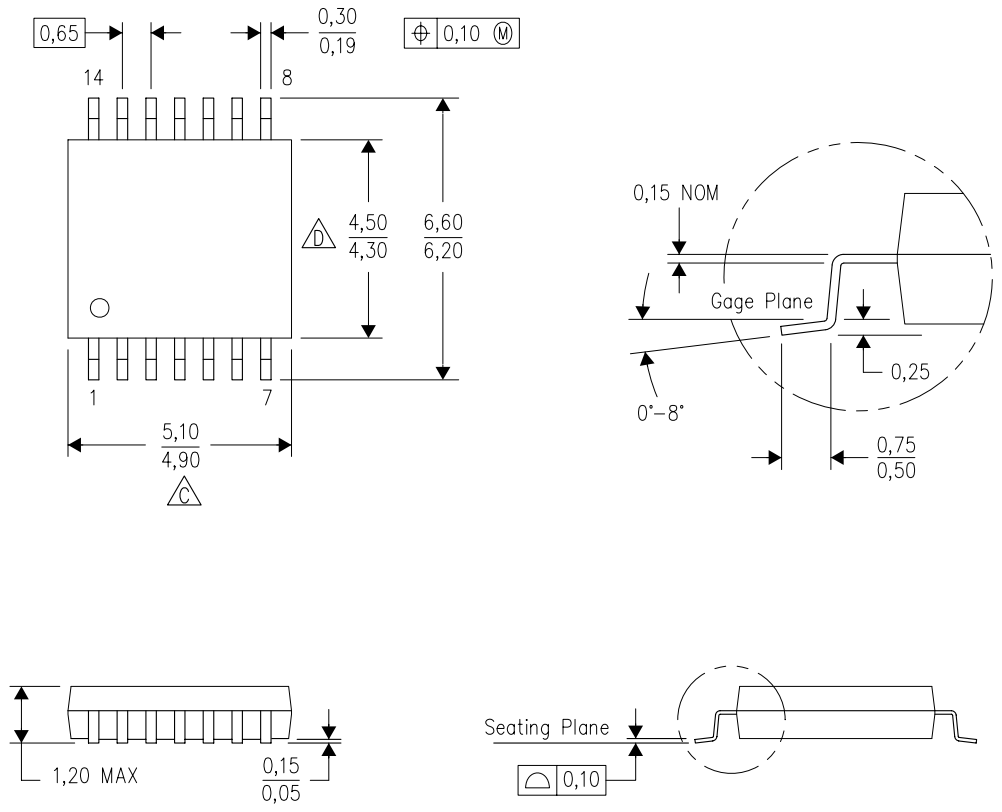
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

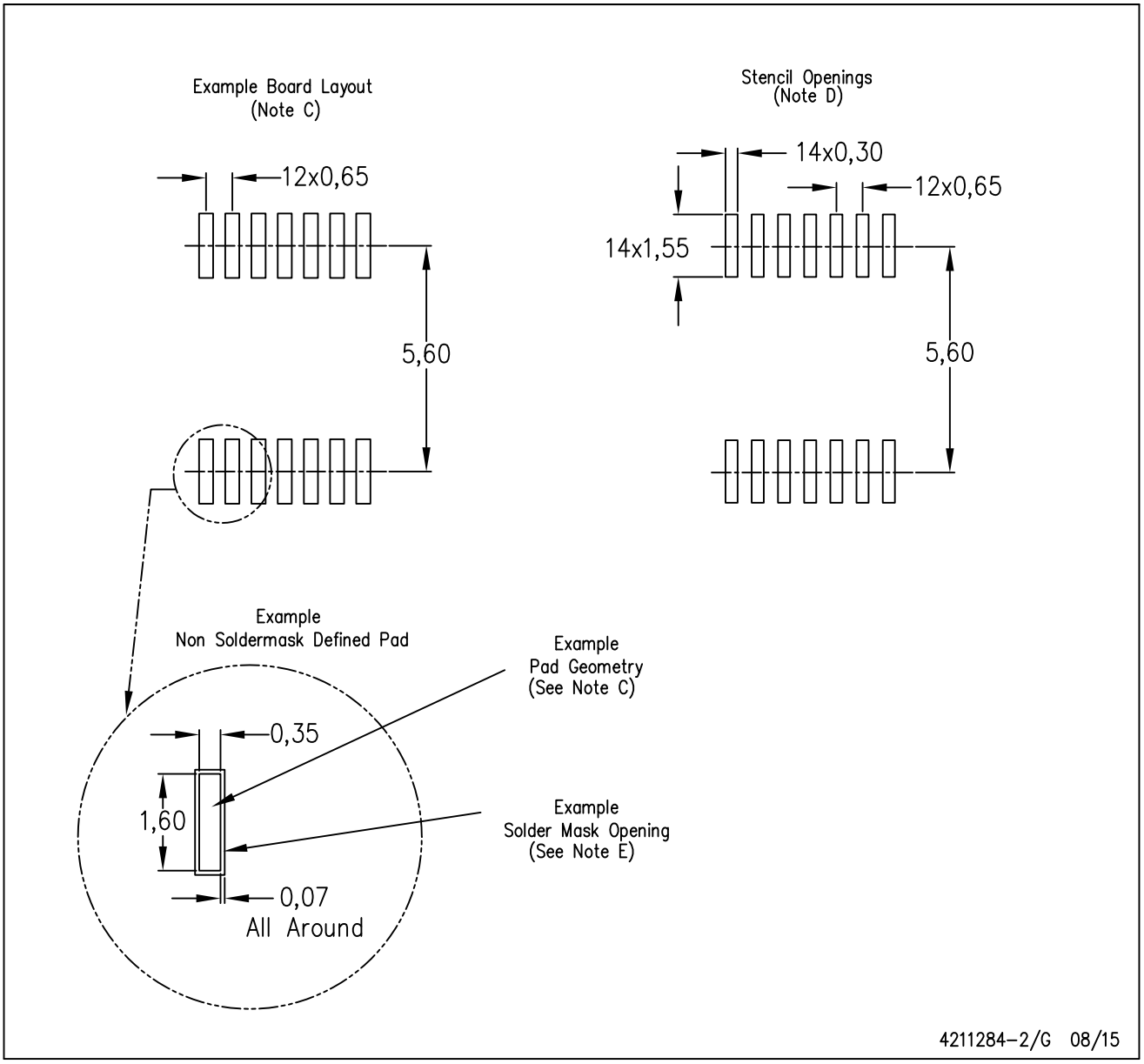
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040064–3/G 02/11

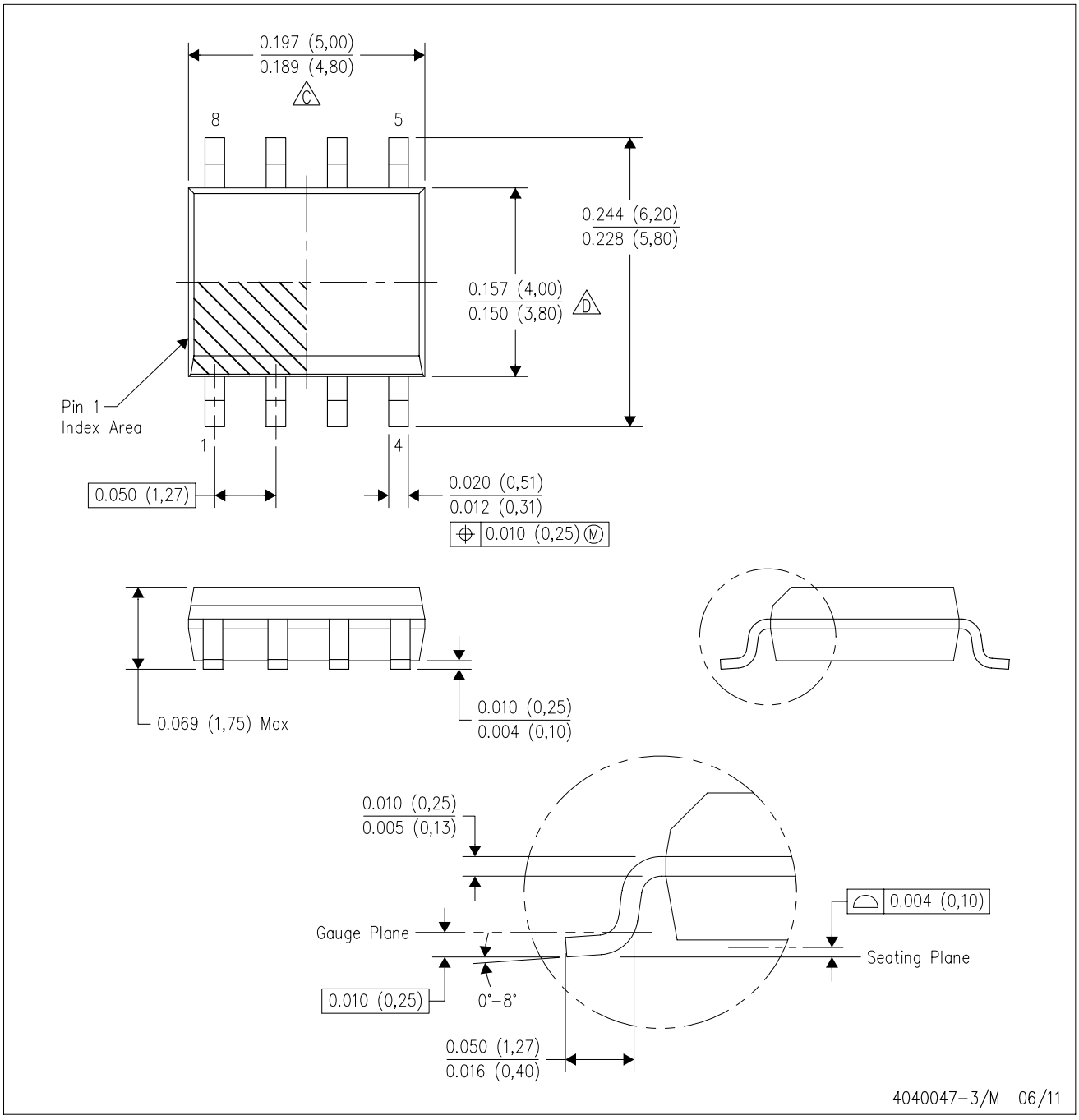
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



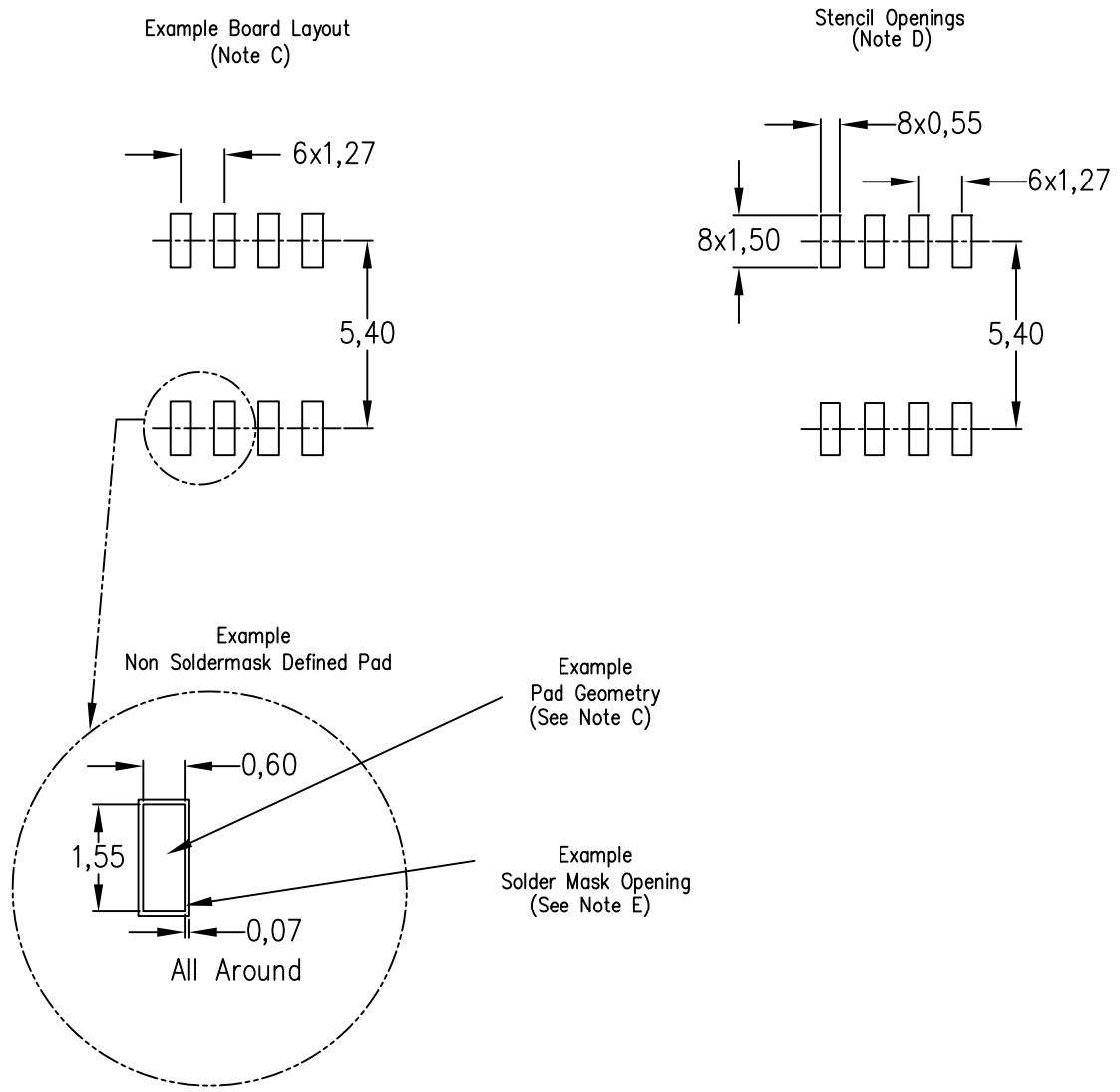
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



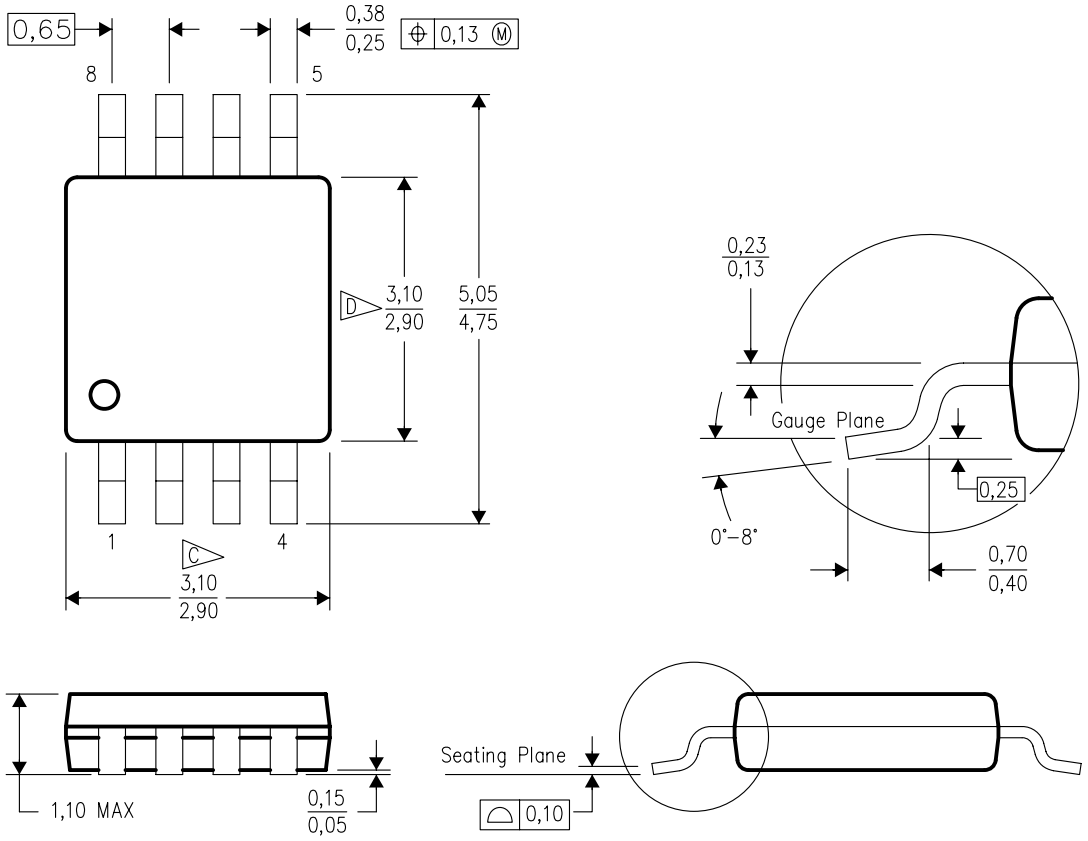
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

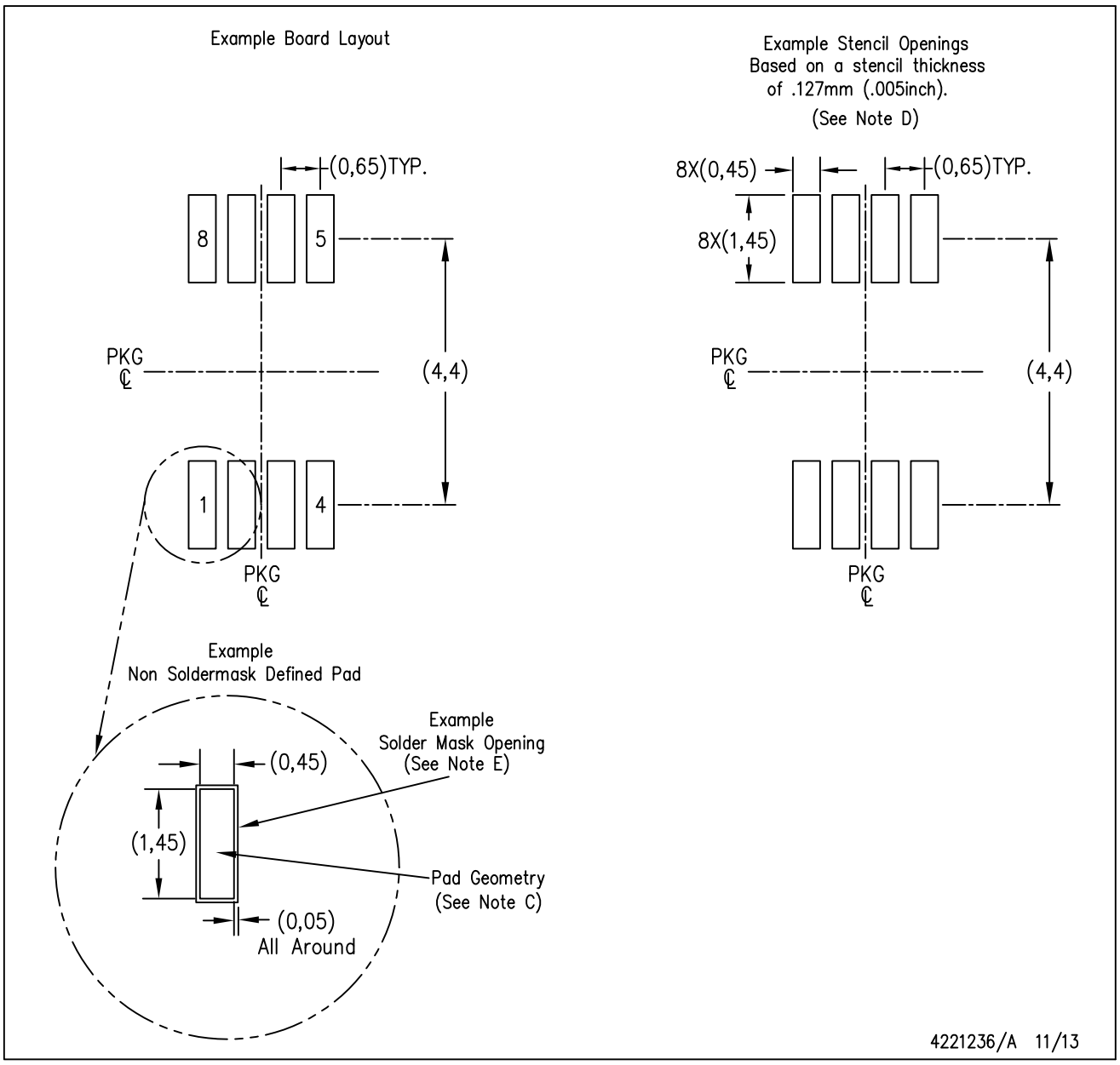
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

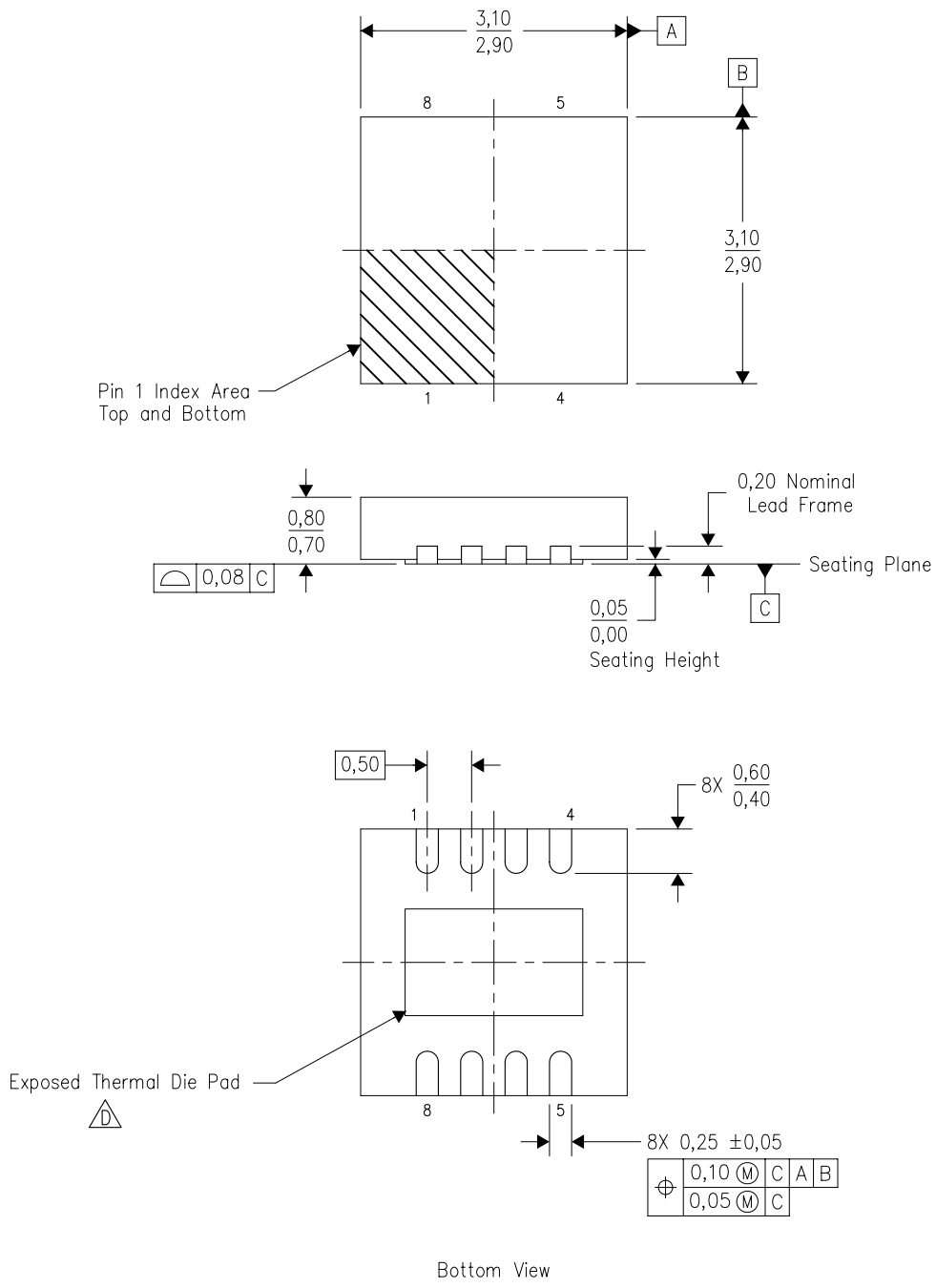
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DRG (S–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. SON (Small Outline No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. JEDEC MO–229 package registration pending.

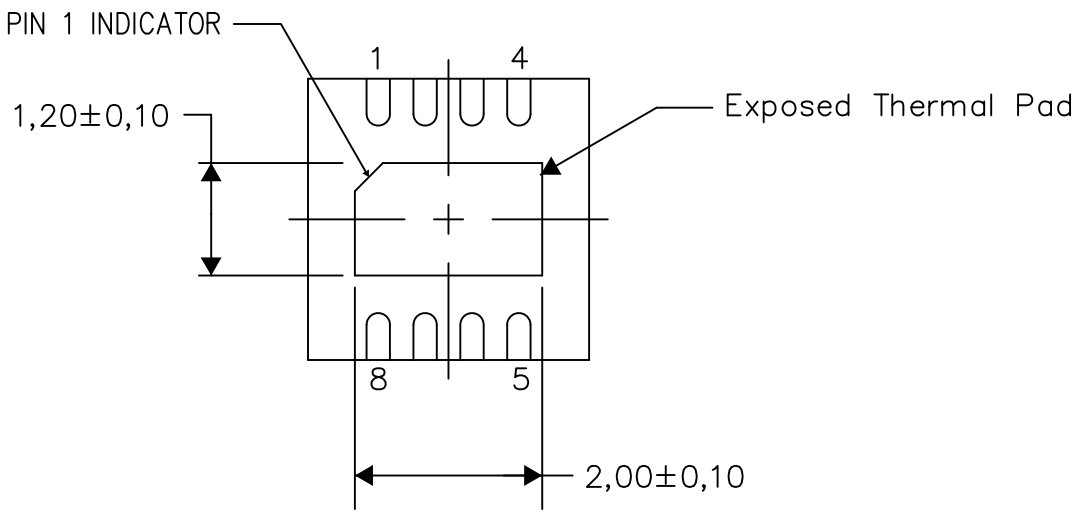
DRG (S–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



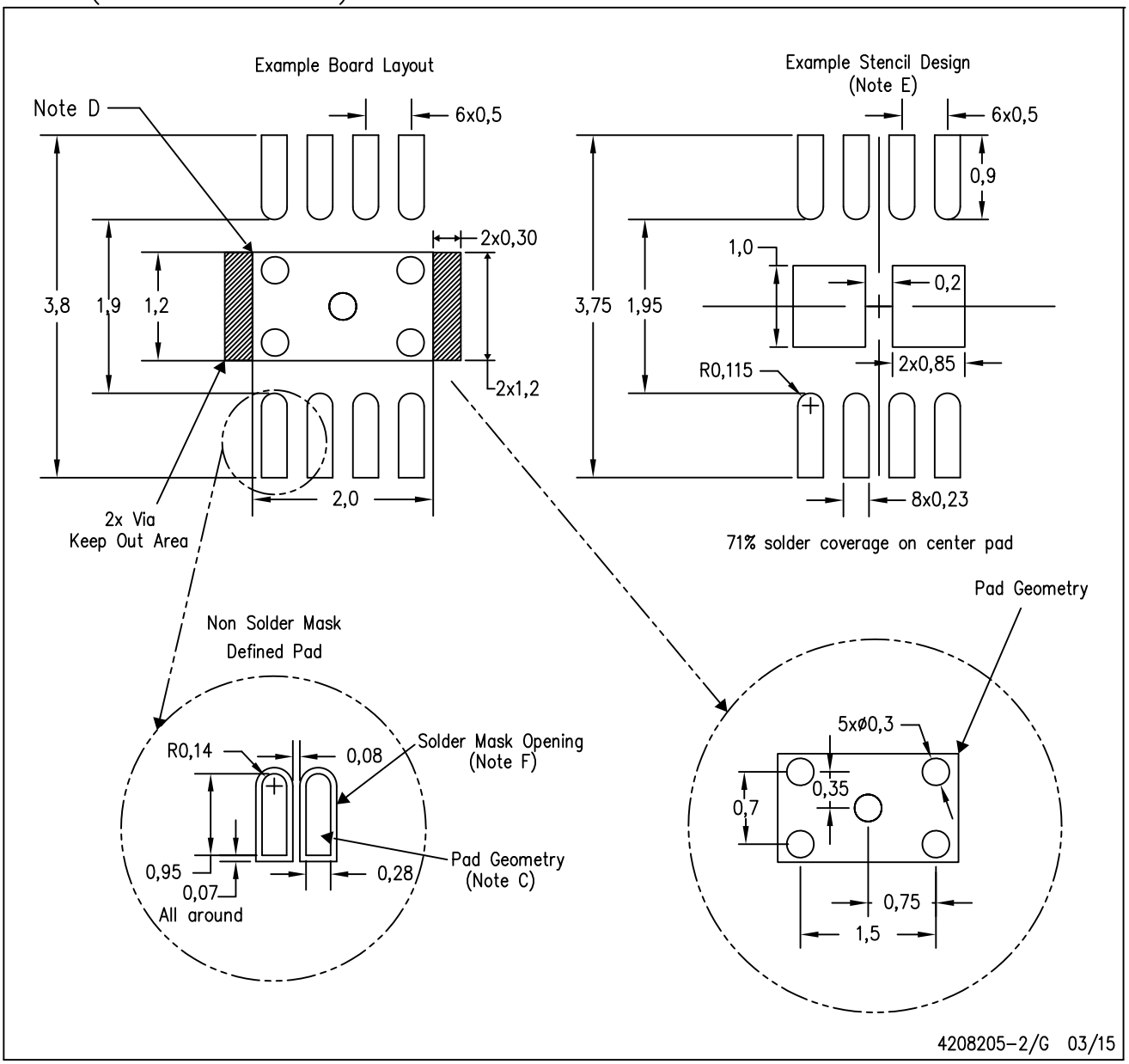
Bottom View

Exposed Thermal Pad Dimensions

4206881–2/I 03/15

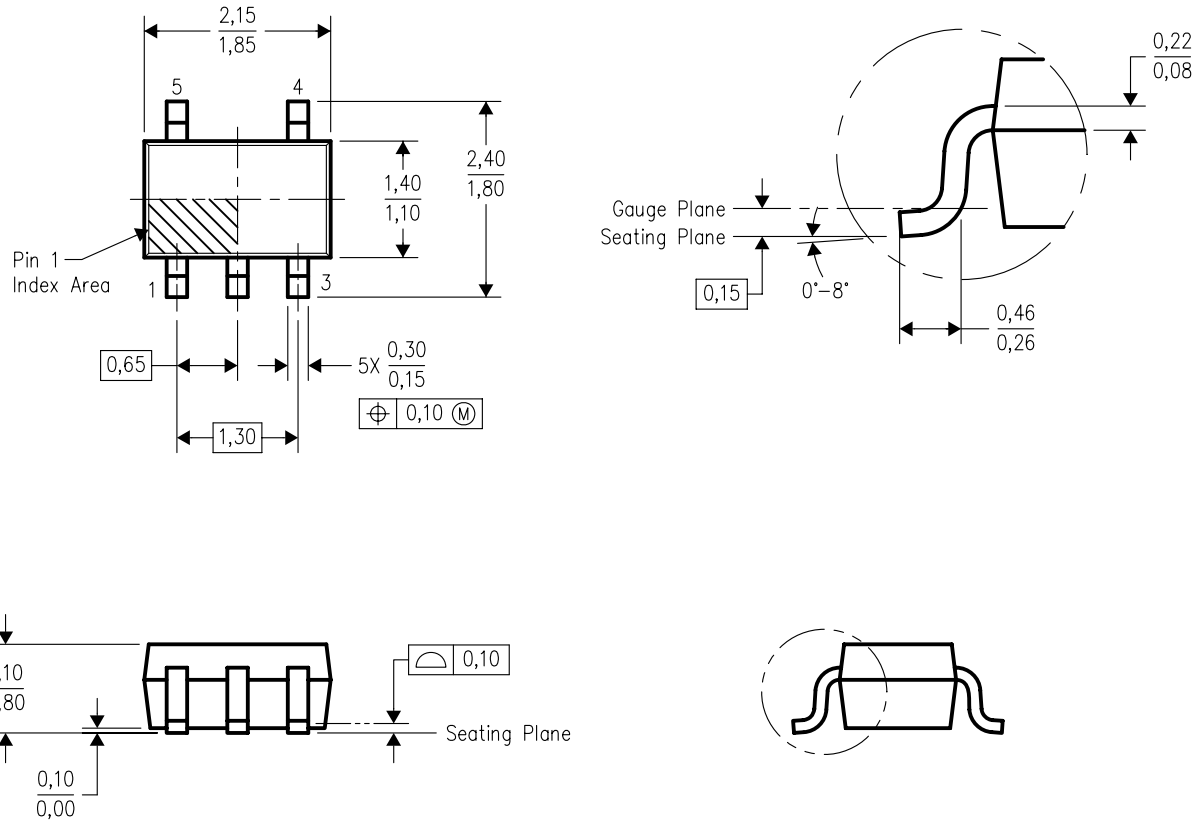
NOTE: All linear dimensions are in millimeters

DRG (S–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–SM–782 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

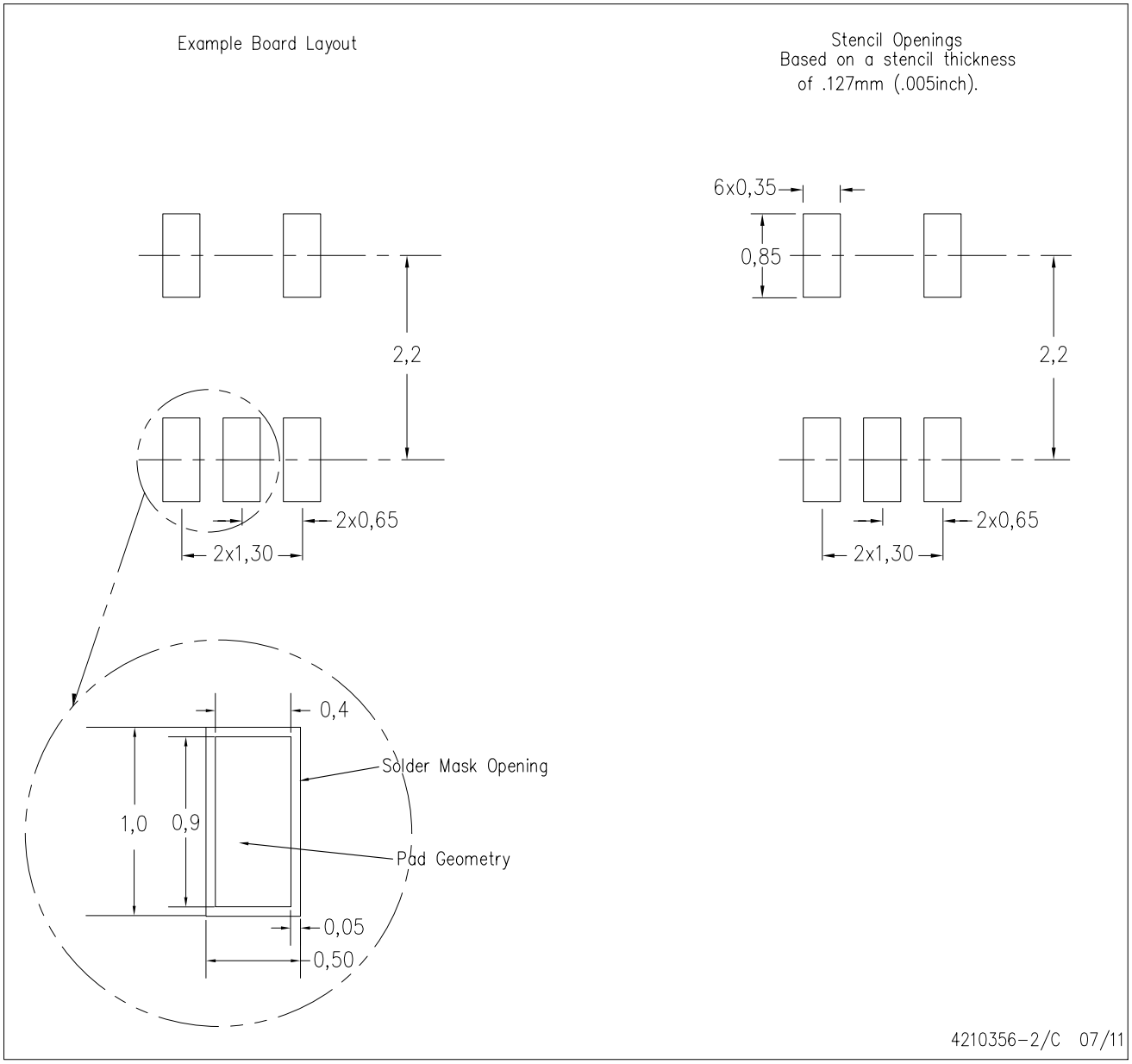
DCK (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



4093553–3/G 01/2007

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–203 variation AA.

DCK (R–PDSO–G5) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

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