DMN53D0L

N-CHANNEL ENHANCEMENT MODE FIELD EFFECT TRANSISTOR

NEW PRODUCT

Product Summary

$V_{(BR)DSS}$	$R_{DS(ON)}$	I_D T_A = +25°C
50V	1.6Ω @ V_{GS} = 10V	500 mA
	2.5Ω @ V_{GS} = 4.5V	200 mA

Features and Benefits

- N-Channel MOSFET
- Low On-Resistance
- Very Low Gate Threshold Voltage
- Low Input Capacitance
- Fast Switching Speed
- Low Input/Output Leakage
- ESD Protected to 2KV
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **Qualified to AEC-Q101 Standards for High Reliability**

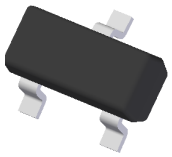
Description and Applications

This MOSFET has been designed to minimize the on-state resistance ($R_{DS(ON)}$) and yet maintain superior switching performance, making it ideal for high efficiency power management applications.

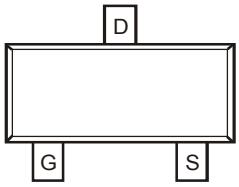
Mechanical Data

- Case: SOT23
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Matte Tin Finish annealed over Alloy 42 leadframe (Lead Free Plating). Solderable per MIL-STD-202, Method 208 e3
- Terminal Connections: See Diagram
- Weight: 0.008 grams (approximate)

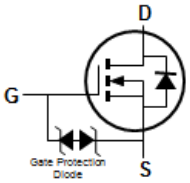
SOT23



Top View



Top View



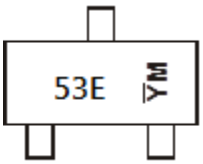
Equivalent Circuit

Ordering Information (Note 4)

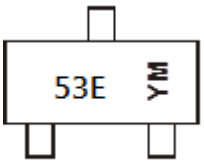
Part Number	Case	Packaging
DMN53D0L-7	SOT23	3000/Tape & Reel
DMN53D0L-13	SOT23	10000/Tape & Reel

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
2. See http://www.diodes.com/quality/lead_free.html for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. For packaging details, go to our website at http://www.diodes.com/products/packages.html.

Marking Information



Chengdu A/T Site



Shanghai A/T Site

53E = Product Type Marking Code
YM = Date Code Marking for SAT (Shanghai Assembly/ Test site)
$\overline{Y}\overline{M}$ = Date Code Marking for CAT (Chengdu Assembly/ Test site)
Y or $\overline{Y}$ = Year (ex: B = 2014)
M = Month (ex: 9 = September)

Date Code Key

Year	2014	2015	2016	2017	2018	2019	2020
Code	B	C	D	E	F	G	H

Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Code	1	2	3	4	5	6	7	8	9	O	N	D

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Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit
Drain Source Voltage	V_{DSS}	50	V
Gate-Source Voltage	V_{GSS}	±20	V
Drain Current (Note 6)	I_D	500	mA

Thermal Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit
Total Power Dissipation (Note 5)	P_D	370	mW
Thermal Resistance, Junction to Ambient (Note 5)	$R_{\theta JA}$	344	°C/W
Total Power Dissipation (Note 6)	P_D	540	mW
Thermal Resistance, Junction to Ambient (Note 6)	$R_{\theta JA}$	236	°C/W
Operating and Storage Temperature Range	T_J, T_{STG}	-55 to +150	°C

Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 7)						
Drain-Source Breakdown Voltage	BV_{DSS}	50	—	—	V	V_{GS} = 0V, I_D = 250μA
Zero Gate Voltage Drain Current	I_{DSS}	—	—	1.0	μA	V_{DS} = 50V, V_{GS} = 0V
Gate-Body Leakage	I_{GSS}	—	—	10	μA	V_{GS} = ±20V, V_{DS} = 0V
ON CHARACTERISTICS (Note 7)						
Gate Threshold Voltage	$V_{GS(th)}$	0.8	—	1.5	V	V_{DS} = V_{GS}, I_D = 250μA
Static Drain-Source On-Resistance	$R_{DS(ON)}$	— — —	— — —	1.6 2.5 4.5	Ω	V_{GS} = 10V, I_D = 500mA V_{GS} = 4.5V, I_D = 200mA V_{GS} = 2.5V, I_D = 100mA
Source-Drain Diode Forward Voltage	V_{SD}	—	—	1.4	V	V_{GS} = 0V, I_S = 500mA
DYNAMIC CHARACTERISTICS (Note 8)						
Input Capacitance	C_{iss}	—	46	—	pF	V_{DS} = 25V, V_{GS} = 0V f = 1.0MHz
Output Capacitance	C_{oss}	—	5.3	—	pF	
Reverse Transfer Capacitance	C_{rss}	—	4.0	—	pF	
Total Gate Charge	Q_g	—	0.6	—	nC	V_{GS} = 4.5V, V_{DS} = 10V, I_D = 250mA
Gate-Source Charge	Q_{gs}	—	0.2	—	nC	
Gate-Drain Charge	Q_{gd}	—	0.1	—	nC	
Turn-On Delay Time	$t_{D(on)}$	—	2.7	—	ns	V_{DD} = 30V, V_{GS} = 10V, R_G = 25Ω, I_D = 200mA
Turn-On Rise Time	t_r	—	2.5	—	ns	
Turn-Off Delay Time	$t_{D(off)}$	—	19	—	ns	
Turn-Off Fall Time	t_f	—	11	—	ns	

Notes:
5. Device mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout
6. Device mounted on FR-4 substrate PC board, 2oz copper, with thermal vias to bottom layer 1inch square copper plate
7. Short duration pulse test used to minimize self-heating effect.
8. Guaranteed by design. Not subject to product testing.

NEW PRODUCT

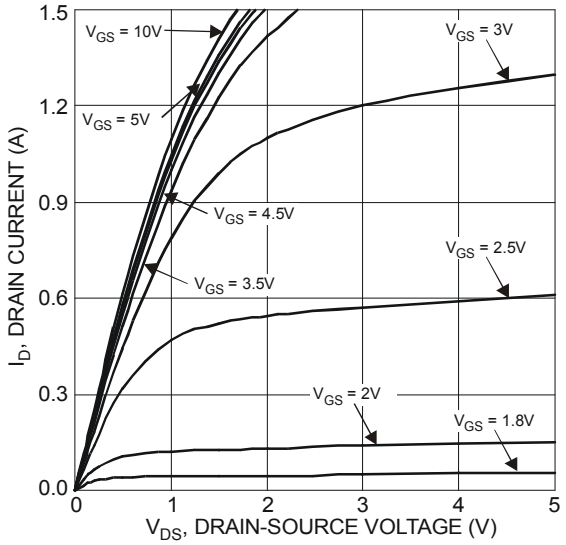

Figure 1 Typical Output Characteristics

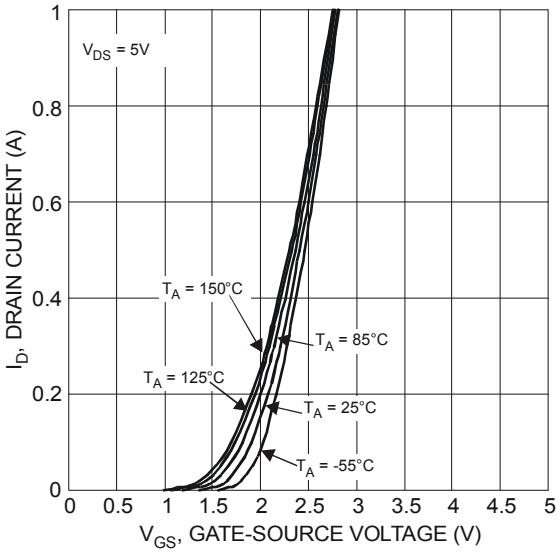

Figure 2 Typical Transfer Characteristics

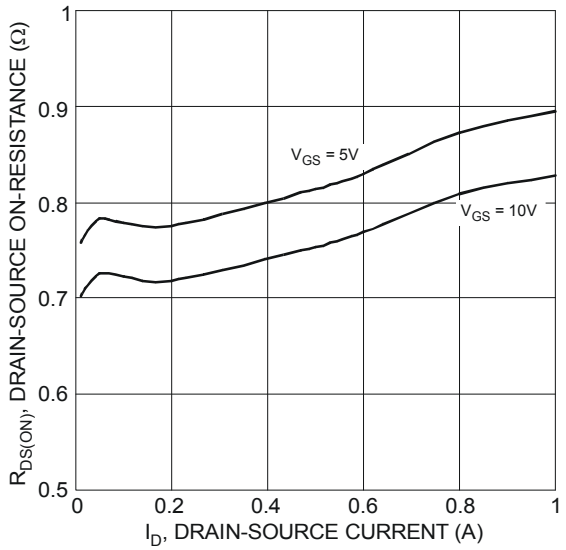

Figure 3 Typical On-Resistance vs. Drain Current and Gate Voltage

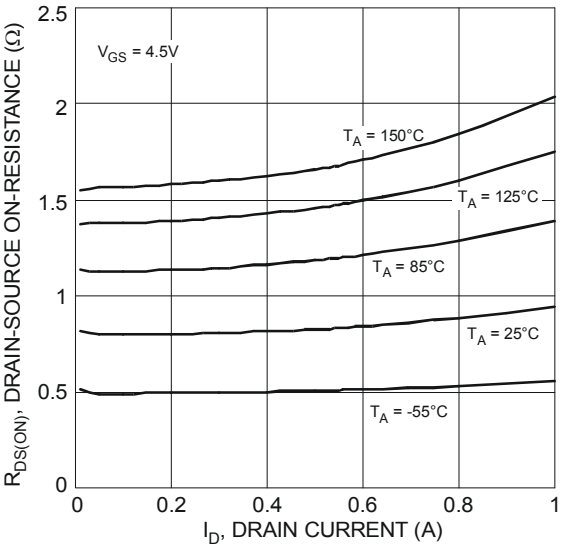

Figure 4 Typical On-Resistance vs. Drain Current and Temperature

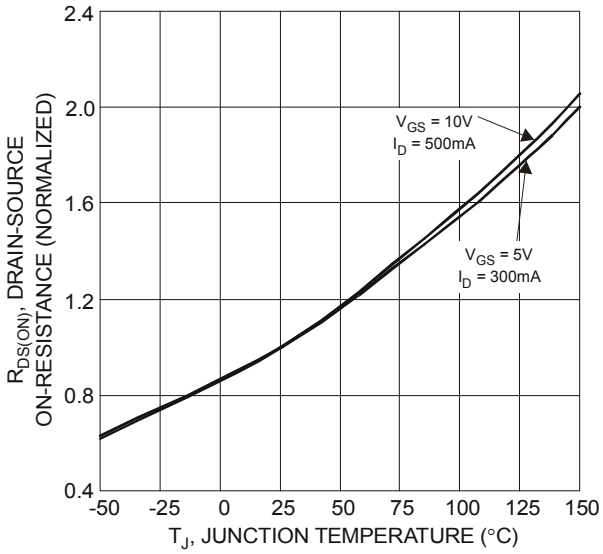

Figure 5 On-Resistance Variation with Temperature

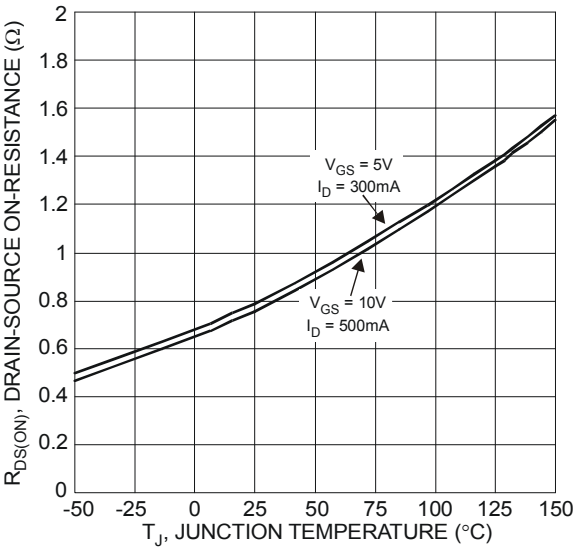

Figure 6 On-Resistance Variation with Temperature

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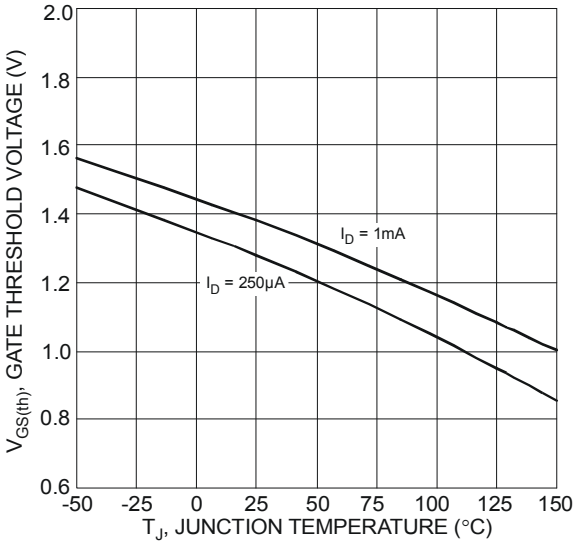


Figure 7 Gate Threshold Variation vs. Ambient Temperature

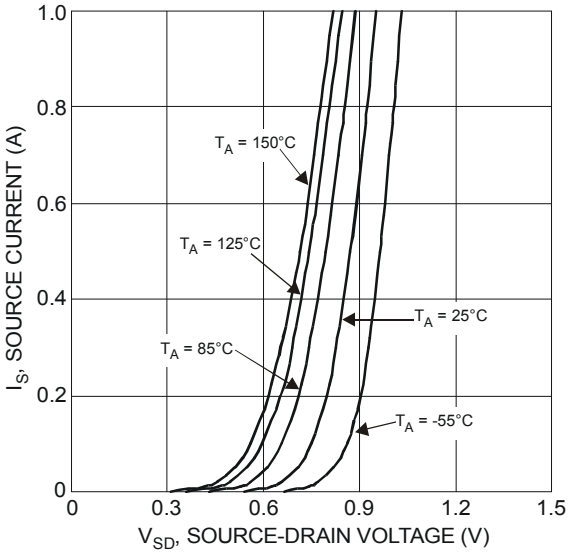


Figure 8 Diode Forward Voltage vs. Current

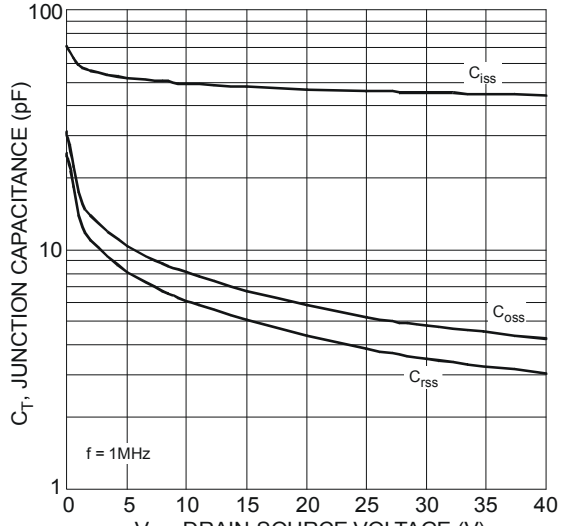


Figure 9 Typical Junction Capacitance

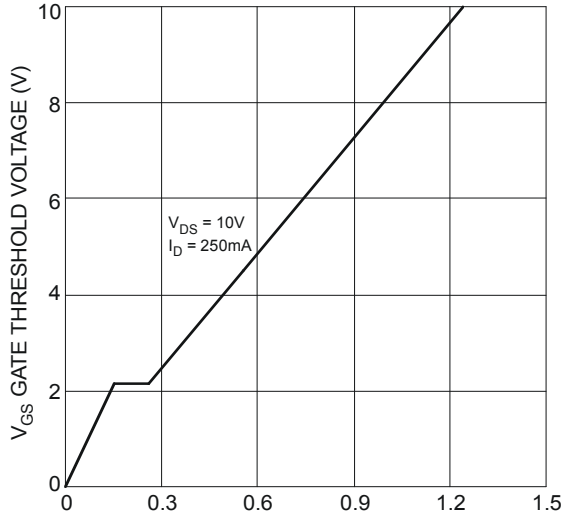
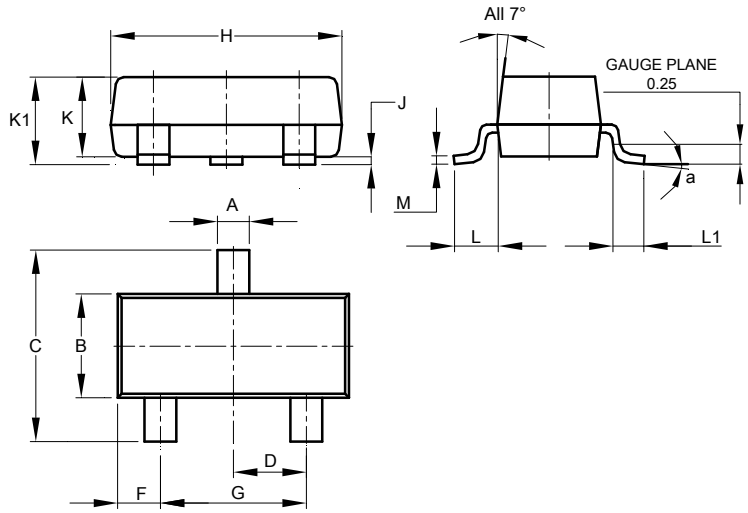


Figure 10 Gate Charge

Package Outline Dimensions

Please see AP02002 at http://www.diodes.com/datasheets/ap02002.pdf for latest version.

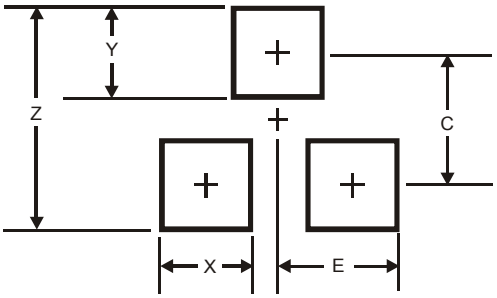


SOT23			
Dim	**Min**	**Max**	**Typ**
A	0.37	0.51	0.40
B	1.20	1.40	1.30
C	2.30	2.50	2.40
D	0.89	1.03	0.915
F	0.45	0.60	0.535
G	1.78	2.05	1.83
H	2.80	3.00	2.90
J	0.013	0.10	0.05
K	0.890	1.00	0.975
K1	0.903	1.10	1.025
L	0.45	0.61	0.55
L1	0.25	0.55	0.40
M	0.085	0.150	0.110
α	8°		
All Dimensions in mm			

NEW PRODUCT

Suggested Pad Layout

Please see AP02001 at http://www.diodes.com/datasheets/ap02001.pdf for the latest version.



Dimensions	Value (in mm)
Z	2.9
X	0.8
Y	0.9
C	2.0
E	1.35