

## 3-Pin Voltage Supervisors with Active-Low, Open-Drain Reset

 Check for Samples: [TLV803M](#), [TLV803R](#), [TLV803S](#), [TLV803Z](#)

### FEATURES

- 3-Pin SOT23 Package
- Supply Current: 9  $\mu$ A (Typical)
- Precision Supply Voltage Monitor: 2.5 V, 3 V, 3.3 V, 5 V
- Power-On Reset Generator with Fixed Delay Time of 200 ms
- Pin-for-Pin Compatible with MAX803
- Temperature Range:  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Open-Drain,  $\overline{\text{RESET}}$  Output

### APPLICATIONS

- DSPs, Microcontrollers, and Microprocessors
- Wireless Communication Systems
- Portable/Battery-Powered Equipment
- Programmable Controls
- Intelligent Instruments
- Industrial Equipment
- Notebook and Desktop Computers
- Automotive Systems

### DESCRIPTION

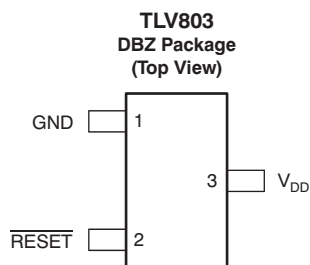
The TLV803 family of supervisory circuits provides circuit initialization and timing supervision, primarily for DSPs and processor-based systems.

During power-on,  $\overline{\text{RESET}}$  asserts when the supply voltage ( $V_{\text{DD}}$ ) becomes greater than 1.1 V. Thereafter, the supervisory circuit monitors  $V_{\text{DD}}$  and keeps  $\overline{\text{RESET}}$  active as long as  $V_{\text{DD}}$  remains below the threshold voltage  $V_{\text{IT}}$ . An internal timer delays the return of the output to the inactive state (high) to ensure proper system reset. The delay time ( $t_{\text{d(typ)}}$ ) = 200 ms) starts after  $V_{\text{DD}}$  has risen above the threshold voltage,  $V_{\text{IT}}$ . When the supply voltage drops below the  $V_{\text{IT}}$  threshold voltage, the output becomes active (low) again. All the devices in this family have a fixed sense-threshold voltage ( $V_{\text{IT}}$ ) set by an internal voltage divider.

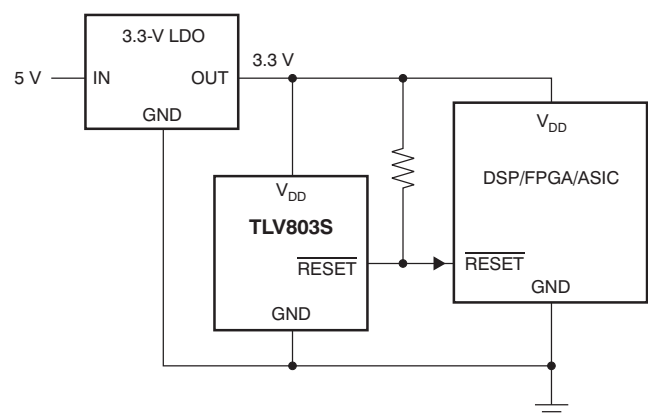
The product spectrum is designed for supply voltages of 2.5 V, 3 V, 3.3 V, and 5 V. The circuits are available in a 3-pin SOT-23 package. The TLV803 devices are characterized for operation over a temperature range of  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ .

### DEVICE FAMILY COMPARISON

DEVICE	FUNCTION
TLV803	Open-Drain, $\overline{\text{RESET}}$ Output
TLV809	Push-Pull, $\overline{\text{RESET}}$ Output
TLV810	Push-Pull, $\overline{\text{RESET}}$ Output



### TYPICAL APPLICATION



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### PACKAGE/ORDERING INFORMATION<sup>(1)</sup>

PRODUCT	THRESHOLD VOLTAGE	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED OPERATING TEMPERATURE	PACKAGE MARKING	ORDERING INFORMATION	TRANSPORT MEDIA, QUANTITY
TLV803Z	2.25 V	SOT23-3	DBZ	-40°C TO +125°C	VORQ	TLV803ZDBZR	Tape and Reel, 3000
						TLV803ZDBZT	Tape and Reel, 250
TLV803R	2.64 V	SOT23-3	DBZ	-40°C TO +125°C	VOSQ	TLV803RDBZR	Tape and Reel, 3000
						TLV803RDBZT	Tape and Reel, 250
TLV803S	2.93 V	SOT23-3	DBZ	-40°C TO +125°C	VOTQ	TLV803SDBZR	Tape and Reel, 3000
						TLV803SDBZT	Tape and Reel, 250
TLV803M	4.38 V	SOT23-3	DBZ	-40°C TO +125°C	VOUQ	TLV803MDBZR	Tape and Reel, 3000
						TLV803MDBZT	Tape and Reel, 250

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this data sheet, or visit the device product folder at [www.ti.com](http://www.ti.com).

### ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Over operating free-air temperature range (unless otherwise noted) .

		VALUE		UNIT
		MIN	MAX	
Voltage	$V_{DD}$ <sup>(2)</sup>	0	7	V
	All other pins <sup>(2)</sup>	-0.3	7	V
Current	Maximum low output current, $I_{OL}$		5	mA
	Maximum high output current, $I_{OH}$		-5	mA
	Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{DD}$ )		±20	mA
	Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{DD}$ )		±20	mA
Temperature	Operating free-air temperature range, $T_A$	-40	+125	°C
	Storage temperature range, $T_{stg}$	-65	+150	°C
	Soldering temperature		+260	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to GND. For reliable operation the device should not be operated at 7 V for more than  $t = 1000$ h continuously

### THERMAL INFORMATION

THERMAL METRIC <sup>(1)</sup>		TLV803	UNITS
		DBZ	
		3 PINS	
$\theta_{JA}$	Junction-to-ambient thermal resistance	286.9	°C/W
$\theta_{JCTop}$	Junction-to-case (top) thermal resistance	105.6	
$\theta_{JB}$	Junction-to-board thermal resistance	124.4	
$\psi_{JT}$	Junction-to-top characterization parameter	25.8	
$\psi_{JB}$	Junction-to-board characterization parameter	107.9	
$\theta_{JCbott}$	Junction-to-case (bottom) thermal resistance	—	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](http://www.ti.com).

## RECOMMENDED OPERATING CONDITIONS

At specified temperature range (unless otherwise noted).

		MIN	MAX	UNIT
$V_{DD}$	Supply voltage	1.1	6	V
$T_A$	Operating free-air temperature range	-40	+125	°C

## ELECTRICAL CHARACTERISTICS

Over recommended operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	
$V_{OL}$	Low-level output voltage	$V_{DD} = 2\text{ V to }6\text{ V}, I_{OL} = 500\text{ }\mu\text{A}$			0.2	V	
		$V_{DD} = 3.3\text{ V}, I_{OL} = 2\text{ mA}$			0.4		
		$V_{DD} = 6\text{ V}, I_{OL} = 4\text{ mA}$			0.4		
Power-up reset voltage <sup>(1)</sup>		$I_{OL} = 50\text{ }\mu\text{A}, V_{OL} < 0.2\text{ V}$	1.1			V	
$V_{IT-}$	Negative-going input threshold voltage <sup>(2)</sup>	$T_A = -40^\circ\text{C to }125^\circ\text{C}$	TLV803Z	2.20	2.25	2.30	V
			TLV803R	2.58	2.64	2.70	
			TLV803S	2.87	2.93	2.99	
			TLV803M	4.28	4.38	4.48	
$V_{hys}$	Hysteresis	$T_A = +25^\circ\text{C}, I_{OL} = 50\text{ }\mu\text{A}$	TLV803Z		30		mV
			TLV803R		35		
			TLV803S		40		
			TLV803M		60		
$I_{DD}$	Supply current	$V_{DD} = 2\text{ V}, \text{ output unconnected}$		9	15	$\mu\text{A}$	
		$V_{DD} = 6\text{ V}, \text{ output unconnected}$		20	30		
$I_{OH}$	Output leakage current	$V_{DD} = 6\text{ V}$			100	nA	

(1) The lowest supply voltage at which  $\overline{\text{RESET}}$  becomes valid.  $t_r, V_{DD} \leq 66.7\text{ V/ms}$ .

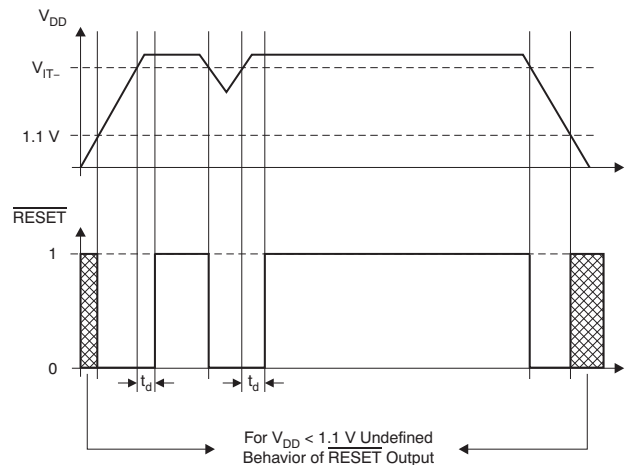
(2) To ensure best stability of the threshold voltage, a bypass capacitor (0.1- $\mu\text{F}$  ceramic) should be placed near the supply terminals.

## SWITCHING CHARACTERISTICS

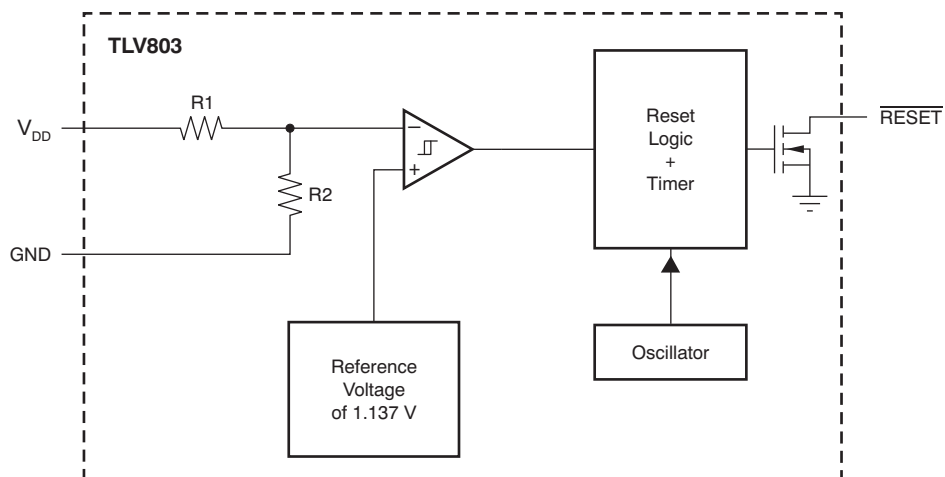
At  $T_A = +25^\circ\text{C}$ , unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
$t_w$	Pulse duration at $V_{DD}$		1		$\mu\text{s}$	
$t_d$	Delay time	$V_{DD} \geq V_{IT-} + 0.2\text{ V}$ ; see <a href="#">Timing Diagram</a>	120	200	280	ms

## TIMING DIAGRAM



## FUNCTIONAL BLOCK DIAGRAM



### TYPICAL CHARACTERISTICS

At  $T_A = +25^\circ\text{C}$ ,  $V_{IT-} = 4.38\text{ V}$ , and  $V_{DD} = 5.0\text{ V}$ , unless otherwise noted.

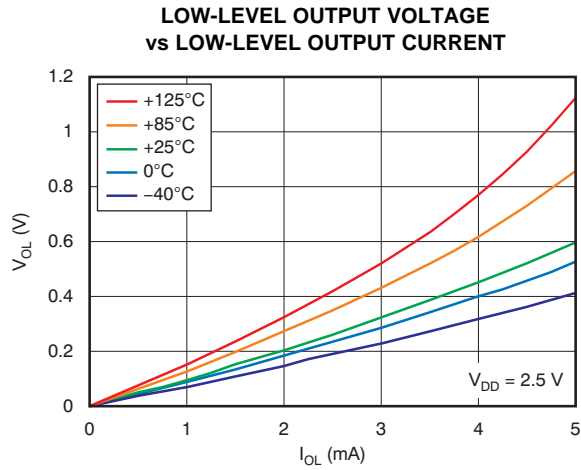


Figure 1.

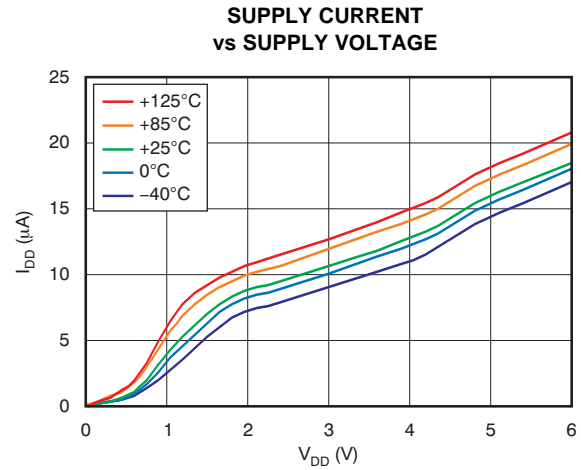


Figure 2.

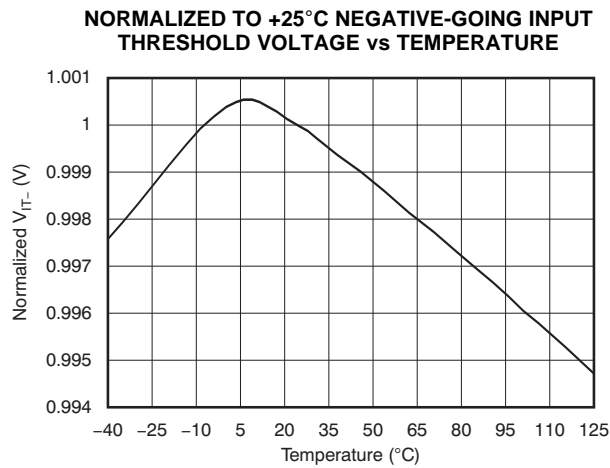


Figure 3.

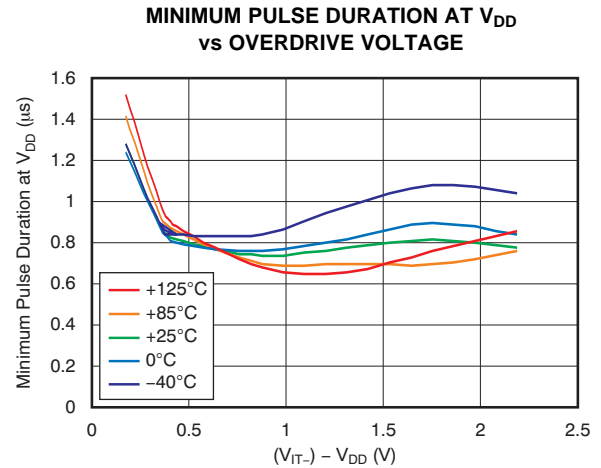


Figure 4.

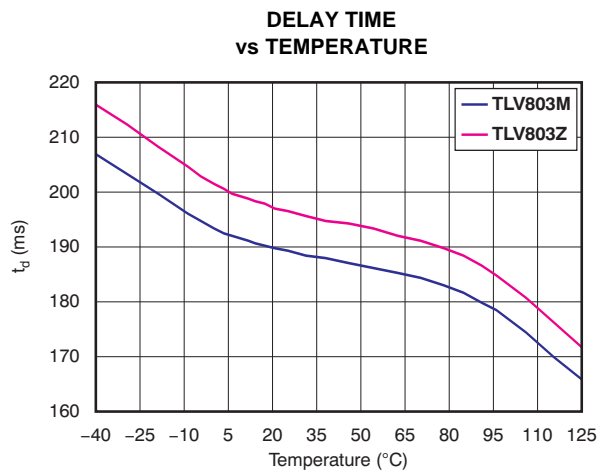


Figure 5.

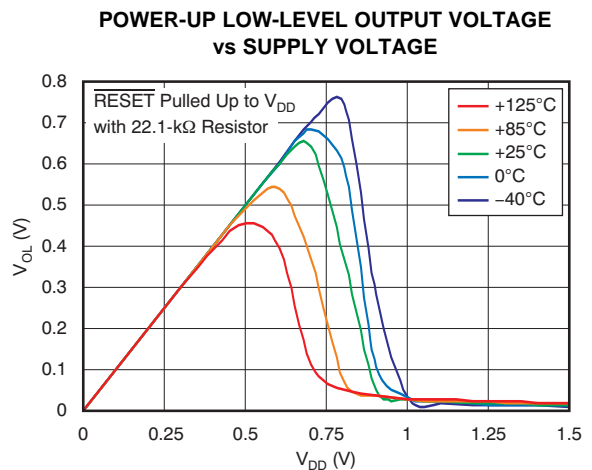


Figure 6.

## APPLICATION INFORMATION

### V<sub>DD</sub> TRANSIENT REJECTION

The TLV803 has built-in rejection of fast transients on the V<sub>DD</sub> pin. The rejection of transients depends on both the duration and the amplitude of the transient. The amplitude of the transient is measured from the bottom of the transient to the negative threshold voltage of the TLV803, as shown in Figure 7.

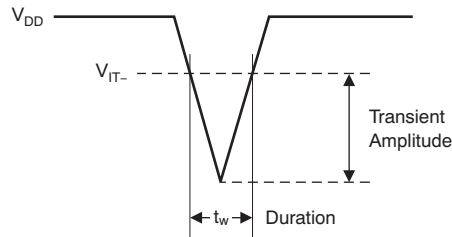


Figure 7. Voltage Transient Measurement

The TLV803 does not respond to transients that are fast duration/low amplitude or long duration/small amplitude. Figure 4 shows the relationship between the transient amplitude and duration needed to trigger a reset. Any combination of duration and amplitude above the curve generates a reset signal.

### RESET DURING POWER UP/DOWN

The TLV803 output is valid when V<sub>DD</sub> is greater than 1.1 V. When V<sub>DD</sub> is less than 1.1 V, the output transistor turns off and becomes high impedance. The voltage on the RESET pin rises to the voltage level connected to the pull-up resistor. Figure 8 shows a typical waveform for power-up, assuming the RESET pin has a pull-up resistor connected to the V<sub>DD</sub> pin.

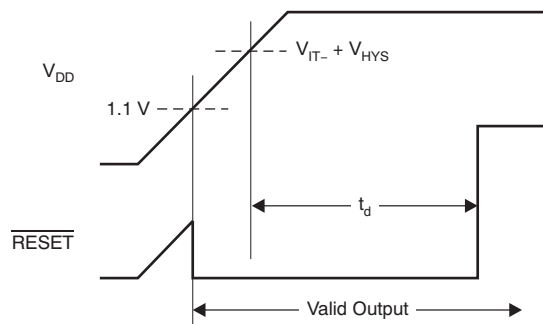


Figure 8. Power-Up Response

## MONITORING MULTIPLE SUPPLIES

Because the TLV803 has an open-drain output, multiple TLV803 outputs can be directly tied together to form a logical OR-ing function for the  $\overline{\text{RESET}}$  line. Only one pull-up resistor is required for this configuration. Figure 9 shows two TLV803s connected together to provide monitoring of a 3.3-V power rail and a 5.0-V power rail. A reset is generated if either power rail falls below the threshold voltage of its corresponding TLV803.

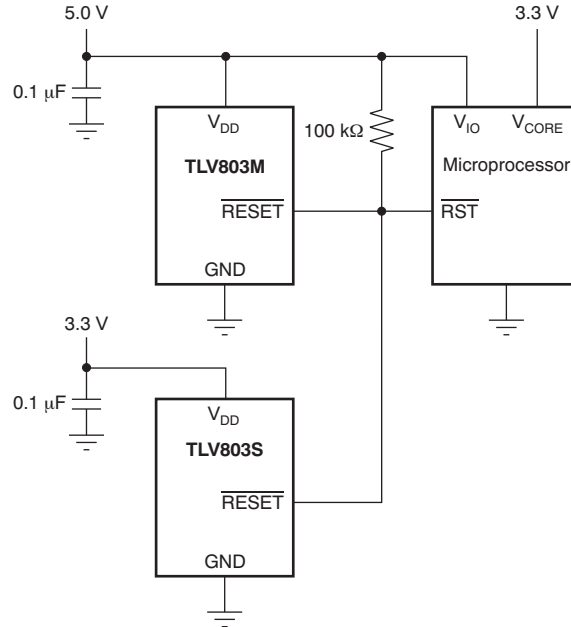


Figure 9. Multiple Voltage Rail Monitoring

## BIDIRECTIONAL RESET PINS

Some microcontrollers have bidirectional reset pins that act as both inputs and outputs. In a situation where the TLV803 is pulling the  $\overline{\text{RESET}}$  line low while the microcontroller is trying to force the  $\overline{\text{RESET}}$  line high, a series resistor should be placed between the output of the TLV803 and the  $\overline{\text{RESET}}$  pin of the microcontroller to protect against excessive current flow. Figure 10 shows the connection of the TLV803 to a microcontroller using a series resistor to drive a bidirectional  $\overline{\text{RESET}}$  line.

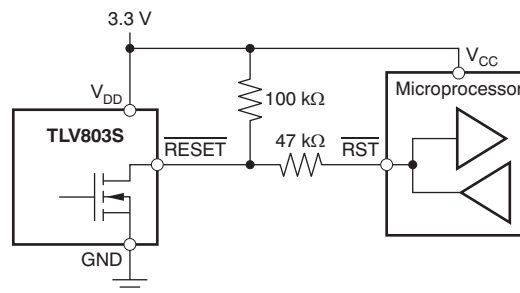


Figure 10. Connection to Bidirectional Reset Pin

## OUTPUT LEVEL SHIFTING

The  $\overline{\text{RESET}}$  output of the TLV803 can be pulled to a maximum voltage of 6 V and can be pulled higher in voltage than  $V_{\text{DD}}$ . It is useful to provide level shifting of the output for cases where the monitored voltage is less than the useful logic levels of the load. Figure 11 shows the TLV803Z used to monitor a 2.5-V power rail, with a logic  $\overline{\text{RESET}}$  input to a microprocessor that is connected to 5.0 V and has 5.0-V logic levels.

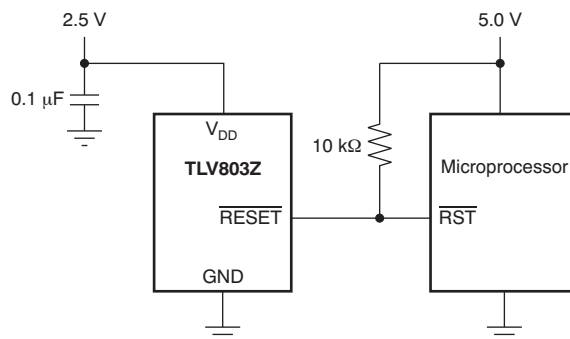


Figure 11. Output Voltage Level Shifting



**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TLV803MDBZR	ACTIVE	SOT-23	DBZ	3	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	VOUQ	<a href="#">Samples</a>
TLV803MDBZT	ACTIVE	SOT-23	DBZ	3	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	VOUQ	<a href="#">Samples</a>
TLV803RDBZR	ACTIVE	SOT-23	DBZ	3	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	VOSQ	<a href="#">Samples</a>
TLV803RDBZT	ACTIVE	SOT-23	DBZ	3	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	VOSQ	<a href="#">Samples</a>
TLV803SDBZR	ACTIVE	SOT-23	DBZ	3	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	VOTQ	<a href="#">Samples</a>
TLV803SDBZT	ACTIVE	SOT-23	DBZ	3	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	VOTQ	<a href="#">Samples</a>
TLV803ZDBZR	ACTIVE	SOT-23	DBZ	3	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	VORQ	<a href="#">Samples</a>
TLV803ZDBZT	ACTIVE	SOT-23	DBZ	3	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	VORQ	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

<sup>(4)</sup> Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV803MDBZR	SOT-23	DBZ	3	3000	179.0	8.4	3.15	2.95	1.22	4.0	8.0	Q3
TLV803MDBZT	SOT-23	DBZ	3	250	179.0	8.4	3.15	2.95	1.22	4.0	8.0	Q3
TLV803RDBZR	SOT-23	DBZ	3	3000	179.0	8.4	3.15	2.95	1.22	4.0	8.0	Q3
TLV803RDBZT	SOT-23	DBZ	3	250	179.0	8.4	3.15	2.95	1.22	4.0	8.0	Q3
TLV803SDBZR	SOT-23	DBZ	3	3000	179.0	8.4	3.15	2.95	1.22	4.0	8.0	Q3
TLV803SDBZT	SOT-23	DBZ	3	250	179.0	8.4	3.15	2.95	1.22	4.0	8.0	Q3
TLV803ZDBZR	SOT-23	DBZ	3	3000	179.0	8.4	3.15	2.95	1.22	4.0	8.0	Q3
TLV803ZDBZT	SOT-23	DBZ	3	250	179.0	8.4	3.15	2.95	1.22	4.0	8.0	Q3

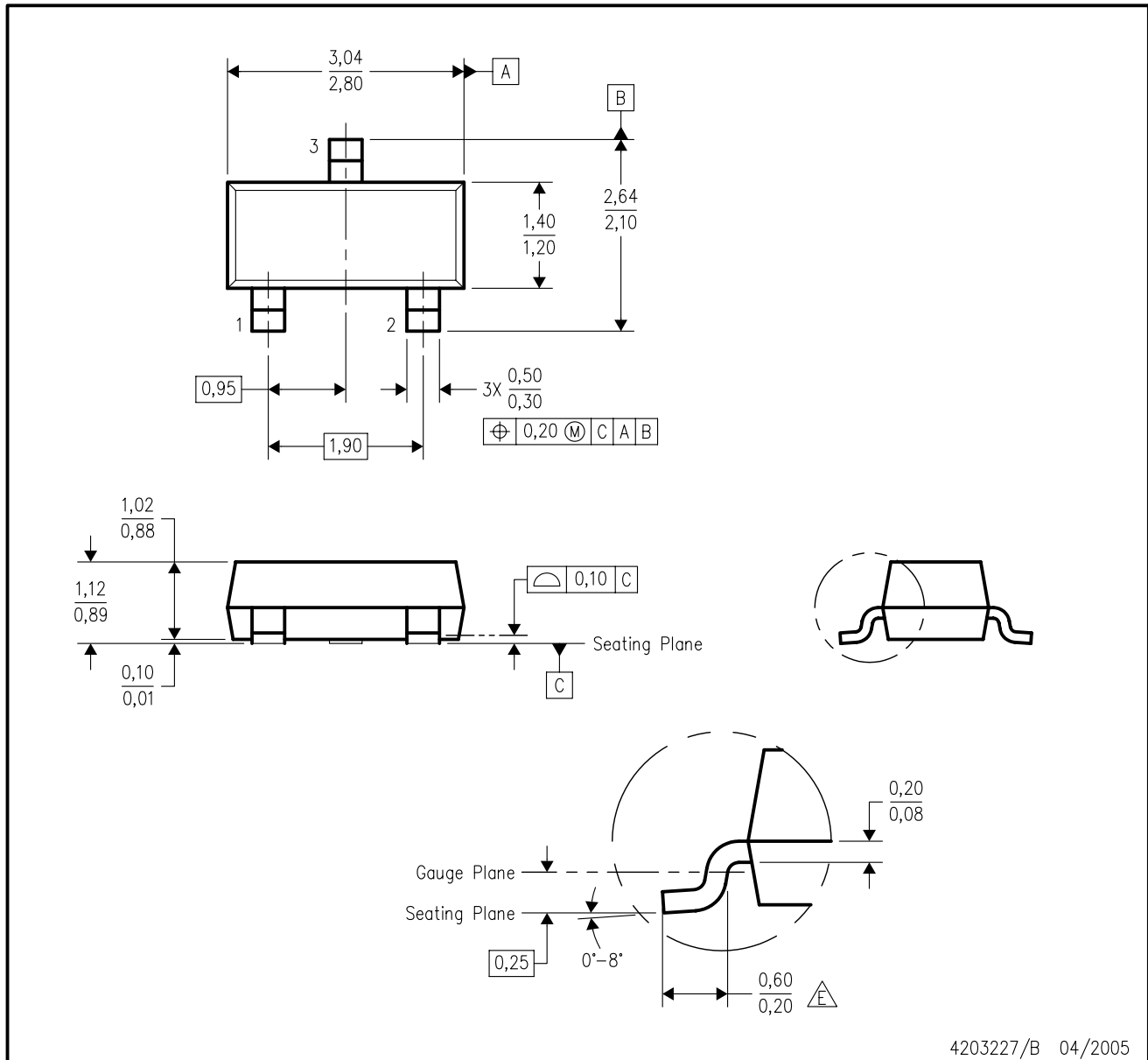
**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV803MDBZR	SOT-23	DBZ	3	3000	203.0	203.0	35.0
TLV803MDBZT	SOT-23	DBZ	3	250	203.0	203.0	35.0
TLV803RDBZR	SOT-23	DBZ	3	3000	203.0	203.0	35.0
TLV803RDBZT	SOT-23	DBZ	3	250	203.0	203.0	35.0
TLV803SDBZR	SOT-23	DBZ	3	3000	203.0	203.0	35.0
TLV803SDBZT	SOT-23	DBZ	3	250	203.0	203.0	35.0
TLV803ZDBZR	SOT-23	DBZ	3	3000	203.0	203.0	35.0
TLV803ZDBZT	SOT-23	DBZ	3	250	203.0	203.0	35.0

DBZ (R-PDSO-G3)

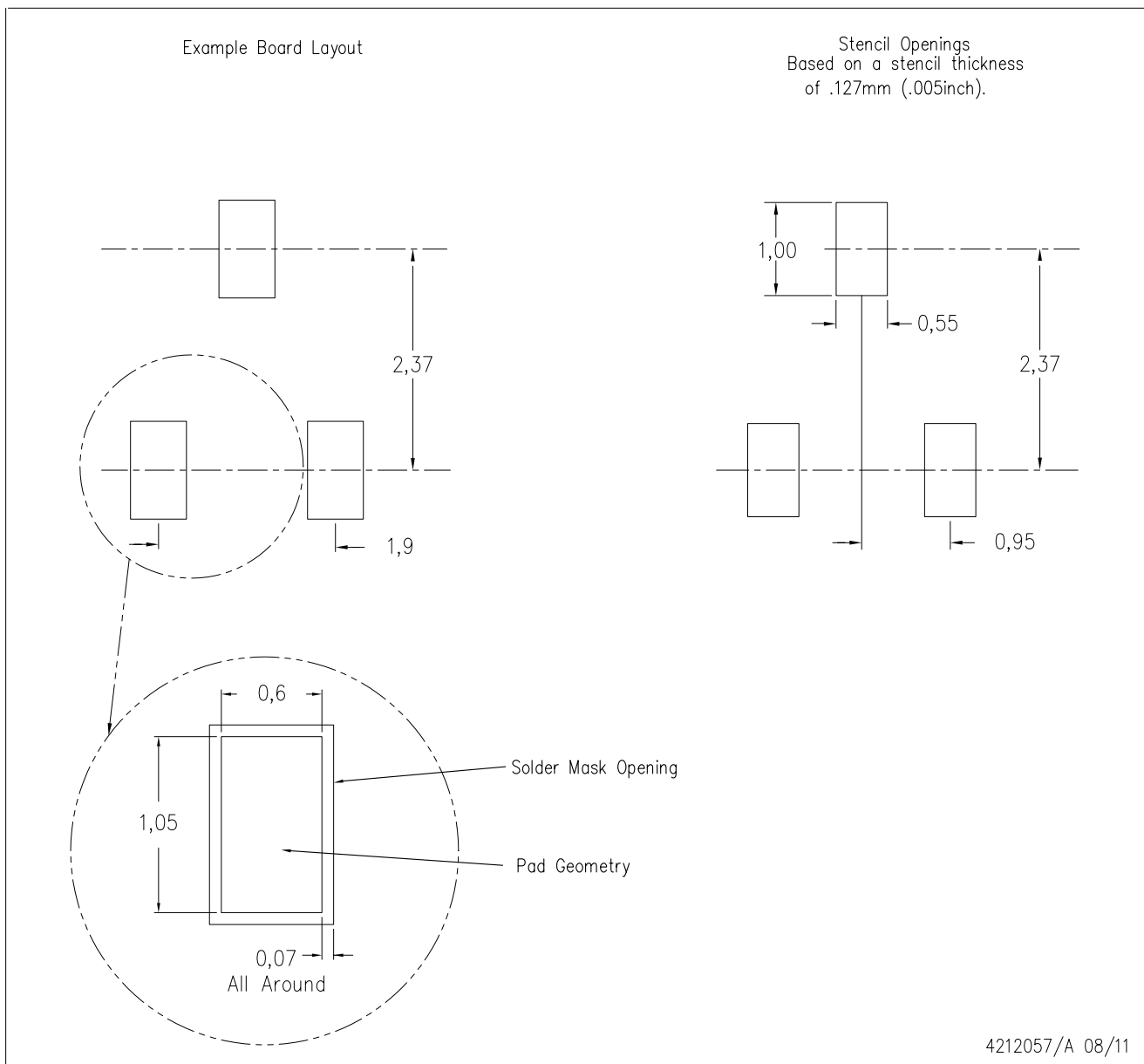
PLASTIC SMALL-OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Lead dimensions are inclusive of plating.
  - D. Body dimensions are exclusive of mold flash and protrusion. Mold flash and protrusion not to exceed 0.25 per side.
  - $\triangle E$  Falls within JEDEC TO-236 variation AB, except minimum foot length.

DBZ (R-PDSO-G3)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
  - D. Publication IPC-7351 is recommended for alternate designs.
  - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

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No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

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