25-06694

SY58606U

4.25Gbps Precision, 1:2 CML Fanout Buffer with Internal Termination and Fail Safe Input

General Description

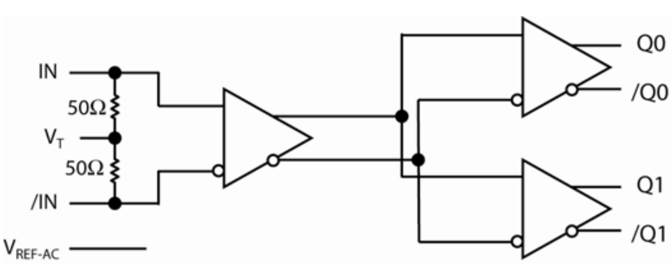
The SY58606U is a 2.5/3.3V, high-speed, fully differential 1:2 CML fanout buffer optimized to provide two identical output copies with less than 15ps of skew and less than $10ps_{pp}$ total jitter. The SY58606U can process clock signals as fast as 3GHz or data patterns up to 4.25Gbps.

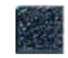
The differential input includes Micrel's unique, 3-pin input termination architecture that interfaces to LVPECL, LVDS or CML differential signals, (AC- or DC-coupled) as small as 100mV ($200mV_{pp}$) without any level-shifting or termination resistor networks in the signal path. For AC-coupled input interface applications, an integrated voltage reference ($V_{REF\text{-}AC}$) is provided to bias the V_T pin. The outputs are 400mV CML, with extremely fast rise/fall times guaranteed to be less than 85ps.

The SY58606U operates from a 2.5V ±5% supply or 3.3V ±10% supply and is guaranteed over the full industrial temperature range (–40°C to +85°C). For applications that require LVPECL or LVDS outputs, consider Micrel's SY58607U and SY58608U, 1:2 fanout buffers with 800mV and 325mV output swings respectively. The SY58606U is part of Micrel's high-speed, Precision Edge® product line.

Data sheets and support documentation can be found on Micrel's web site at: www.micrel.com.

Functional Block Diagram





Precision Edge®

Features

- Precision 1:2, 400mV CML fanout buffer
- Guaranteed AC performance over temperature and voltage:
  - DC-to > 4.25Gbps throughput
  - <320ps propagation delay (IN-to-Q)
  - <15ps within-device skew
  - <85ps rise/fall times
- Fail Safe Input
  - Prevents outputs from oscillating when input is invalid
- Ultra-low jitter design
  - $<1ps_{RMS}$ cycle-to-cycle jitter
  - $<10ps_{PP}$ total jitter
  - $<1ps_{RMS}$ random jitter
  - $<10ps_{PP}$ deterministic jitter
- High-speed CML outputs
- 2.5V ±5% or 3.3V ±10% power supply operation
- Industrial temperature range: –40°C to +85°C
- Available in 16-pin (3mm x 3mm) MLF® package

Applications

- Data Distribution: OC-48, OC-48+FEC, XAUI
- SONET clock and data distribution
- Fibre Channel clock and data distribution
- Gigabit Ethernet clock and data distribution

Markets

- Storage
- ATE
- Test and measurement
- Enterprise networking equipment
- High-end servers
- Access
- Metro area network equipment

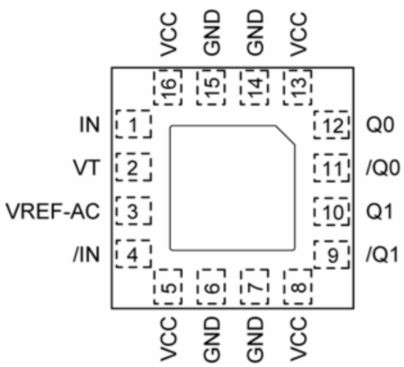
Ordering Information[1]

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY58606UMG	MLF-16	Industrial	606U with Pb-Free bar-line indicator	NiPdAu Pb-Free
SY58606UMGTR[2]	MLF-16	Industrial	606U with Pb-Free bar-line indicator	NiPdAu Pb-Free

Notes:

1. Contact factory for die availability. Dice are guaranteed at T_A = 25°C, DC Electricals only.
2. Tape and Reel.

Pin Configuration



16-Pin MLF® (MLF-16)

Pin Description

Pin Number	Pin Name	Pin Function
1, 4	IN, /IN	Differential Input: This input pair is the differential signal input to the device. Input accepts DC-coupled differential signals as small as 100mV (200mV$_{PP}$). Each pin of this pair internally terminates with 50Ω to the VT pin. If the input swing falls below a certain threshold (typical 30mV), the Fail Safe Input (FSI) feature will guarantee a stable output by latching the output to its last valid state. See “Input Interface Applications” subsection.
2	VT	Input Termination Center-Tap: Each side of the differential input pair terminates to VT pin. This pin provides a center-tap to a termination network for maximum interface flexibility. See “Input Interface Applications” subsection.
3	VREF-AC	Reference Voltage: This output biases to V_{CC}–1.2V. It is used for AC-coupling inputs IN and /IN. Connect VREF-AC directly to the VT pin. Bypass with 0.01µF low ESR capacitor to VCC. Maximum sink/source current is ±1.5mA. See “Input Interface Applications” subsection.
5, 8,13, 16	VCC	Positive Power Supply: Bypass with 0.1uF//0.01uF low ESR capacitors as close to the V_{CC} pins as possible.
6, 7, 14, 15	GND, Exposed pad	Ground: Exposed pad must be connected to a ground plane that is the same potential as the ground pins.
9, 10 11, 12	/Q1, Q1 /Q0, Q0	CML Differential Output Pairs: Differential buffered copies of the input signal. The output swing is typically 400mV. Unused output pair may be left floating with no impact on jitter. See “CML Output Termination” subsection.

Absolute Maximum Ratings[1]

Supply Voltage (V_{CC}) .... –0.5V to +4.0V
Input Voltage (V_{IN}) .... –0.5V to V_{CC}
CML Output Voltage (V_{OUT}) .... V_{CC}-1.0V to V_{CC}+0.5V
Current (V_T)
  Source or sink on VT pin .... ±100mA
Input Current
  Source or sink Current on (IN, /IN) .... ±50mA
Current (V_{REF})
  Source or sink current on V_{REF-AC}[4] .... ±1.5mA
Maximum operating Junction Temperature .... 125°C
Lead Temperature (soldering, 20sec.) .... 260°C
Storage Temperature (T_s) .... –65°C to +150°C

Operating Ratings[2]

Supply Voltage (V_{IN}) .... +2.375V to +3.60V
Ambient Temperature (T_A) .... –40°C to +85°C
Package Thermal Resistance[3]
  MLF®
    Still-air (θ_{JA}) .... 60°C/W
    Junction-to-board (ψ_{JB}) .... 33°C/W

DC Electrical Characteristics[5]

T_A = –40°C to +85°C, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{CC}	Power Supply Voltage Range		2.375 3.0	2.5 3.3	2.625 3.6	V
I_{CC}	Power Supply Current	No load, max. V_{CC}		60	77	mA
R_{DIFF_IN}	Differential Input Resistance (IN-to-/IN)		90	100	110	Ω
V_{IH}	Input HIGH Voltage (IN, /IN)	IN, /IN	1.2		V_{CC}	V
V_{IL}	Input LOW Voltage (IN, /IN)	IN, /IN	0		V_{IH}–0.1	V
V_{IN}	Input Voltage Swing (IN, /IN)	see Figure 3a, Note 6	0.1		1.7	V
V_{DIFF_IN}	Differential Input Voltage Swing (|IN - /IN|)	see Figure 3b	0.2			V
V_{IN_FSI}	Input Voltage Threshold that Triggers FSI			30	100	mV
V_{REF-AC}	Output Reference Voltage		V_{CC}–1.3	V_{CC}–1.2	V_{CC}–1.1	V
V_{T_IN}	Voltage from Input to V_T				1.28	V

Notes:

1. Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.
2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
3. Package thermal resistance assumes exposed pad is soldered (or equivalent) to the device's most negative potential on the PCB. ψ_{JB} and θ_{JA} values are determined for a 4-layer board in still-air number, unless otherwise stated.
4. Due to the limited drive capability, use for input of the same package only.
5. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.
6. V_{IN}(max) is specified when V_T is floating.

CML Outputs DC Electrical Characteristics[7]

V_{CC} = +2.5V ±5% or +3.3V ±10%, R_L = 100Ω across the outputs; T_A = –40°C to +85°C, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{OH}	Output HIGH Voltage	R_L = 50Ω to V_{CC}	V_{CC}-0.020	V_{CC}-0.010	V_{CC}	V
V_{OUT}	Output Voltage Swing	See Figure 3a	325	400		mV
V_{DIFF_OUT}	Differential Output Voltage Swing	See Figure 3b	650	800		mV
R_{OUT}	Output Source Impedance		45	50	55	Ω

Note:

7. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

AC Electrical Characteristics

V_{CC} = +2.5V ±5% or +3.3V ±10%, R_L = 100Ω across the outputs, Input t_r/t_f: ≤300ps; T_A = –40°C to +85°C, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{MAX}	Maximum Frequency	NRZ Data	4.25			Gbps
		V_{OUT} > 200mV Clock	2.5	3.0		GHz
t_{PD}	Propagation Delay IN-to-Q	V_{IN}: 100mV-200mV	150	270	400	ps
		V_{IN}: 200mV-800mV	120	220	320	ps
t_{Skew}	Within Device Skew	Note 8		3	15	ps
	Part-to-Part Skew	Note 9			100	ps
t_{Jitter}	Data Random Jitter	Note 10			1	ps_{RMS}
	Deterministic Jitter	Note 11			10	ps_{PP}
	Clock Cycle-to-Cycle Jitter	Note 12			1	ps_{RMS}
	Total Jitter	Note 13			10	ps_{PP}
t_R t_F	Output Rise/Fall Times (20% to 80%)	At full output swing.	30	50	85	ps
	Duty Cycle	Differential I/O	47		53	%

Notes:

8. Within device skew is measured between two different outputs under identical input transitions.
9. Part-to-part skew is defined for two parts with identical power supply voltages at the same temperature and no skew at the edges at the respective inputs.
10. Random jitter is measured with a K28.7 pattern, measured at ≤ f_{MAX}.
11. Deterministic jitter is measured at 2.5Gbps with both K28.5 and 2^{23}–1 PRBS pattern.
12. Cycle-to-cycle jitter definition: the variation period between adjacent cycles over a random sample of adjacent cycle pairs. $t_{JITTER\_CC} = T_n - T_{n+1}$, where T is the time between rising edges of the output signal.
13. Total jitter definition: with an ideal clock input frequency of ≤ f_{MAX} (device), no more than one output edge in 10^{12} output edges will deviate by more than the specified peak-to-peak jitter value.

Functional Description

Fail-Safe Input (FSI)

The input includes a special failsafe circuit to sense the amplitude of the input signal and to latch the outputs when there is no input signal present, or when the amplitude of the input signal drops sufficiently below $100mV_{PK}$ ($200mV_{PP}$), typically $30mV_{PK}$. Maximum frequency of SY58606U is limited by the FSI function.

Input Clock Failure Case

If the input clock fails to a floating, static, or extremely low signal swing, then the FSI function will eliminate a metastable condition and guarantee a stable output. No ringing and no undetermined state will occur at the output under these conditions.

Note that the FSI function will not prevent duty cycle distortion in case of a slowly deteriorating (but still toggling) input signal. Due to the FSI function, the propagation delay will depend on rise and fall time of the input signal and on its amplitude. Refer to "Typical Characteristics" for detailed information.

Timing Diagrams

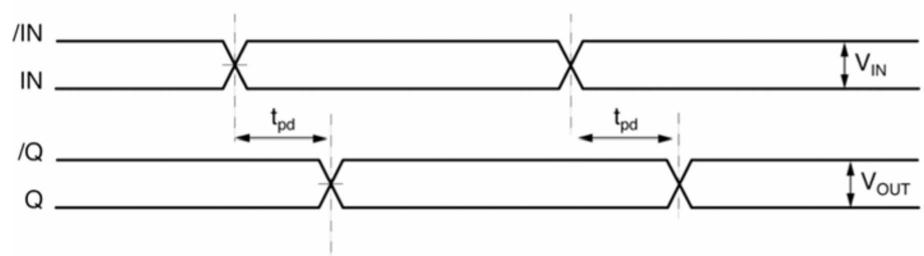


Figure 1a. Propagation Delay

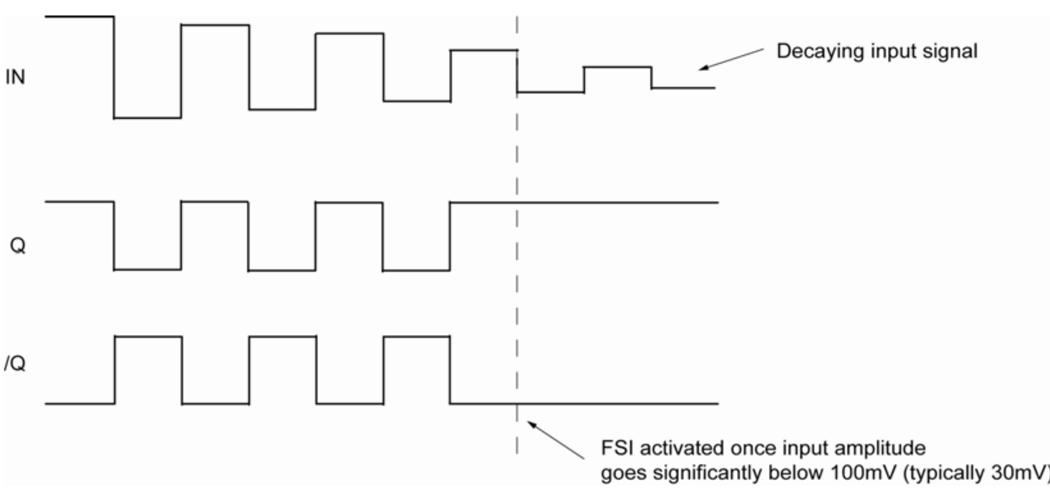
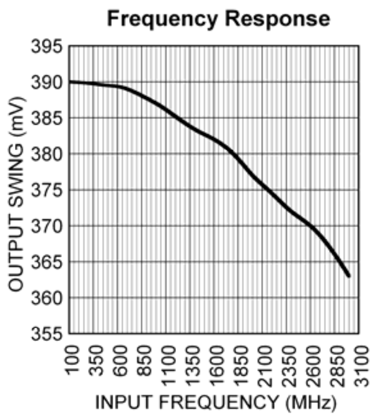
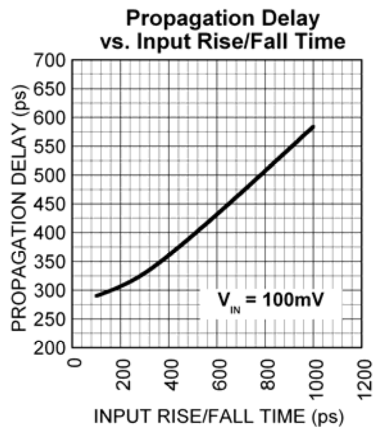


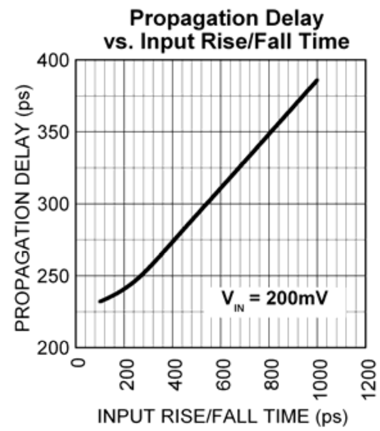
Figure 1b. Fail Safe Feature

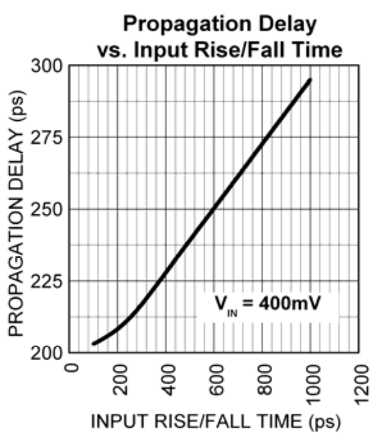
Typical Characteristics

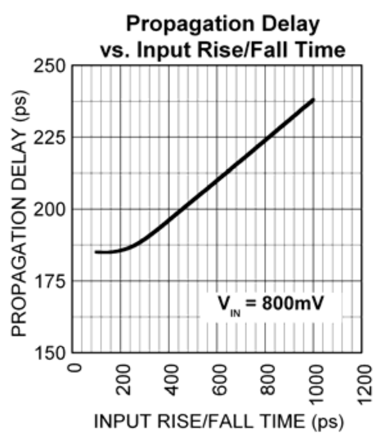
V_{CC} = 3.3V, GND = 0V, V_{IN} = 100mV, R_L = 100Ω across the outputs, T_A = 25°C, unless otherwise stated.





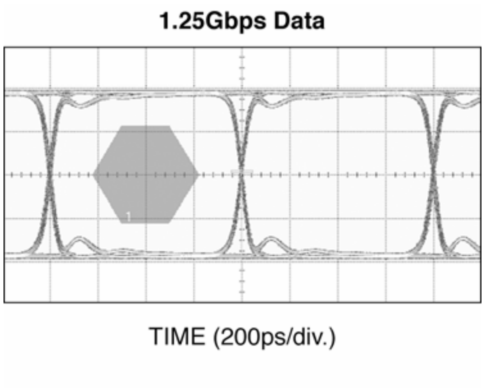


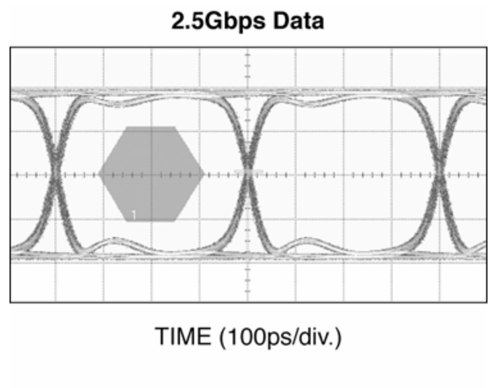


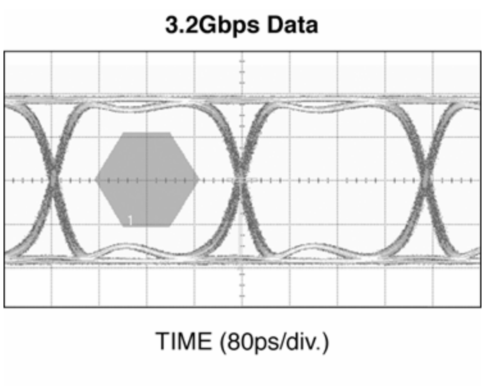


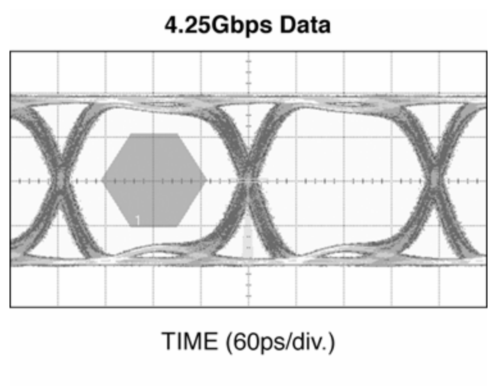
Functional Characteristics

V_{CC} = 2.5V, GND = 0V, V_{IN} = 325mV, Data Pattern: 2^{23}-1, R_L = 100Ω across the outputs, T_A = 25°C, unless otherwise stated.



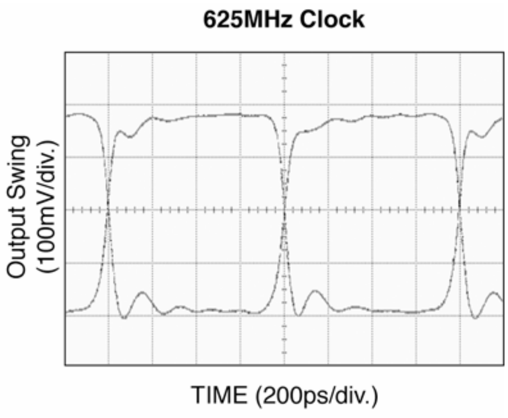


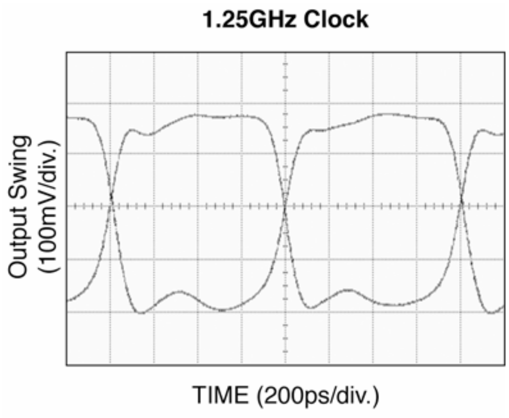


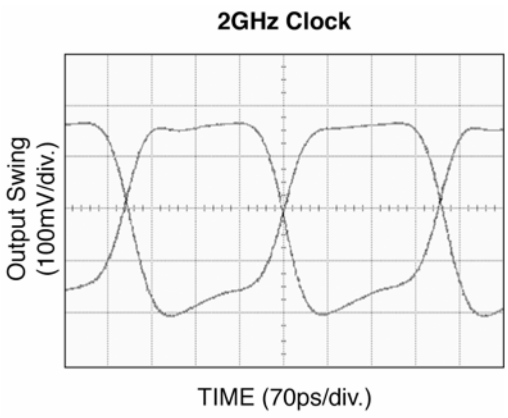


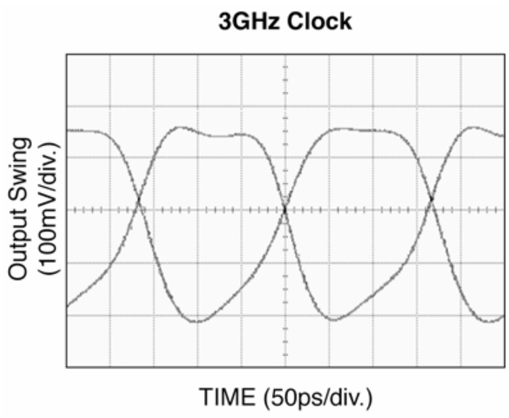
Functional Characteristics (continued)

V_{CC} = 2.5V, GND = 0V, V_{IN} = 325mV, R_L = 100Ω across the outputs, T_A = 25°C, unless otherwise stated.









Input and Output Stage

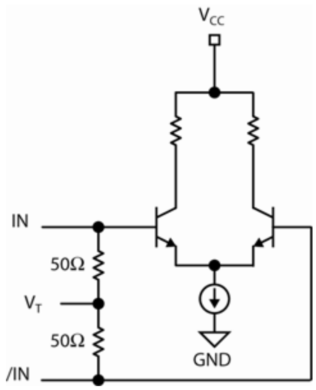


Figure 2a. Simplified Differential Input Buffer

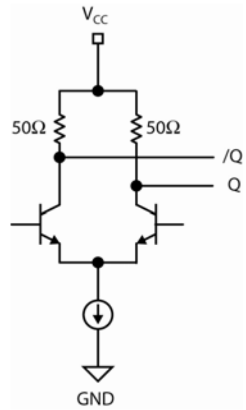


Figure 2b. Simplified CML Output Buffer

Single-Ended and Differential Swings

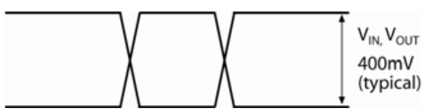


Figure 3a. Single-Ended Swing

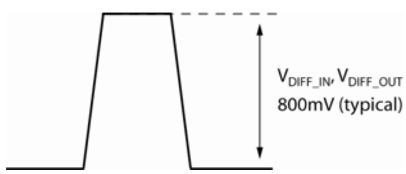


Figure 3b. Differential Swing

Input Interface Applications

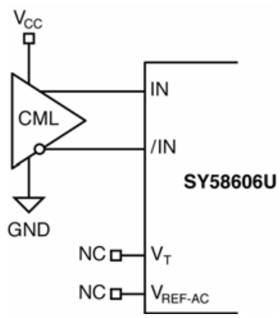


Figure 4a. CML Interface (DC-Coupled)

Option: May connect V_T to V_{CC}

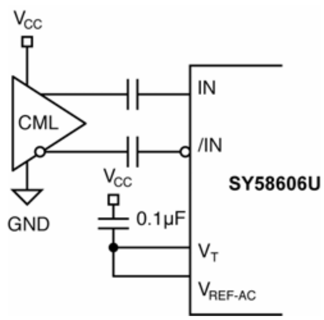


Figure 4b. CML Interface (AC-Coupled)

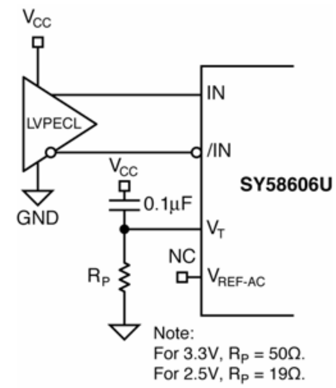


Figure 4c. LVPECL Interface (DC-Coupled)

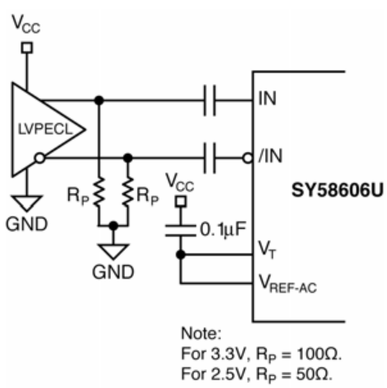


Figure 4d. LVPECL Interface (AC-Coupled)

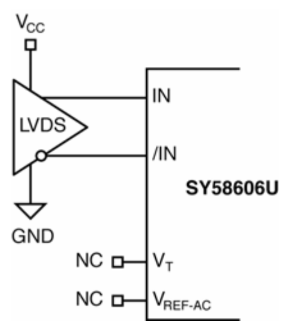


Figure 4e. LVDS Interface

hbwhelp@micrel.com or (408) 955-1690

CML Output Termination

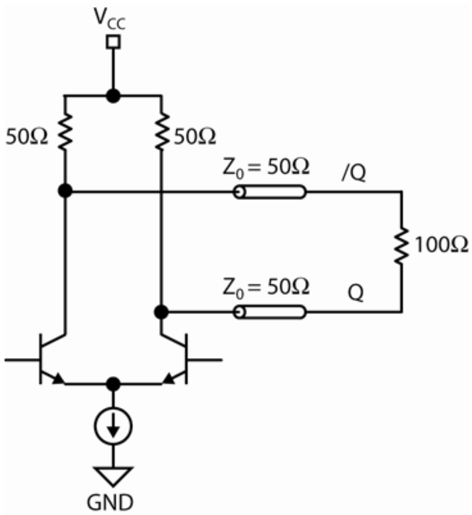


Figure 5a. CML DC-Coupled Termination

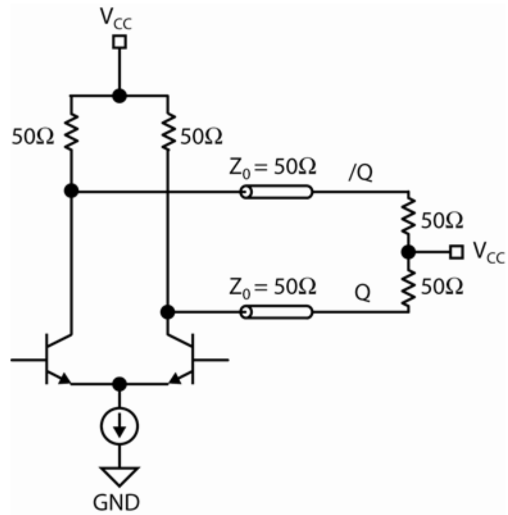


Figure 5b. CML DC-Coupled Termination

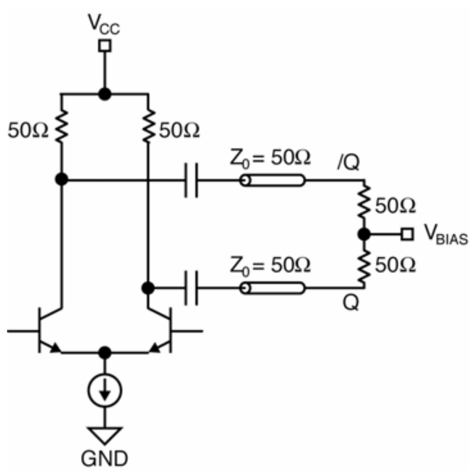
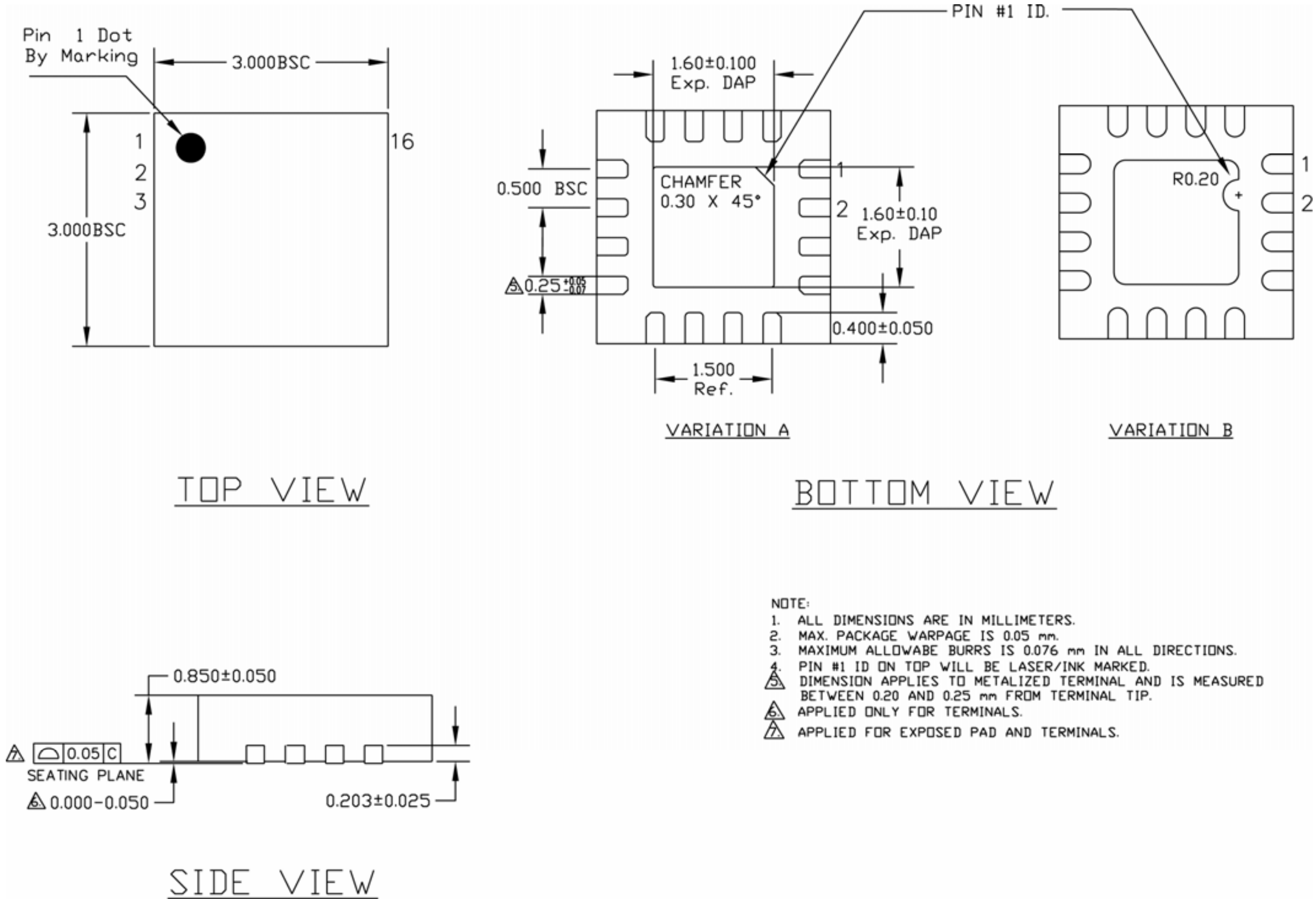


Figure 5c. CML AC-Coupled Termination

Related Product and Support Documents

Part Number	Function	Data Sheet Link
SY58607U	3.2Gbps Precision, 1:2 LVPECL Fanout Buffer with Internal Termination and Fail Safe Input	http://www.micrel.com/page.do?page=/product-info/products/sy58607u.shtml
SY58608U	3.2Gbps Precision, 1:2 LVDS Fanout Buffer with Internal Termination and Fail Safe Input	http://www.micrel.com/page.do?page=/product-info/products/sy58608u.shtml
HBW Solutions	New Products and Termination Application Notes	http://www.micrel.com/page.do?page=/product-info/as/HBWsolutions.shtml

Package Information



16-Pin MLF® (3mm x3mm) (MLF-16)

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