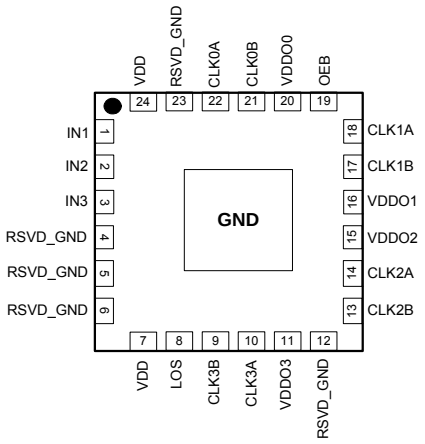
1.8/2.5/3.3 V Low-Jitter, Low-Skew Clock Buffer/Level Translator

Features

- Supports single-ended or differential input clock signals
- Generates four differential (LVPECL, LVDS, HCSL) or eight single-ended (CMOS, SSTL, HSTL) outputs
- Provides signal level translation
  - Differential to single-ended
  - Single-ended to differential
  - Differential to differential
  - Single-ended to single-ended
- Wide frequency range
  - LVPECL, LVDS: 5 to 710 MHz
  - HCSL: 5 to 250 MHz
  - SSTL, HSTL: 5 to 350 MHz
  - CMOS: 5 to 200 MHz
- Additive jitter: 150 fs RMS typ
- Output-output skew: 100 ps
- Propagation delay: 2.5 ns typ
- Single core supply with excellent PSRR: 1.8, 2.5, or 3.3 V
- Output driver supply voltage independent of core supply: 1.5, 1.8, 2.5, or 3.3 V
- Loss of Signal (LOS) indicator allows system clock monitoring
- Output Enable (OEB) pin allows glitchless control of output clocks
- Low power: 10 mA typical core current
- Industrial temperature range: –40 to +85 °C
- Small size: 24-lead, 4 x 4 mm QFN

Ordering Information:
See page 14.

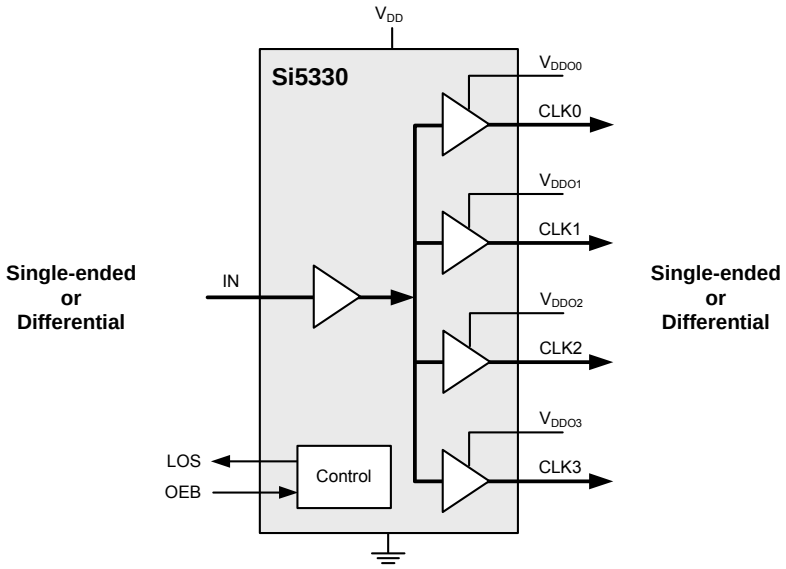
Pin Assignments



Applications

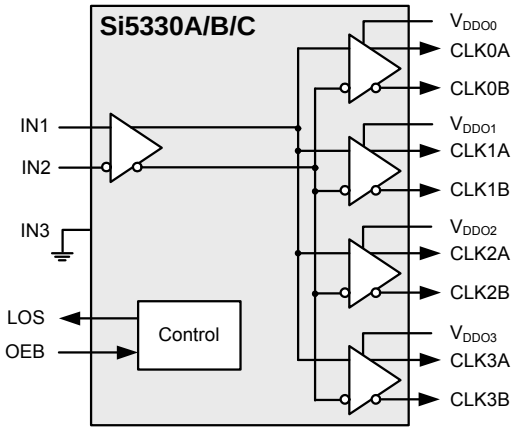
- High Speed Clock Distribution
- Ethernet Switch/Router
- SONET / SDH
- PCI Express 2.0/3.0
- Fibre Channel
- MSAN/DSLAM/PON
- Telecom Line Cards

Functional Block Diagram

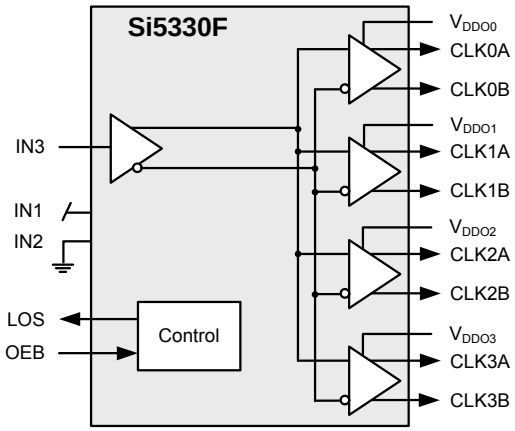


Functional Block Diagrams Based on Orderable Part Number*

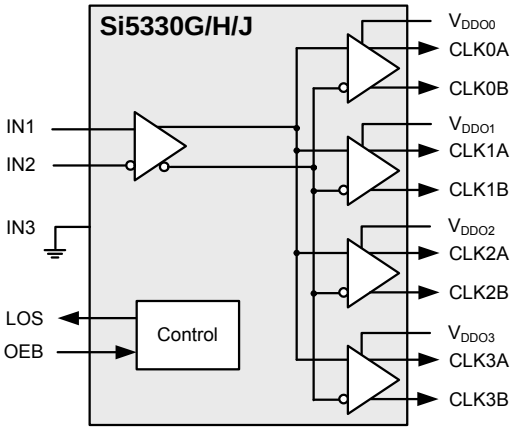
1:4 Differential to Differential Buffer



1:8 Single-Ended to Single-Ended Buffer



1:8 Differential to Single-Ended Buffer



1:4 Single-Ended to Differential Buffer

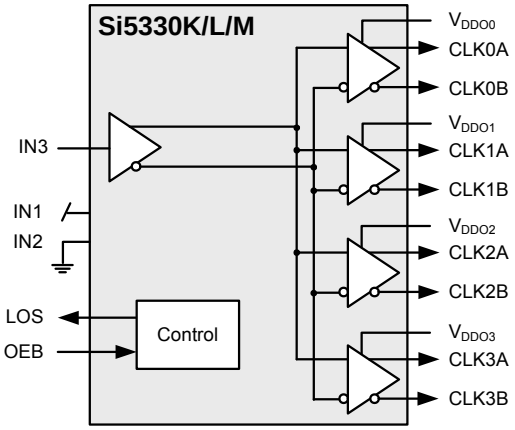


Figure 1. Si5330 Functional Block Diagrams

***Note:** See Table 11 for detailed ordering information.

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Section **Page**

1. Electrical Specifications

Table 1. Recommended Operating Conditions

(V_{DD} = 1.8 V –5% to +10%, 2.5 V ±10%, or 3.3 V ±10%, T_A = –40 to 85°C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Ambient Temperature	T_A		–40	25	85	°C
Core Supply Voltage	V_{DD}		2.97	3.3	3.63	V
			2.25	2.5	2.75	V
			1.71	1.8	1.98	V
Output Buffer Supply Voltage	V_{DDOn}		1.4	—	3.63	V

Note: All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at nominal supply voltages and an operating temperature of 25 °C unless otherwise noted.

Table 2. DC Characteristics

(V_{DD} = 1.8 V –5% to +10%, 2.5 V ±10%, or 3.3 V ±10%, T_A = –40 to 85°C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Core Supply Current	I_{DD}	50 MHz refclk	—	10	—	mA
Output Buffer Supply Current	I_{DDOx}	LVPECL, 710 MHz	—	—	30	mA
		LVDS, 710 MHz	—	—	8	mA
		HCSL, 250 MHz 2 pF load capacitance	—	—	20	mA
		SSTL, 350 MHz	—	—	19	mA
		CMOS, 50 MHz 15 pF load capacitance	—	—	28	mA
		CMOS, 200 MHz 2 pF load capacitance	—	—	28	mA
		HSTL, 350 MHz	—	—	19	mA

Table 3. Performance Characteristics

(V_{DD} = 1.8 V –5% to +10%, 2.5 V ±10%, or 3.3 V ±10%, T_A = –40 to 85°C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
CLKIN Loss of Signal Assert Time	t_{LOS}		—	2.6	5	µs
CLKIN Loss of Signal De-Assert Time	t_{LOS_B}	After initial start-up time has expired	0.01	0.2	1	µs
Input-to-Output Propagation Delay	t_{PROP}		—	2.5	4.0	ns
Output-Output Skew	t_{DSKEW}	Outputs at same signal format	—	—	100	ps
POR to Output Clock Valid	t_{START}	Start-up time for output clocks	—	—	2	ms

Table 4. Input and Output Clock Characteristics

(V_{DD} = 1.8 V –5% to +10%, 2.5 V ±10%, or 3.3 V ±10%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Input Clock (AC Coupled Differential Input Clocks on Pin IN1/2)						
Frequency	f_{IN}		5	—	710	MHz
Differential Voltage Swing	V_{PP}	710 MHz input	0.4	—	2.4	V_{PP}
Rise/Fall Time	t_R/t_F	20%–80%	—	—	1.0	ns
Duty Cycle	DC	< 1 ns tr/tf	40	50	60	%
Input Impedance	R_{IN}		10	—	—	kΩ
Input Capacitance	C_{IN}		—	3.5	—	pF
Input Clock (DC-Coupled Single-Ended Input Clock on Pin IN3)						
Frequency	f_{IN}	CMOS	5	—	200	MHz
		HSTL, SSTL	5	—	350	MHz
Input Voltage	V_I		–0.1	—	VDD	V
Input Voltage Swing (CMOS Standard)		200 MHz, Tr/Tf = 1.3 ns	0.8	—	—	Vpp
Rise/Fall Time	t_R/t_F	20%–80%	—	—	4	ns
Duty Cycle	DC	< 2 ns tr/tf	40	50	60	%
Input Capacitance	C_{IN}		—	2	—	pF
Output Clocks (Differential)						
Frequency	f_{OUT}	LVPECL, LVDS	5	—	710	MHz
		HCSL	5	—	250	MHz

Table 4. Input and Output Clock Characteristics (Continued)
(V_{DD} = 1.8 V –5% to +10%, 2.5 V ±10%, or 3.3 V ±10%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
LVPECL Output Voltage	V_{OC}	common mode	—	V_{DDO} – 1.45 V	—	V
	V_{SEPP}	peak-to-peak single-ended swing	0.55	0.8	0.96	V_{PP}
LVDS Output Voltage (2.5/3.3 V)	V_{OC}	common mode	1.125	1.2	1.275	V
	V_{SEPP}	peak-to-peak single-ended swing	0.25	0.35	0.45	V_{PP}
LVDS Output Voltage (1.8 V)	V_{OC}	common mode	0.8	0.875	0.95	V
	V_{SEPP}	peak-to-peak single-ended swing	0.25	0.35	0.45	V_{PP}
HCSL Output Voltage	V_{OC}	common mode	0.35	0.375	0.400	V
	V_{SEPP}	peak-to-peak single-ended swing	0.575	0.725	0.85	V_{PP}
Rise/Fall Time	t_R/t_F	20%–80%	—	—	450	ps
Duty Cycle*	DC	CKn < 350 MHz	45	—	55	%
		350 MHz < CLKn < 710 MHz	40	—	60	%
Output Clocks (Single-Ended)						
Frequency	f_{OUT}	CMOS	5	—	200	MHz
		SSTL, HSTL	5	—	350	MHz
CMOS 20%-80% Rise/Fall Time	t_R/t_F	2 pF load	—	0.45	0.85	ns
CMOS 20%-80% Rise/Fall Time	t_R/t_F	15 pF load	—	—	2.0	ns
CMOS Output Resistance			—	50	—	Ω
SSTL Output Resistance			—	50	—	Ω
HSTL Output Resistance			—	50	—	Ω
CMOS Output Voltage	V_{OH}	4 mA load	VDDO–0.3	—		V
	V_{OL}	4 mA load		—	0.3	V
SSTL Output Voltage	V_{OH}	SSTL-3 VDDOx = 2.97 to 3.63 V	0.45xVDDO+0.41	—	—	V
	V_{OL}		—	—	0.45xVDDO –0.41	V
	V_{OH}	SSTL-2 VDDOx = 2.25 to 2.75 V	0.5xVDDO+0.41	—	—	V
	V_{OL}		—	—	0.5xVDDO–0.41	V
	V_{OH}	SSTL-18 VDDOx = 1.71 to 1.98 V	0.5xVDDO+0.34	—		V
	V_{OL}		—	—	0.5xVDDO–0.34	V

Table 4. Input and Output Clock Characteristics (Continued)

(V_{DD} = 1.8 V –5% to +10%, 2.5 V ±10%, or 3.3 V ±10%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
HSTL Output Voltage	V_{OH}	VDDO = 1.4 to 1.6 V	0.5xVDDO +0.3	—	—	V
	V_{OL}		—	—	0.5xVDDO –0.3	V
Duty Cycle*	DC		45	—	55	%
***Note:** Input clock has a 50% duty cycle.						

Table 5. OEB Input Specifications

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input Voltage Low	V_{IL}		—	—	0.3 x V_{DD}	V
Input Voltage High	V_{IH}		0.7 x V_{DD}	—	—	V
Input Resistance	R_{IN}		20	—	—	kΩ

Table 6. Output Control Pins (LOS)

(V_{DD} = 1.8 V –5% to +10%, 2.5 V ±10%, or 3.3 V ±10%, T_A = –40 to 85 °C)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Output Voltage Low	V_{OL}	I_{SINK} = 3 mA	0	—	0.4	V
Rise/Fall Time 20–80%	t_R/t_F	C_L < 10 pf, pull up ≤ 1 kΩ	—	—	10	ns

Table 7. Jitter Specifications

(V_{DD} = 1.8 V –5% to +10%, 2.5 V ±10%, or 3.3 V ±10%, T_A = –40 to 85°C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Additive Phase Jitter (12 kHz–20 MHz)	t_{RPHASE}	0.7 V pk-pk differential input clock at 622.08 MHz with 70 ps rise/fall time	—	0.150	—	ps RMS
Additive Phase Jitter (50 kHz–80 MHz)	$t_{RPHASEWB}$	0.7 V pk-pk differential input clock at 622.08 MHz with 70 ps rise/fall time	—	0.225	—	ps RMS

Table 8. Thermal Characteristics

Parameter	Symbol	Test Condition	Value	Unit
Thermal Resistance Junction to Ambient	θ_{JA}	Still Air	37	°C/W
Thermal Resistance Junction to Case	θ_{JC}	Still Air	25	°C/W

Table 9. Absolute Maximum Ratings[1,2,3,4,5]

Parameter	Symbol	Test Condition	Value	Unit
DC Supply Voltage	V_{DD}		–0.5 to 3.8	V
Storage Temperature Range	T_{STG}		–55 to 150	°C
ESD Tolerance		HBM (100 pF, 1.5 kΩ)	2.5	kV
ESD Tolerance		CDM	550	V
ESD Tolerance		MM	175	V
Latch-up Tolerance			JESD78 Compliant	
Junction Temperature	T_J		150	°C
Soldering Temperature (Pb-free profile)[5]	T_{PEAK}		260	°C
Soldering Temperature Time at T_{PEAK} (Pb-free profile)[5]	T_P		20–40	sec

Notes:

1. Permanent device damage may occur if the Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure to maximum rating conditions for extended periods may affect device reliability.
2. 24-QFN package is RoHS compliant.
3. For more packaging information, go to www.silabs.com/support/quality/pages/RoHSInformation.aspx.
4. Moisture sensitivity level is MSL3.
5. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

2. Functional Description

The Si5330 is a low-jitter, low-skew fanout buffer optimized for high-performance PCB clock distribution applications. The device produces four differential or eight single-ended, low-jitter output clocks from a single input clock. The input can accept either a single-ended or a differential clock allowing the device to function as a clock level translator.

2.1. V_{DD} and V_{DDO} Supplies

The core V_{DD} and output V_{DDO} supplies have separate and independent supply pins allowing the core supply to operate at a different voltage than the I/O voltage levels.

The V_{DD} supply powers the core functions of the device, which operates from 1.8, 2.5, or 3.3 V. Using a lower supply voltage helps minimize the device's power consumption. The V_{DDO} supply pins are used to set the output signal levels and must be set at a voltage level compatible with the output signal format.

2.2. Loss Of Signal Indicator (LOS)

The input is monitored for a valid clock signal using an LOS circuit that monitors input clock edges and declares an LOS condition when signal edges are not detected over a 1 to 5 µs observation period. The LOS pin is asserted "low" when activity on the input clock pin is present. A "high" level on the LOS pin indicates a loss of signal (LOS). The LOS pin must be pulled to VDD as shown in Figure 2.

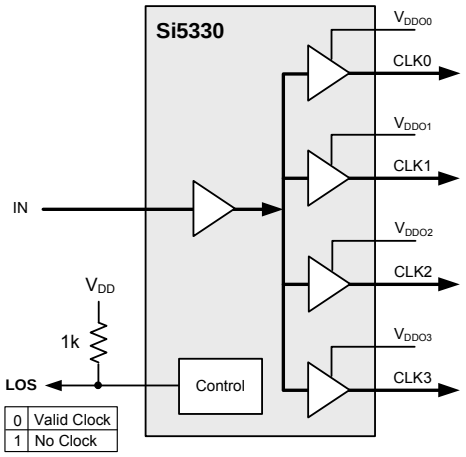


Figure 2. LOS Indicator with External Pull-Up

2.3. Output Enable (OEB)

The output enable (OEB) pin allows disabling or enabling of the outputs clocks (CLK0-CLK3). The output enable is logically controlled to ensure that no glitches or runt pulses are generated at the output as shown in Figure 3.

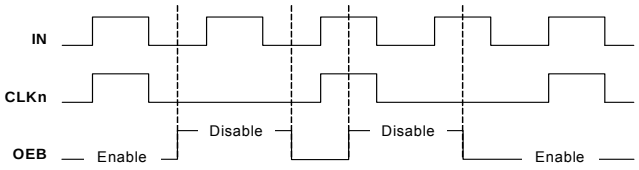


Figure 3. OEB Glitchless Operation

All outputs are enabled when the OEB pin is connected to ground or below the V_{IL} voltage for this pin. Connecting the OEB pin to VDD or above the V_{IH} level will disable the outputs. Both V_{IL} and V_{IH} are specified in Table 5. All outputs are forced to a logic "low" when disabled. The OEB pin is 3.3 V tolerant.

2.4. Input Signals

The Si5330 can accept single-ended and differential input clocks. See "AN408: Termination Options for Any-Frequency, Any-Output Clock Generators and Clock Buffers—Si5338, Si5334, Si5330" for details on connecting a wide variety of signals to the Si5330 inputs.

2.5. Output Driver Formats

The Si5330 supports single-ended output formats of CMOS, SSTL, and HSTL and differential formats of LVDS, LVPECL, and HCSL. It is normally required that the LVDS driver be dc-coupled to the 100 Ω termination at the receiver end. If your application requires an ac-coupled 100 Ω load, contact the applications team for advice. See AN408 for additional information on the terminations for these driver types.

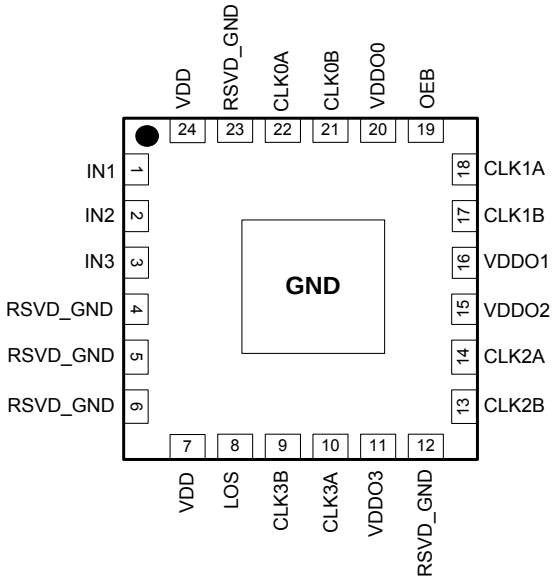
2.6. Input and Output Terminations

See AN408 for detailed information.

3. Ordering the Si5330

The Si5330 can be ordered to meet the requirements of the most commonly-used input and output signal types, such as CMOS, SSTL, HSTL, LVPECL, LVDS, and HSCL. See Figure 1, "Si5330 Functional Block Diagrams," on page 2 and Table 11, "Order Numbers and Device Functionality," on page 14 for specific ordering information.

4. Pin Descriptions



Note: Center pad must be tied to GND for normal operation.

Table 10. Si5330 Pin Descriptions

Pin #	Pin Name	I/O	Signal Type	Description
1	IN1	I	Multi	**Si5330A/B/C/G/H/J Differential Input Devices.** These pins are used as the differential clock input. IN1 is the positive input; IN2 is the negative input. Refer to "AN408: Termination Options for Any-Frequency, Any-Output Clock Generators and Clock Buffers—Si5338, Si5334, Si5330" for interfacing and termination details. **Si5330F/K/L/M Single-Ended Input Devices.** These pins are not used. Leave IN1 unconnected and IN2 connected to ground.
2	IN2	I	Multi	
3	IN3	I	Multi	**Si5330F/K/L/M Single-Ended Devices.** This is the single-ended clock input. Refer to AN408 for interfacing and termination details. **Si5330A/B/C/G/H/J Differential Input Devices.** This pin is not used. Connect to ground.
4	RSVD_GND			**Ground.** Must be connected to system ground.
5	RSVD_GND			**Ground.** Must be connected to system ground.
6	RSVD_GND			**Ground.** Must be connected to system ground.

Table 10. Si5330 Pin Descriptions (Continued)

Pin #	Pin Name	I/O	Signal Type	Description
7	VDD	VDD	Supply	**Core Supply Voltage.** The device operates from a 1.8, 2.5, or 3.3 V supply. A 0.1 µF bypass capacitor should be located very close to this pin.
8	LOS	O	Open Drain	**Loss of Signal Indicator.** 0 = CLKIN present. 1 = Loss of signal (LOS). This pin requires an external ≥1 kΩ pull-up resistor.
9	CLK3B	O	Multi	**Si5330A/B/C/K/L/M Differential Output Devices.** This is the negative side of the differential CLK3 output. Refer to AN408 for interfacing and termination details. Leave unconnected when not in use. **Si5330F/G/H/J Single-Ended Output Devices.** This is one of the single-ended CLK3 outputs. Both CLK3A and CLK3B single-ended outputs are in phase. Refer to AN408 for interfacing and termination details. Leave unconnected when not is use.
10	CLK3A	O	Multi	**Si5330A/B/C/K/L/M Differential Devices.** This is the positive side of the differential CLK3 output. Refer to AN408 for interfacing and termination details. Leave unconnected when not in use. **Si5330F/G/H/J Single-Ended Devices.** This is one of the single-ended CLK3 outputs. Both CLK3A and CLK3B single-ended outputs are in phase. Refer to AN408 for interfacing and termination details. Leave unconnected when not is use.
11	VDDO3	VDD	Supply	**Output Clock Supply Voltage.** Supply voltage for CLK3A/B. Use a 0.1 µF bypass cap as close as possible to this pin. If CLK3 is not used, this pin must be tied to V_{DD} (pin 7 and/or pin 24).
12	RSVD_GND			**Ground.** Must be connected to system ground.
13	CLK2B	O	Multi	**Si5330A/B/C/K/L/M Differential Output Devices.** This is the negative side of the differential CLK2 output. Refer to AN408 for interfacing and termination details. Leave unconnected when not in use. **Si5330F/G/H/J Single-Ended Output Devices.** This is one of the single-ended CLK2 outputs. Both CLK2A and CLK2B single-ended outputs are in phase. Refer to AN408 for interfacing and termination details. Leave unconnected when not is use.

Table 10. Si5330 Pin Descriptions (Continued)

Pin #	Pin Name	I/O	Signal Type	Description
14	CLK2A	O	Multi	**Si5330A/B/C/K/L/M Differential Devices.** This is the positive side of the differential CLK2 output. Refer to AN408 for interfacing and termination details. Leave unconnected when not in use. **Si5330F/G/H/J Single-Ended Devices.** This is one of the single-ended CLK2 outputs. Both CLK2A and CLK2B single-ended outputs are in phase. Refer to AN408 for interfacing and termination details. Leave unconnected when not is use.
15	VDDO2	VDD	Supply	**Output Clock Supply Voltage.** Supply voltage for CLK2A/B. Use a 0.1 µF bypass cap as close as possible to this pin. If CLK2 is not used, this pin must be tied to V_{DD} (pin 7 and/or pin 24).
16	VDDO1	VDD	Supply	**Output Clock Supply Voltage.** Supply voltage for CLK1A,B. Use a 0.1 µF bypass cap as close as possible to this pin. If CLK1 is not used, this pin must be tied to V_{DD} (pin 7 and/or pin 24).
17	CLK1B	O	Multi	**Si5330A/B/C/K/L/M Differential Output Devices.** This is the negative side of the differential CLK1 output. Refer to AN408 for interfacing and termination details. Leave unconnected when not in use. **Si5330F/G/H/J Single-Ended Output Devices.** This is one of the single-ended CLK1 outputs. Both CLK1A and CLK1B single-ended outputs are in phase. Refer to AN408 for interfacing and termination details. Leave unconnected when not is use.
18	CLK1A	O	Multi	**Si5330A/B/C/K/L/M Differential Devices.** This is the positive side of the differential CLK1 output. Refer to AN408 for interfacing and termination details. Leave unconnected when not in use. **Si5330F/G/H/J Single-Ended Devices.** This is one of the single-ended CLK1 outputs. Both CLK1A and CLK1B single-ended outputs are in phase. Refer to AN408 for interfacing and termination details. Leave unconnected when not is use.
19	OEB	I	CMOS	**Output Enable.** All outputs are enabled when the OEB pin is connected to ground or below the V_{IL} voltage for this pin. Connecting the OEB pin to V_{DD} or above the V_{IH} level will disable the outputs. Both V_{IL} and V_{IH} are specified in Table 5. All outputs are forced to a logic “low” when disabled. This pin is 3.3 V tolerant.
20	VDDO0	VDD	Supply	**Output Clock Supply Voltage.** Supply voltage for CLK0A,B. Use a 0.1 µF bypass cap as close as possible to this pin. If CLK2 is not used, this pin must be tied to V_{DD} (pin 7 and/or pin 24).

Table 10. Si5330 Pin Descriptions (Continued)

Pin #	Pin Name	I/O	Signal Type	Description
21	CLK0B	O	Multi	**Si5330A/B/C/K/L/M Differential Output Devices.** This is the negative side of the differential CLK0 output. Refer to AN408 for interfacing and termination details. Leave unconnected when not in use. **Si5330F/G/H/J Single-ended Output Devices.** This is one of the single-ended CLK0 outputs. Both CLK0A and CLK0B single-ended outputs are in phase. Refer to AN408 for interfacing and termination details. Leave unconnected when not is use.
22	CLK0A	O	Multi	**Si5330A/B/C/K/L/M Differential Devices.** This is the positive side of the differential CLK0 output. Refer to AN408 for interfacing and termination details. Leave unconnected when not in use. **Si5330F/G/H/J Single-ended Devices.** This is one of the single-ended CLK0 outputs. Both CLK0A and CLK0B single-ended outputs are in phase. Refer to AN408 for interfacing and termination details. Leave unconnected when not is use.
23	RSVD_GND			**Ground.** Must be connected to system ground.
24	VDD	VDD	Supply	**Core Supply Voltage.** The device operates from a 1.8, 2.5, or 3.3 V supply. A 0.1 µF bypass capacitor should be located very close to this pin.
GND PAD	GND	GND	Supply	**Ground Pad.** This is main ground connection for this device. It is located at the bottom center of the package. Use as many vias as possible to connect this pad to the main ground plane. The device will not function as specified unless this ground pad is properly connected to ground.

5. Orderable Part Numbers and Device Functionality

Table 11. Order Numbers and Device Functionality

Part Number[1,2]	Input Signal Format	Output Signal Format	Number of Outputs	Frequency Range
LVPECL Buffers				
Si5330A-B00200-GM	Differential	3.3 V LVPECL	4	5 to 710 MHz
Si5330A-B00202-GM	Differential	2.5 V LVPECL	4	5 to 710 MHz
LVDS Buffers				
Si5330B-B00204-GM	Differential	3.3 V LVDS	4	5 to 710 MHz
Si5330B-B00205-GM	Differential	2.5 V LVDS	4	5 to 710 MHz
Si5330B-B00206-GM	Differential	1.8 V LVDS	4	5 to 710 MHz
HCSL Buffers				
Si5330C-B00207-GM	Differential	3.3 V HCSL	4	5 to 250 MHz
Si5330C-B00208-GM	Differential	2.5 V HCSL	4	5 to 250 MHz
Si5330C-B00209-GM	Differential	1.8 V HCSL	4	5 to 250 MHz
CMOS Buffers				
Si5330F-B00214-GM	Single-Ended	3.3 V CMOS	8	5 to 200 MHz
Si5330F-B00215-GM	Single-Ended	2.5 V CMOS	8	5 to 200 MHz
Si5330F-B00216-GM	Single-Ended	1.8 V CMOS	8	5 to 200 MHz
CMOS Buffers (Differential Input)				
Si5330G-B00217-GM	Differential	3.3 V CMOS	8	5 to 200 MHz
Si5330G-B00218-GM	Differential	2.5 V CMOS	8	5 to 200 MHz
Si5330G-B00219-GM	Differential	1.8 V CMOS	8	5 to 200 MHz
SSTL Buffers (Differential Input)				
Si5330H-B00220-GM	Differential	3.3 V SSTL	8	5 to 350 MHz
Si5330H-B00221-GM	Differential	2.5 V SSTL	8	5 to 350 MHz
Si5330H-B00222-GM	Differential	1.8 V SSTL	8	5 to 350 MHz
HSTL Buffers (Differential Input)				
Si5330J-B00223-GM	Differential	1.5 V HSTL	8	5 to 350 MHz
LVPECL Buffers (Single-Ended Input)				
Si5330K-B00224-GM	Single-Ended	3.3 V LVPECL	4	5 to 350 MHz
Si5330K-B00226-GM	Single-Ended	2.5 V LVPECL	4	5 to 350 MHz

Notes:
1. Custom configurations with mixed output types are also available. Please contact the factory for ordering details.
2. Add an “R” to the part number to specify tape and reel shipment media. When specifying non-tape-and-reel shipment media, contact your sales representative for more information.

Table 11. Order Numbers and Device Functionality (Continued)

Part Number[1,2]	Input Signal Format	Output Signal Format	Number of Outputs	Frequency Range
LVDS Buffers (Single-Ended Input)				
Si5330L-B00228-GM	Single-Ended	3.3 V LVDS	4	5 to 350 MHz
Si5330L-B00229-GM	Single-Ended	2.5 V LVDS	4	5 to 350 MHz
Si5330L-B00230-GM	Single-Ended	1.8 V LVDS	4	5 to 350 MHz
HCSL Buffers (Single-Ended Input)				
Si5330M-B00231-GM	Single-Ended	3.3 V HCSL	4	5 to 250 MHz
Si5330M-B00232-GM	Single-Ended	2.5 V HCSL	4	5 to 250 MHz
Si5330M-B00233-GM	Single-Ended	1.8 V HCSL	4	5 to 250 MHz

Notes:
1. Custom configurations with mixed output types are also available. Please contact the factory for ordering details.
2. Add an “R” to the part number to specify tape and reel shipment media. When specifying non-tape-and-reel shipment media, contact your sales representative for more information.

6. Package Outline: 24-Lead QFN

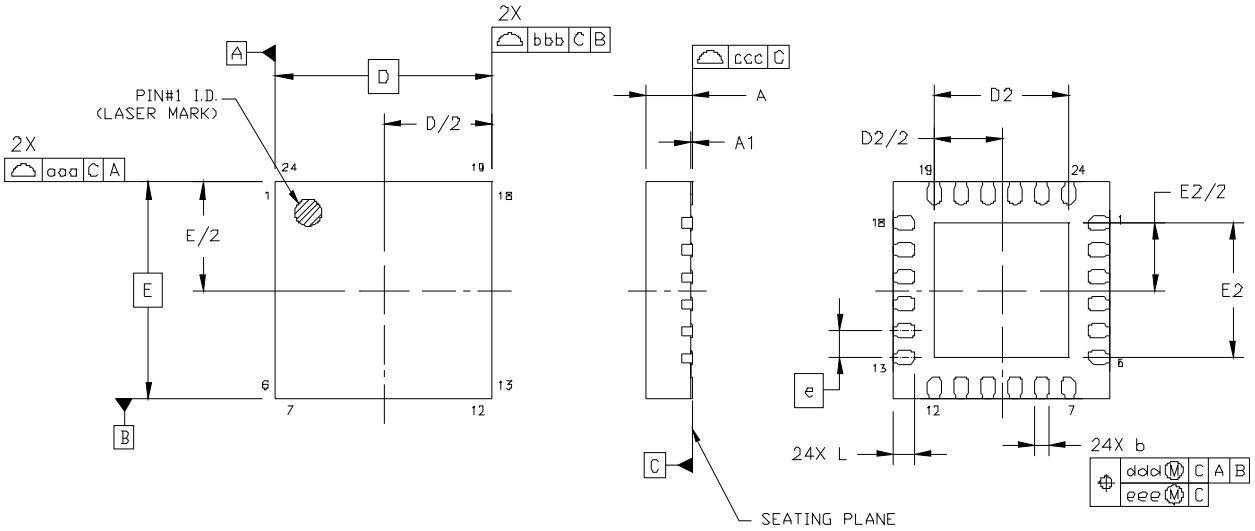


Figure 4. 24-Lead Quad Flat No-Lead (QFN)

Table 12. Package Dimensions

Dimension	Min	Nom	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
D		4.00 BSC.	
D2	2.35	2.50	2.65
e		0.50 BSC.	
E		4.00 BSC.	
E2	2.35	2.50	2.65
L	0.30	0.40	0.50
aaa		0.10	
bbb		0.10	
ccc		0.08	
ddd		0.10	
eee		0.05	

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Outline MO-220, variation VGGD-8.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.
5. J-STD-020 MSL rating: MSL3.
6. Terminal base alloy: Cu.
7. Terminal plating/grid array material: Au/NiPd.
8. For more packaging information, go to www.silabs.com/support/quality/pages/RoHSInformation.aspx.

7. Recommended PCB Layout

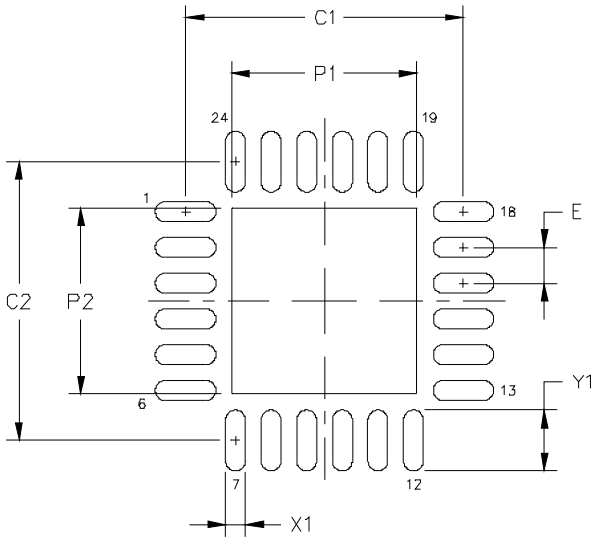


Table 13. PCB Land Pattern

Dimension	Min	Nom	Max
P1	2.50	2.55	2.60
P2	2.50	2.55	2.60
X1	0.20	0.25	0.30
Y1	0.75	0.80	0.85
C1	3.90		
C2	3.90		
E	0.50		

Notes:

General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on the IPC-7351 guidelines.
4. Connect the center ground pad to a ground plane with no less than five vias to a ground plane that is no more than 20 mils below it. Via drill size should be no smaller than 10 mils. A longer distance to the ground plane is allowed if more vias are used to keep the inductance from increasing.

Solder Mask Design

5. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

Stencil Design

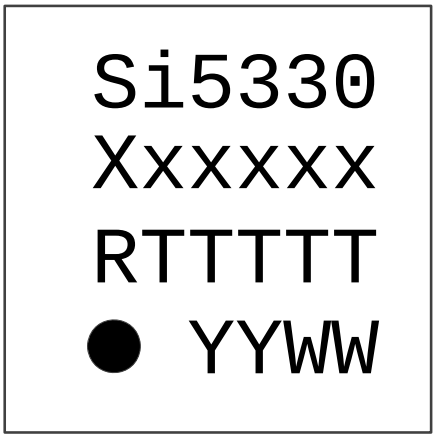
6. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
7. The stencil thickness should be 0.125 mm (5 mils).
8. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pins.
9. A 2x2 array of 1.0 mm square openings on 1.25 mm pitch should be used for the center ground pad.

Card Assembly

10. A No-Clean, Type-3 solder paste is recommended.
11. The recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

8. Top Marking

8.1. Si5330 Top Marking



8.2. Top Marking Explanation

Mark Method:	Laser	
Line 1 Marking:	Device Part Number	Si5330
Line 2 Marking:	X = Frequency and configuration code. xxxxx = Input and output format configuration code. See "5. Orderable Part Numbers and Device Functionality" on page 14 for more information.	Xxxxxx
Line 3 Marking:	R = Product revision. TTTTT = Manufacturing trace code.	RTTTTT
Line 4 Marking:	Pin 1 indicator.	Circle with 0.5 mm diameter; left-justified
	YY = Year. WW = Work week. Characters correspond to the year and work week of package assembly.	YYWW

DOCUMENT CHANGE LIST

Revision 0.1 to Revision 0.2

- Clarified documentation to reflect that Pin 19 is OEB (OE Enable Low).
- Updated Table 4, “Jitter Specifications” on page 7.

Revision 0.2 to Revision 0.3

- Major editorial updates to improve clarity.
- Updated “Additive Jitter” Specification Table.
- Updated “Core Supply Current” Specification in Table 2.
- Removed the Low-Power LVPECL output options from the ordering table in section 5.
- Removed D/E ordering options.

Revision 0.3 to Revision 0.35

- Typo of 150 ps on front page changed to 150 fs.
- Updated PCB layout notes.
- Added no ac coupling for LVDS outputs.
- Changed input rise/fall time spec to 2 ns.

Revision 0.35 to Revision 1.0

- Added maximum junction temperature specification to Table 9 on page 8.
- Added minimum and maximum duty cycle specifications to Table 4 on page 5.
- Updated Table 3, “Performance Characteristics,” on page 5.
  - Added maximum propagation delay spec (4 ns).
  - Added test condition to t_{LOS_B} in Table 3 on page 5.
  - Removed reference to frequency in Output-Output Skew.
- Updated Table 4, “Input and Output Clock Characteristics,” on page 5.
  - Input voltage (max) changed “3.63” to “VDD”
  - Input voltage swing (max) change “3.63” with “—”.
- Added Table 6, “Output Control Pins (LOS),” on page 7.
- Added tape and reel ordering information to "5. Orderable Part Numbers and Device Functionality" on page 14.
- Added "8. Top Marking" on page 18.

Revision 1.0 to Revision 1.1

- Updated ordering information to refer to revision B silicon.
- Updated top marking explanation in section 8.2.

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https://www.silabs.com/support/pages/contacttechnicalsupport.aspx
and register to submit a technical support request.

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TERMINATION OPTIONS FOR ANY-FREQUENCY, ANY-OUTPUT CLOCK GENERATORS AND CLOCK BUFFERS

1. Introduction

This application note provides termination recommendations for connecting input and output clock signals to the Si533x and Si5356/55 family of timing ICs and is not applicable to any other Silicon Labs devices.

The Si533x and Si5356/55 family of any-frequency, any-output clock generators and clock buffers greatly simplifies the task of interfacing between many of today's common signal types. Both the inputs and the outputs are compatible with single-ended (LVTTL, CMOS, HSTL, SSTL) and/or differential signals (LVPECL, LVDS, HCSL, CML) and support multiple supply voltage levels (3.3, 2.5, 1.8, or 1.5 V). All of the inputs and outputs are configured on a per-port basis offering unprecedented flexibility. Block diagrams of the devices are shown in Figures 1 and 2. The Si5338 and Si5356 are I^2C-configured devices that lock to a crystal or external clock and generate up to four independent output frequencies. The Si5338 is compatible with both single-ended and differential clock formats, whereas the Si5356 is limited to single-ended clocks. The Si5334 is a pin-controlled version of the Si5338 that does not have an I^2C interface. Similarly, the Si5355 is a pin-controlled version of the Si5356. The Si5330 is a non-PLL clock buffer device that provides low jitter clock distribution and level translation.

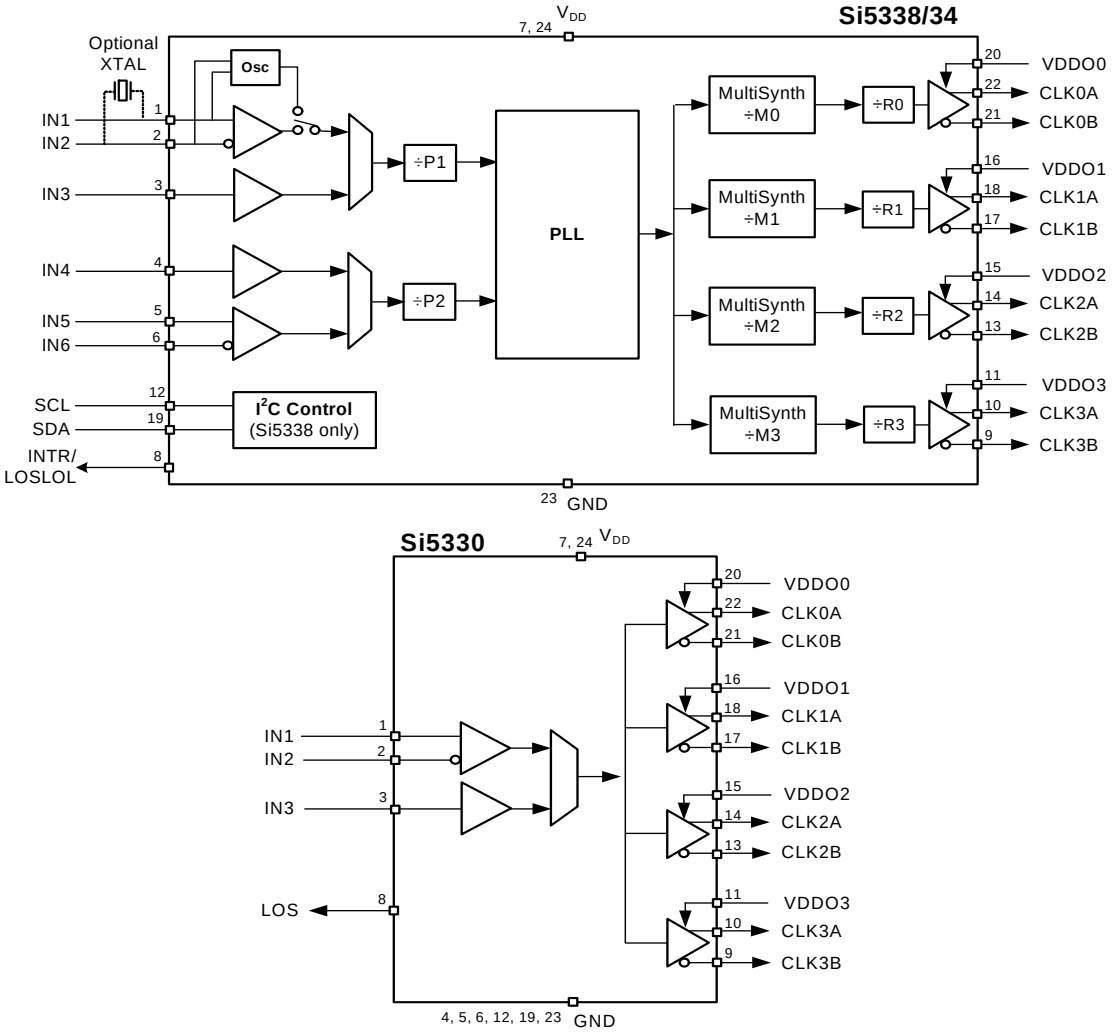


Figure 1. Si5338/34 and Si5330 Block Diagrams

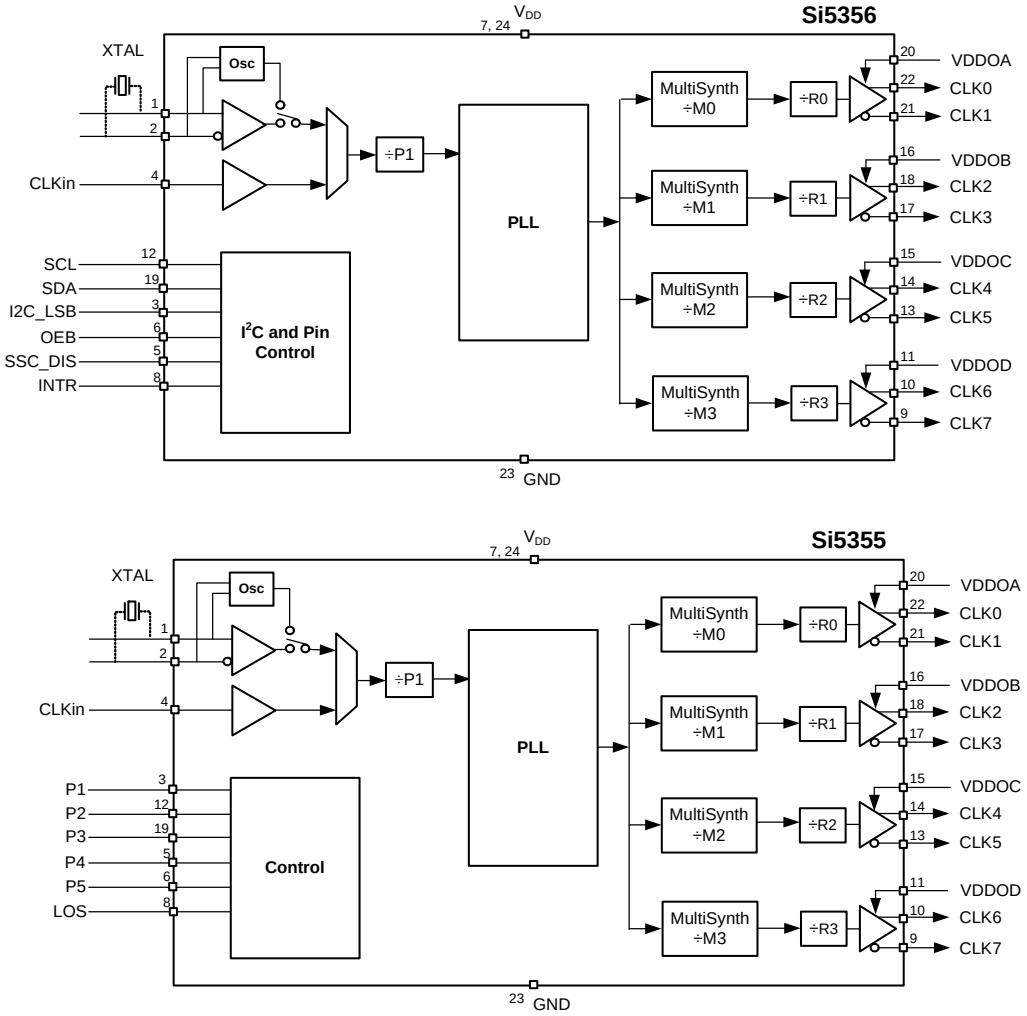


Figure 2. Si5356 and Si5355 Block Diagrams

2. Inputs

The Si533x and Si5356/55 families support both single-ended and differential inputs. The device supports up to two single-ended inputs (Pins 3 and 4) and two differential inputs (Pins 1,2, and 5,6). On the Si5338/34 and Si5356/55 devices, a crystal can be connected to Pins 1 and 2 instead of an input clock. Refer to “AN360: Crystal Selection Guide for Any-Frequency Devices” for more information on using the crystal input option.

2.1. Single-Ended Inputs

The multi-format single-ended clock inputs of the Si533x and Si5356/55 are ac-coupled internally to remove any dc bias from the signal. This allows the device to trigger on a signal swing threshold instead of a specific voltage level (normally specified as V_{IH} and V_{IL}). The receiver accepts any signal with a minimum voltage swing of 800 mV_{PP} and a maximum of 3.73 V_{PP} regardless of the core V_{DD} supply. For best performance, the slew rate at input Pins 3 and 4 must be greater than 1 V/ns. This makes the inputs 3.3 V-tolerant even when the core voltage is powered with 1.8 V. An Si5338/34/56/55 should have an input duty cycle no worse than 40/60%. An Si5330 should have an input duty cycle no worse than 45/55%.

2.1.1. LVTTL/CMOS Inputs

The only termination necessary when interfacing a CMOS driver to the Si533x and Si5356/55 is a source resistor (Rs) placed near the driver to help match its output impedance to the transmission line impedance. In some cases, the value for this series resistor may be zero as it depends upon the CMOS driver characteristics. The CMOS drivers in the Si533x and Si5356/55 are designed to work optimally into a 50 Ω transmission line without an external source resistor. A typical CMOS signal connection is illustrated in Figure 3. Using this configuration, the receiver is capable of interfacing to 3.3, 2.5, or 1.8 V CMOS clock signals.

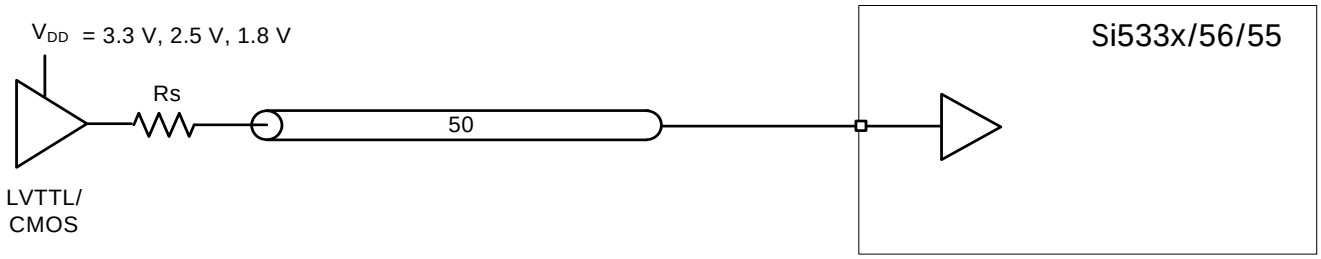
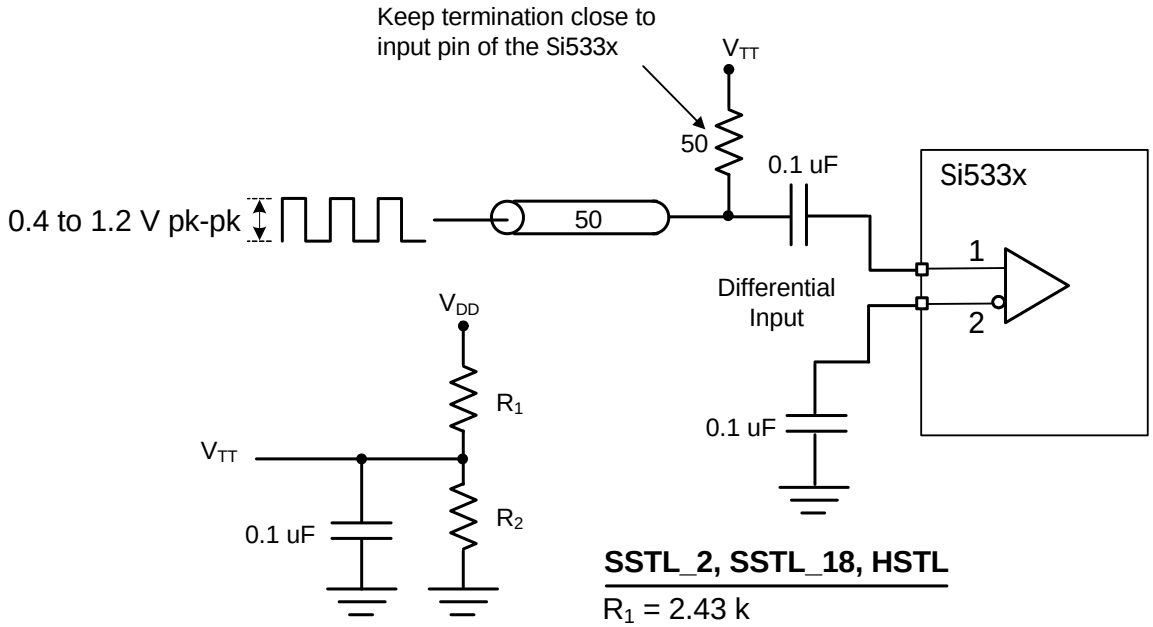


Figure 3. Interfacing to an LVTTL/CMOS Input Signal

2.1.2. Single-Ended SSTL and HSTL Inputs

HSTL and SSTL single-ended clock inputs should be input to the differential inputs, pins 1 and 2, of the Si533x with the circuit shown in Figure 4.

Some drivers may require a series 25 Ω resistor. If the SSTL/HSTL input is being driven by another Si533x device, the 25 Ω series resistor is not required as this is integrated on-chip. The maximum recommended input frequency in this case is 350 MHz.



SSTL_2, SSTL_18, HSTL

R_1 = 2.43 k

R_2 = 2 k

SSTL_3

R_1 = 2.43 k

R_2 = 2 k

Figure 4. Single-Ended SSTL/HSTL Input to Pins 1 and 2

2.1.3. Applying a Single-Ended Signal to a Differential Input

It is possible to interface any single-ended signal to the differential input pins (IN1/IN2 or IN5/IN6). The recommended interface for a signal that requires a 50 Ω load is shown in Figure 5. On these inputs, it is important that the signal level be less than 1.2 V_{PP} SE and greater than 0.4 V_{PP} SE. The maximum recommended input frequency in this case is 350 MHz.

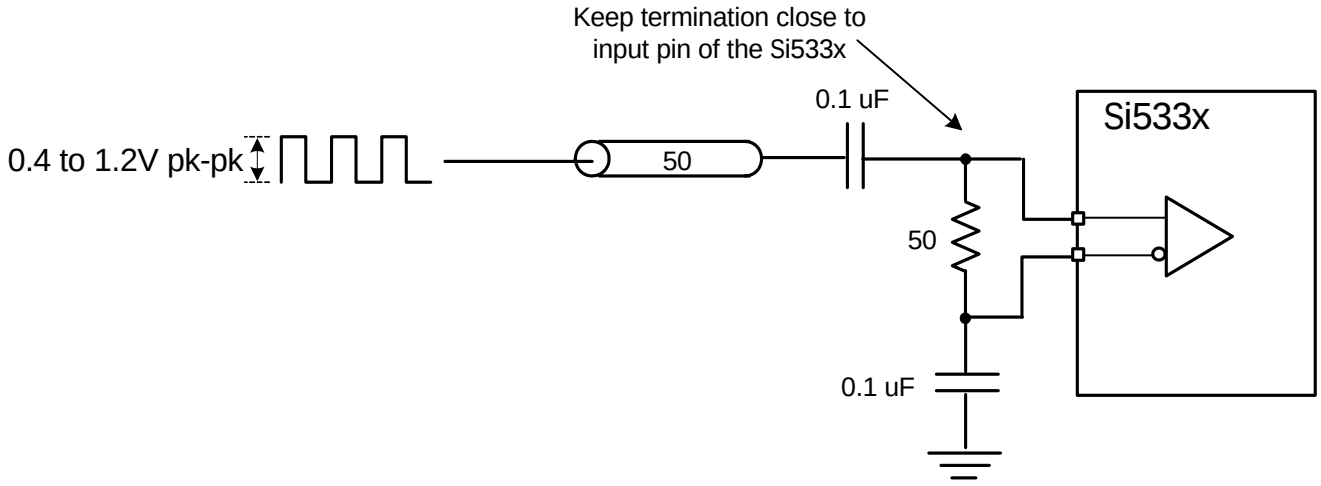


Figure 5. Single-Ended Input Signal with 50 Ω Termination

2.2. Differential Inputs

The multi-format differential clock inputs of the Si533x will interface with today's most common differential signals, such as LVDS, LVPECL, CML, and HCSL. The differential inputs are internally self-biased *and must be ac-coupled externally with a 0.1 µF capacitor*. The receiver will accept a signal with a voltage swing between 400 mV and 2.4 V_{PP} differential. Each half of the differential signal must not exceed 1.2 V_{PP} at the input to the Si533x or else the 1.3 V dc voltage limit may be exceeded.

2.2.1. LVDS Inputs

When interfacing the Si533x device to an LVDS signal, a 100 Ω termination is required at the input along with the required dc blocking capacitors as shown in Figure 6.

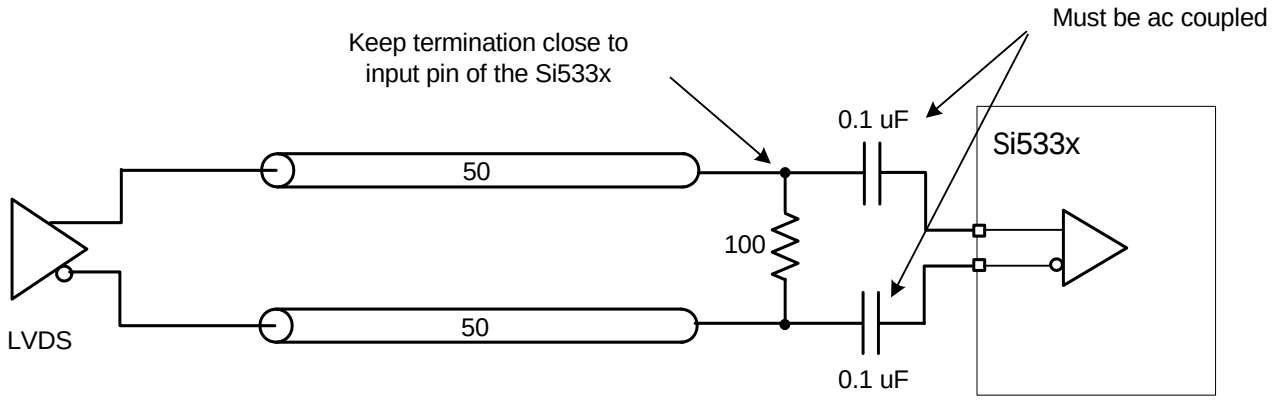
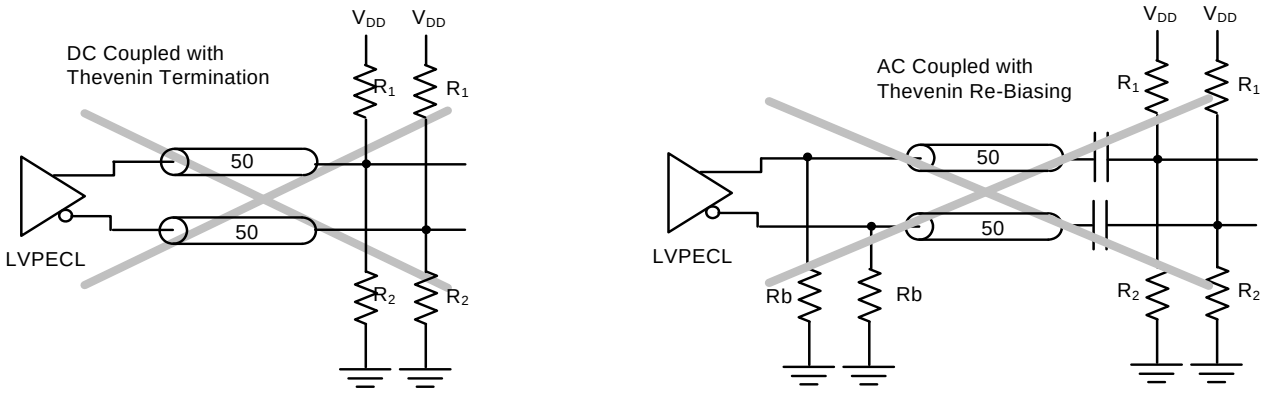


Figure 6. LVDS Input Signal

2.2.2. LVPECL Inputs

Since the differential receiver of the Si533x is internally self biased, an LVPECL signal may not be dc-coupled to the device. Figure 7 shows some common LVPECL connections that should not be used because of the dc levels they present at the receiver's input.



Not Recommended

Figure 7. Common LVPECL Connections that May be Destructive to the Si533x Input

Recommended configurations for interfacing an LVPECL input signal to the Si533x are shown in Figure 8. Typical values for the bias resistors (Rb) range between 120 and 200 Ω depending on the LVPECL driver. The 100 Ω resistor provides line termination. Because the receiver is internally self-biased, no additional external bias is required.

Another solution is to terminate the LVPECL driver with a Thevenin configuration as shown in Figure 8b. The values for R_1 and R_2 are calculated to provide a 50Ω termination to V_{DD}-2V. Given this, the recommended resistor values are R_1 = 127 Ω and R_2 = 82.5 Ω for V_{DD} = 3.3 V, and R_1 = 250 Ω and R_2 = 62.5 Ω for V_{DD} = 2.5 V.

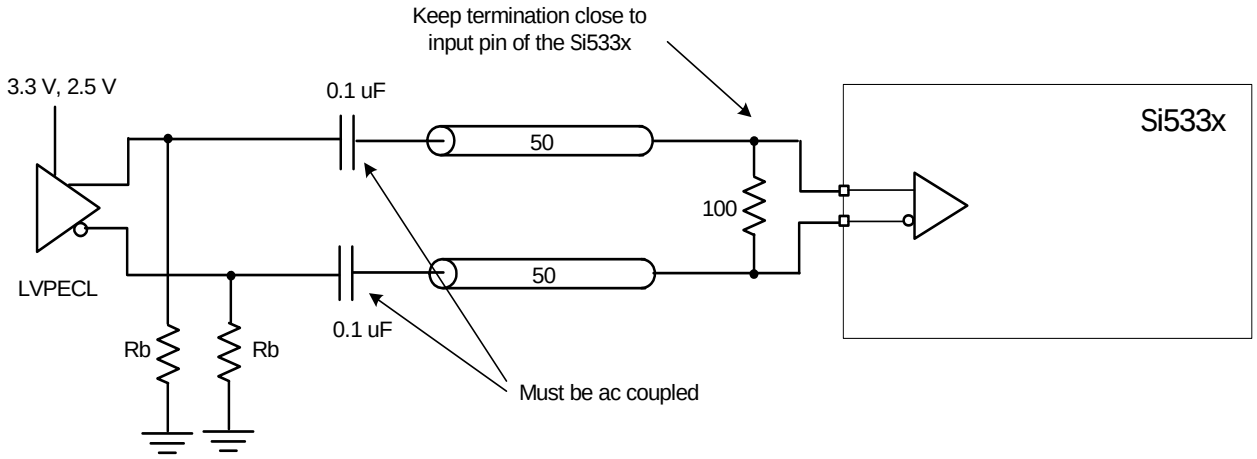


Figure 8a—LVPECL Input Signal with Source Biasing Option

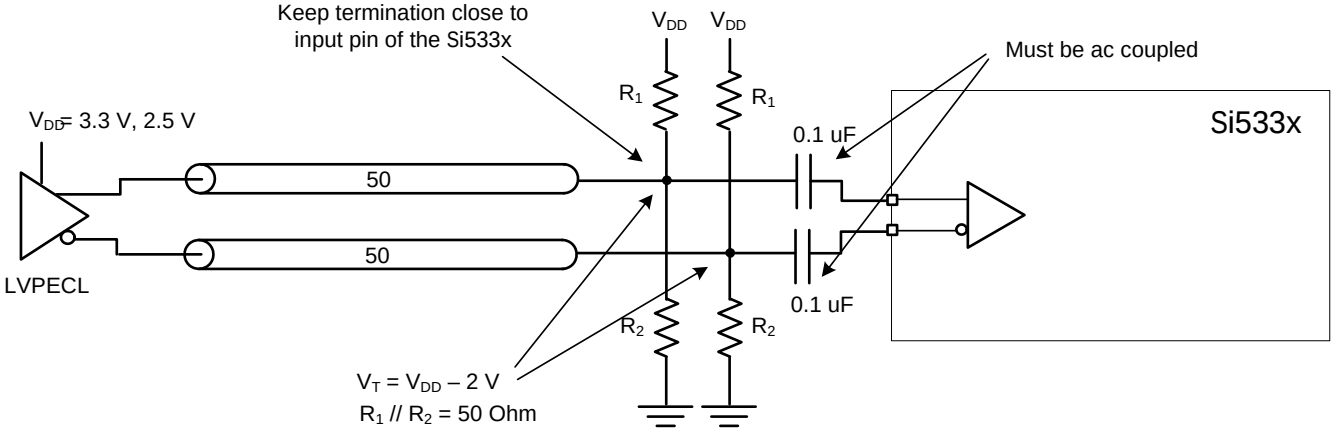


Figure 8b—LVPECL Input Signal with Load Biasing Option

Figure 8. Recommended Options for Interfacing to an LVPECL Signal

2.2.3. CML Inputs

CML signals may be applied to the differential inputs of the Si533x. Since the Si533x differential inputs are internally self-biased, a CML signal may not be dc-coupled to the device.

The recommended configurations for interfacing a CML input signal to the Si533x are shown in Figure 9. The 100 Ω resistor provides line termination, and, since the receiver is internally-biased, no additional external biasing components are required.

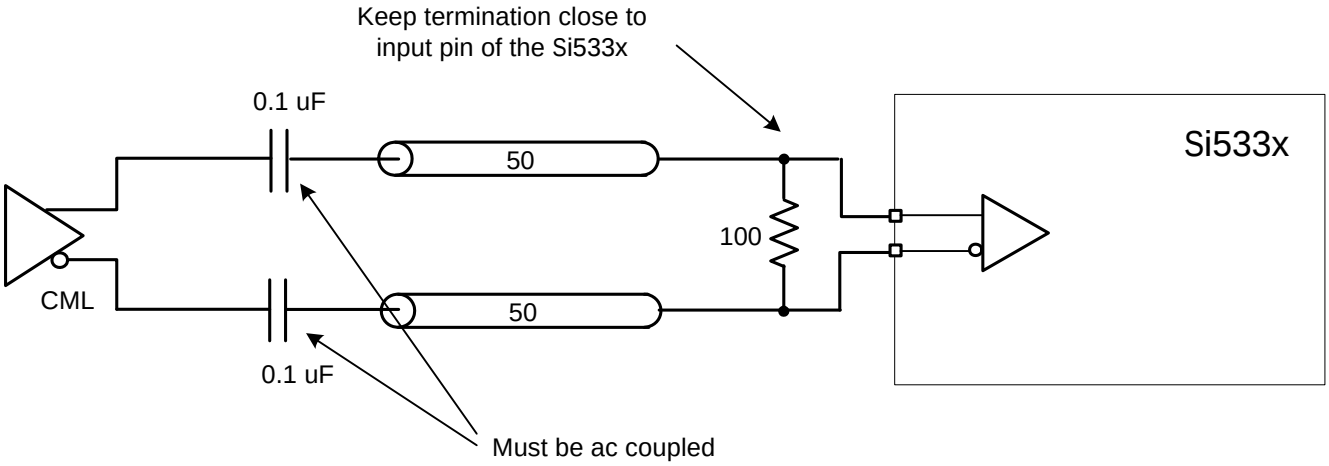


Figure 9. CML Input Signal

2.2.4. Applying CMOS Level Signal to Differential Inputs

Note that the maximum voltage level on the differential input pins on all Si533x must not exceed 1.3 V. To apply a CMOS signal to any of these pins, use the circuit shown in Figure 10. For a CMOS signal applied to these differential inputs, the maximum recommended frequency is 200 MHz.

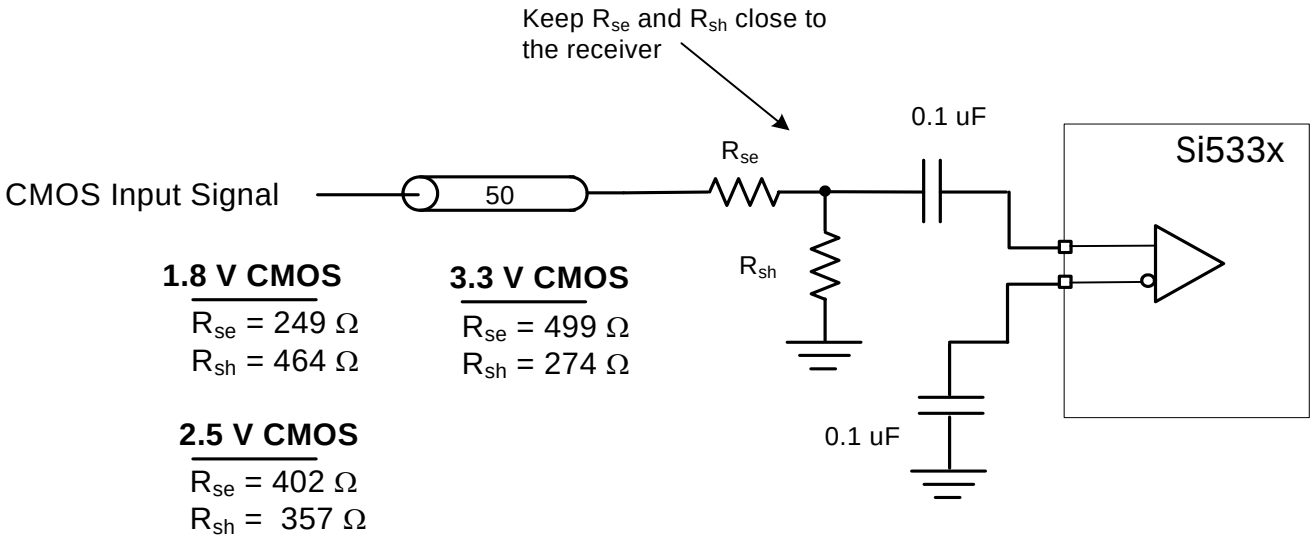


Figure 10. Applying a CMOS Level Signal to the Differential Inputs

2.2.5. HCSL Inputs

A typical HCSL driver has an open source output, which requires an external series resistor and a resistor to ground. The values of these resistors depend on the driver but are typically equal to 33 Ω (Rs) and 50 Ω (Rt). Note that the HCSL driver in the Si533x requires neither Rs nor Rt resistors. Other than two ac-coupling capacitors, no additional external components are necessary when interfacing an HCSL signal to the Si533x.

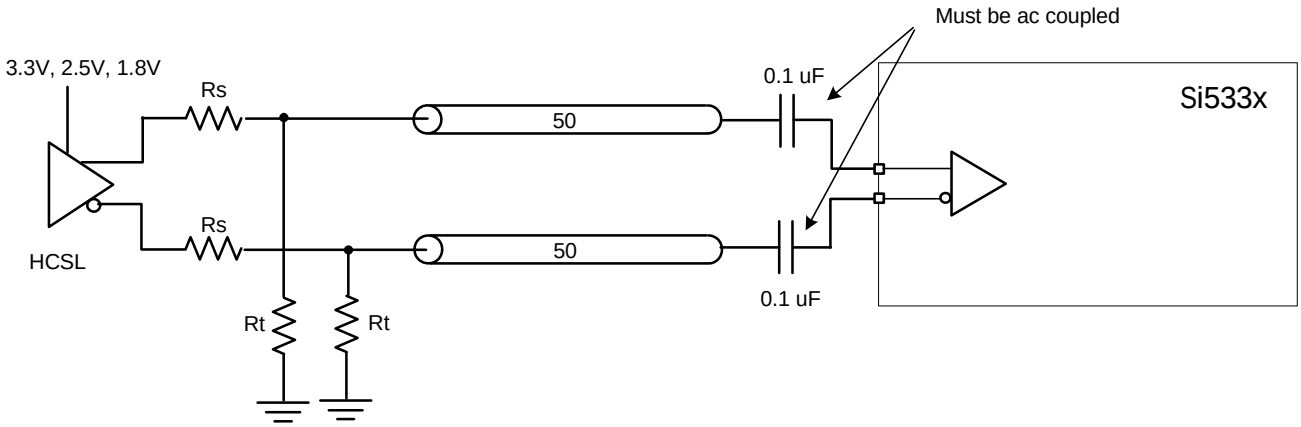


Figure 11. HCSL Input Signal to Si533x

3. Outputs

The Si533x devices provide four outputs that can be differential or single-ended. The Si5356/55 devices only have CMOS outputs. When configured as single-ended, the driver generates two signals that can be configured as in-phase or complimentary. Each of the outputs has its own output supply pin, allowing the device to be used in mixed supply applications without the need for external level translators. Each output driver is configurable to support the following signal types: CMOS/LVTTL, SSTL, HSTL, LVPECL, LVDS, and HCSL. The Si5338 also supports a CML output driver.

3.1. CMOS/LVTTL Outputs

The CMOS output driver has a controlled impedance of about 50 Ω, which includes an internal series resistor of approximately 22 Ω. For this reason, an external Rs series resistor is not recommended when driving 50 Ω traces. If the trace impedance is higher than 50 Ω, a series resistor, Rs, should be used. A typical configuration is shown in Figure 12. By default, the CMOS outputs of the driver are in-phase and can be used to drive two receivers. They can also be configured as complimentary outputs. The output supports 3.3, 2.5, and 1.8 V CMOS signal levels when the appropriate voltage is supplied to the external VDDO pin and the device is configured accordingly.

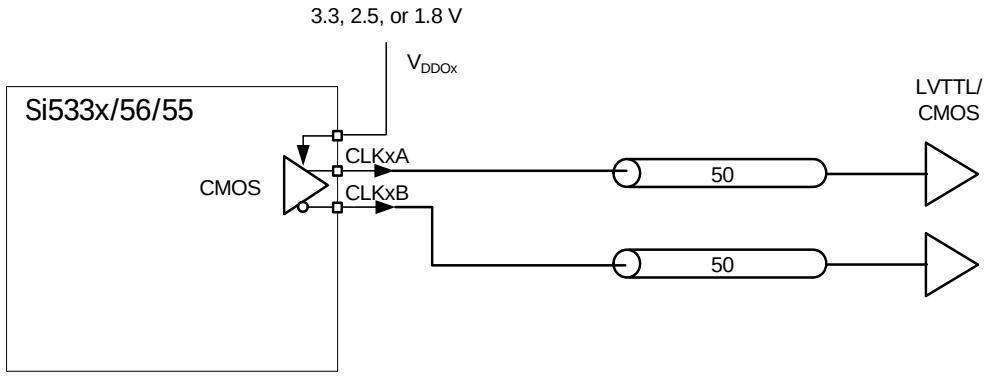


Figure 12. Interfacing to a CMOS Receiver

3.1.1. 1.5 and 1.2 V CMOS Outputs

The Si533x/55/56 output drivers natively support 3.3, 2.5, and 1.8 V CMOS. However, 1.5 and 1.2 V CMOS signals can be obtained using a two-resistor network as shown in Figure 13 and Table 1 below. Place R1 and R2 as close to the device output as possible.

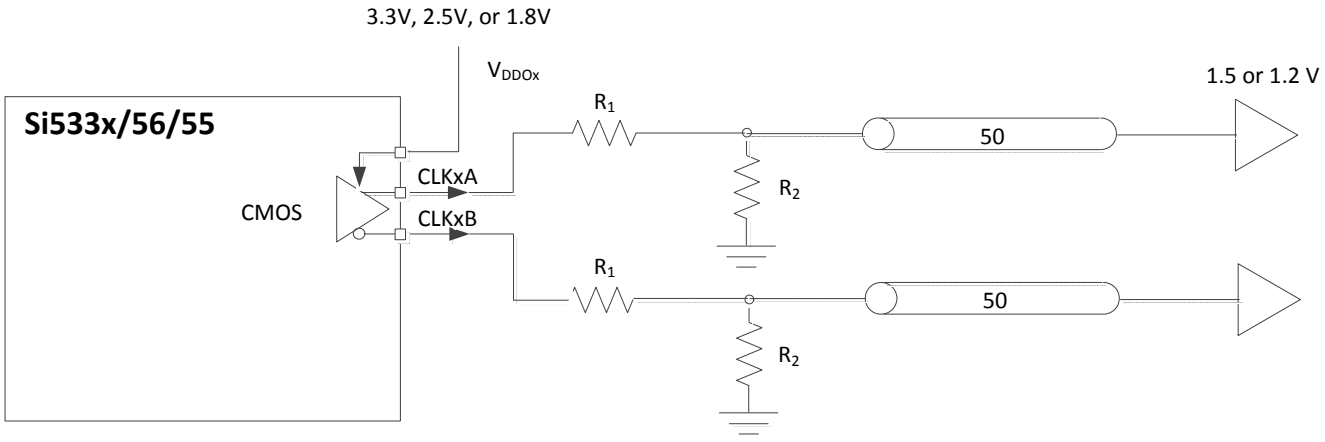


Figure 13. Interfacing to a 1.5 or 1.2 V CMOS Receiver

Table 1. Resistor Values for Interfacing to 1.5 and 1.2 V Receivers

	1.2 V CMOS Output		1.5 V CMOS Output	
VDDOx	**R1**	**R2**	**R1**	**R2**
1.8 V	25 Ω	150 Ω	10 Ω	300 Ω
2.5 V	55 Ω	100 Ω	33 Ω	125 Ω
3.3 V	90 Ω	80 Ω	60 Ω	90 Ω

The resistor values in Table 1 were selected to maintain signal integrity, specifically rise/fall time, at the cost of current consumption. The increase in current consumption is expected to be on the order of 2 to 8 mA per output depending on VDDOx, 4 mA max with VDDOx of 1.8 V.

3.2. SSTL and HSTL Outputs

The Si533x supports both SSTL and HSTL outputs, which can be single-ended or differential. The recommended termination scheme for SSTL is shown in Figure 14. The V_{TT} supply can be generated using a simple voltage divider as shown below.

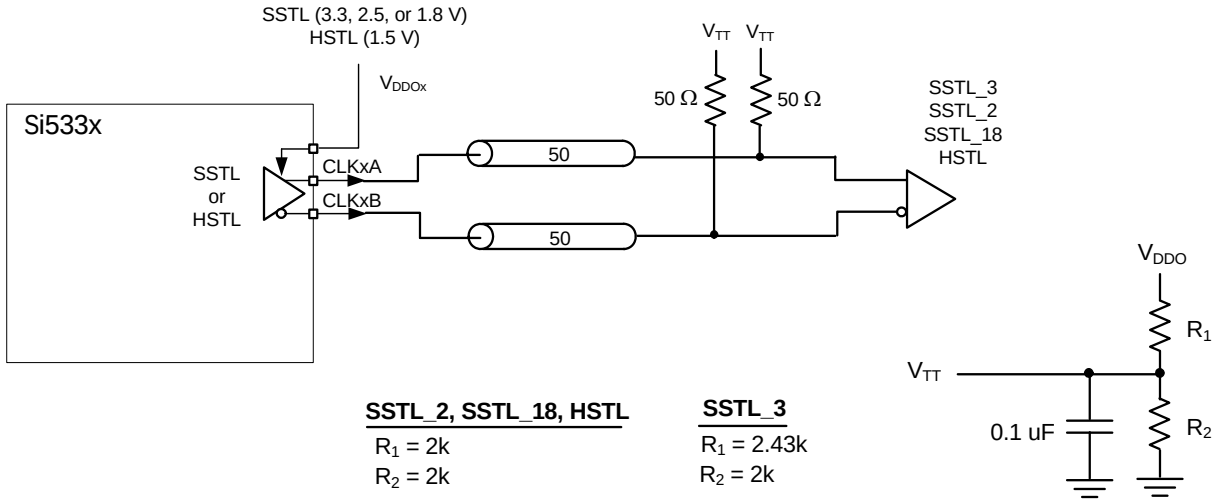


Figure 14. Interfacing the Si533x to an SSTL or HSTL Receiver

3.3. LVPECL Outputs

The LVPECL driver is configurable in both 3.3 V or 2.5 V standard LVPECL modes. The output driver can be ac-coupled or dc-coupled to the receiver.

3.3.1. DC-Coupled LVPECL Outputs

The standard LVPECL driver supports two commonly used dc-coupled configurations. Both of these are shown in Figure 15. LVPECL drivers were designed to be terminated with 50 Ω to VDD–2 V, which is illustrated in Figure 15a. V_{TT} can be supplied with a simple voltage divider as shown in Figure 15.

An alternative method of terminating LVPECL is shown in Figure 15b, which is the Thevenin equivalent to the termination in Figure 15a. It provides a 50 Ω load terminated to V_{DD}–2.0 V. For 3.3 V LVPECL, use R_1 = 127 Ω and R_2 = 82.5 Ω; for 2.5 V LVPECL, use R_1 = 250 Ω and R_2 = 62.5 Ω. The only disadvantage to this type of termination is that the Thevenin circuit consumes additional power from the V_{DDO} supply.

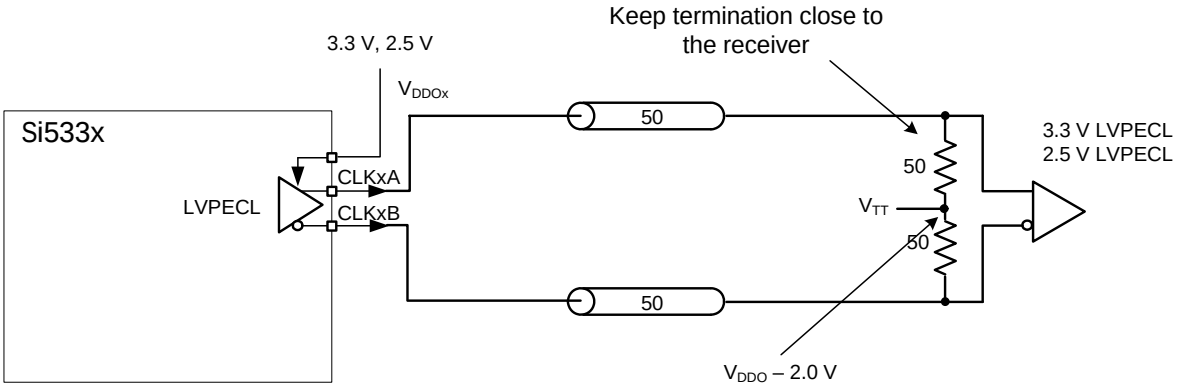


Figure 14a—DC Coupled Termination of 50 Ohms to V_{DD} – 2.0 V

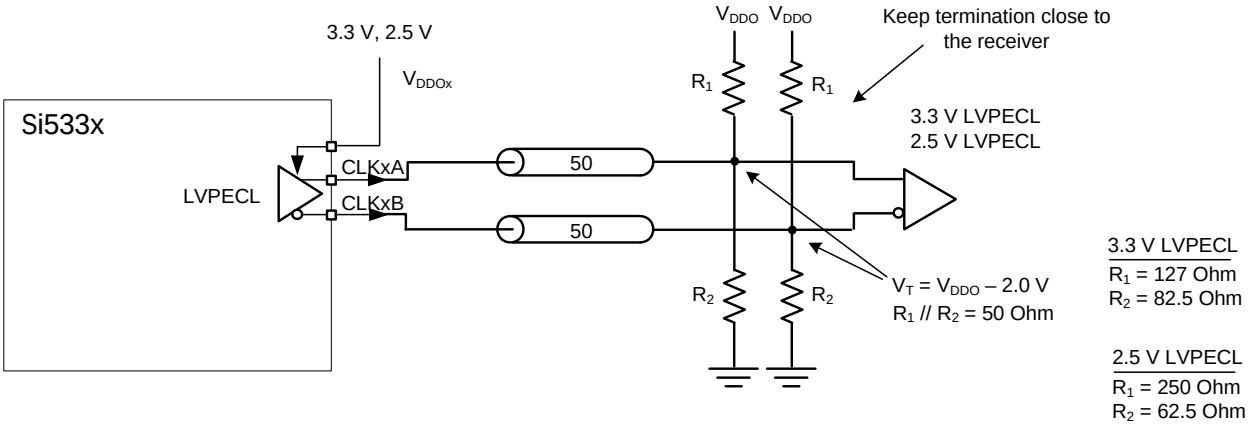


Figure 14b—DC Coupled with Thevenin Termination

Figure 15. Interfacing the Si533x to an LVPECL Receiver Using DC Coupling

3.3.2. AC Coupled LVPECL Outputs

AC coupling is necessary when a receiver and a driver have compatible voltage swings but different common-mode voltages. AC coupling works well for dc-balanced signals, such as for 50% duty cycle clocks. Figure 16 describes two methods for ac coupling the standard LVPECL driver. The Thevenin termination shown in Figure 16a is a convenient and common approach when a V_{BB} (V_{DD} – 1.3 V) supply is not available; however, it does consume additional power. The termination method shown in Figure 16b consumes less power. A V_{BB} supply can be generated from a simple voltage divider circuit as shown in Figure 16.

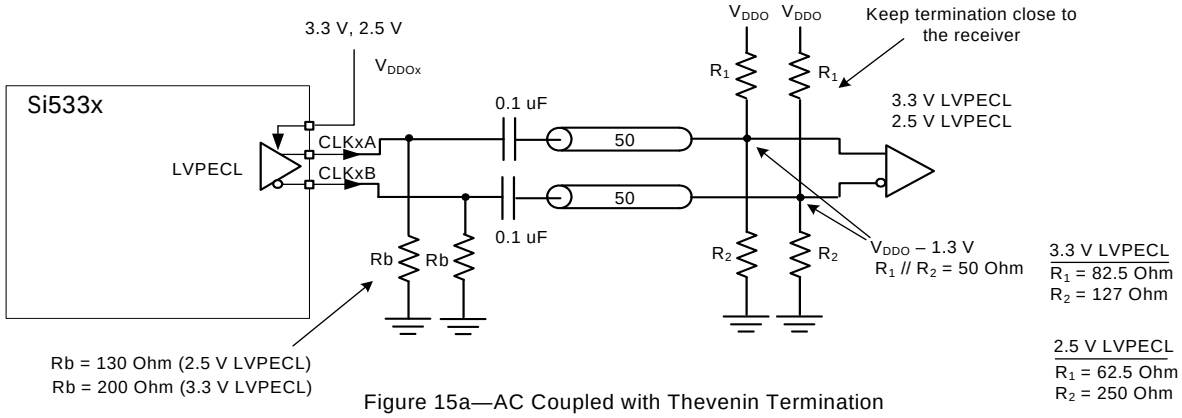


Figure 15a—AC Coupled with Thevenin Termination

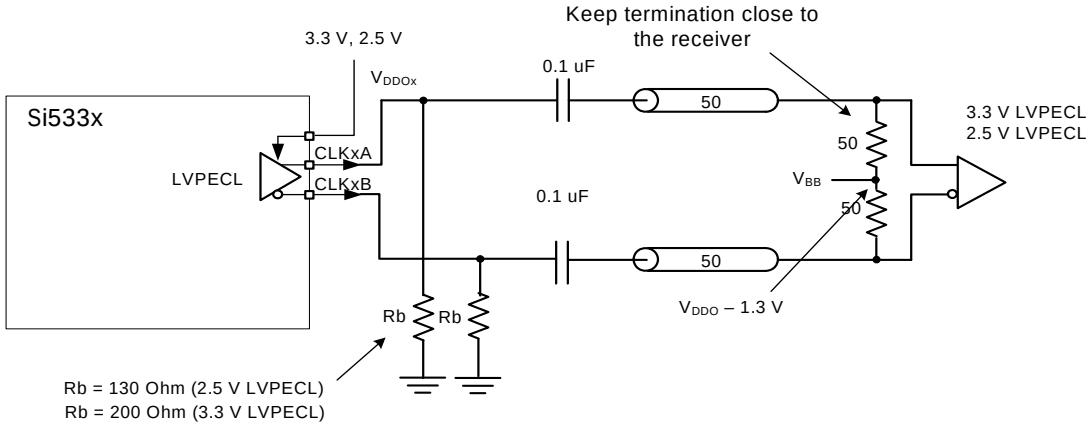


Figure 15b—AC Coupled with 100 Ohm Termination

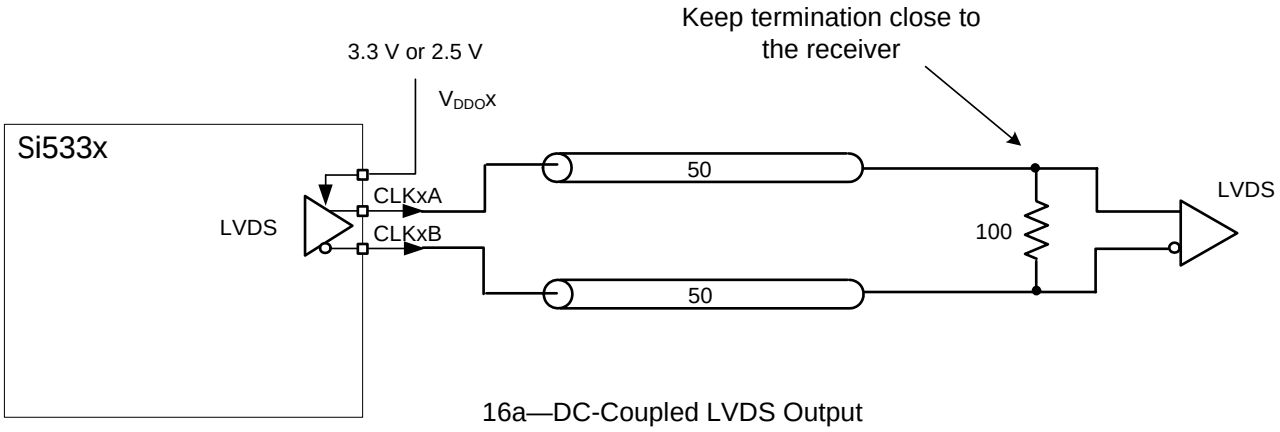
Figure 16. Interfacing to an LVPECL Receiver Using AC Coupling

3.4. LVDS Outputs

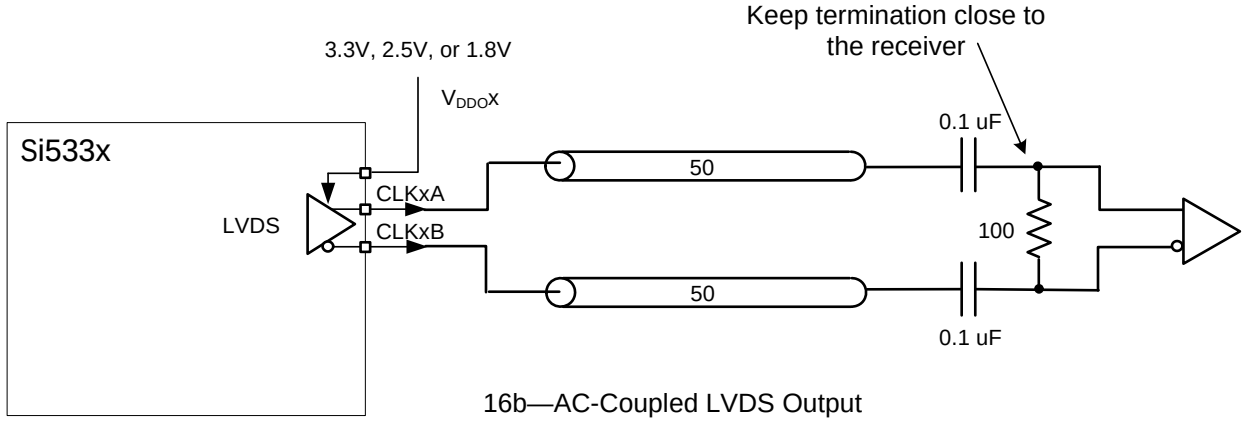
The LVDS output option provides a very simple and power-efficient interface that requires no external biasing when connected to an LVDS receiver. An ac-coupled LVDS driver is often useful as a CML driver. The LVDS driver may be dc-coupled or ac-coupled to the receiver in 3.3 V or 2.5 V output mode.

3.4.1. AC-Coupled LVDS Outputs

The Si5338/34 LVDS output can drive an ac-coupled load. The Si5330 LVDS output can only drive an ac-coupled load if the input to the Si5330 has a very well-controlled duty cycle like any Silicon Labs PLL clock products. The ac coupling capacitors may be placed at either the driver or receiver end, as long as they are placed prior to the 100 Ω termination resistor. Keep the 100 Ω termination resistor as close to the receiver as possible, as shown in Figure 17. When a 1.8 V output supply voltage is used, the LVDS output of the Si533x produces a common-mode voltage of ~0.875 V, which does not support the LVDS standard. In this case, it is best to ac-couple the output to the load.



16a—DC-Coupled LVDS Output



16b—AC-Coupled LVDS Output

Figure 17. Interfacing to an LVDS Receiver

3.5. HCSL Outputs

Host clock signal level (HCSL) outputs are commonly used in PCI Express applications. A typical HCSL driver has an open source output that requires an external series resistor and a resistor to ground. The Si533x HCSL driver has integrated these resistors to simplify the interface to an HCSL receiver. No external components are necessary when connecting the Si533x HCSL driver to an HCSL receiver.

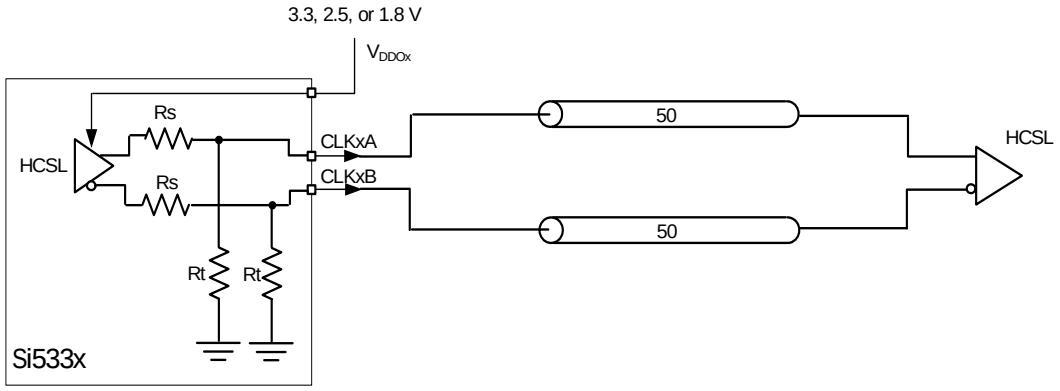


Figure 18. Interfacing the Si533x to an HCSL Receiver

3.6. CML Outputs

The Si5338 has a CML driver option. This driver can be used to replace an LVPECL driver in ac-coupled applications and save ~15 mA for each output driver in the process. When using the CML driver, no external bias resistors from the CML outputs to ground or Vtt should be connected. The CML driver is compliant with LVPECL peak-peak output levels; however, the common-mode output voltage is not compliant to LVPECL specs. The CML driver is individually available for all four differential outputs. See Section 9 of "AN411: Configuring the Si5338 without ClockBuilder Desktop" for information on selecting the CML Driver option. The CML output driver option should only be used when the output clock signal comes from an internal MultiSynth.

The Si5338 CML output driver can be used as long as the following conditions are met:

1. Both pins of the differential output pair are ac coupled to the load.
2. The load at the receiver is effectively 100 Ω differential.
3. The Si5338 PLL is not bypassed.
4. The VDDOx supply for the CML driver voltage is 3.3 V or 2.5 V.

The CML driver has the same specified output voltage swing as the LVPECL driver.

1. Max Vsepp = .95 V
2. Min Vsepp = .55 V
3. Typ Vsepp = .8 V

Figure 19 shows the normal connection for the Si5338 CML Driver format. Figure 20 shows the expected termination for the Si5338 CML driver. This termination is most often within a CML receiver.

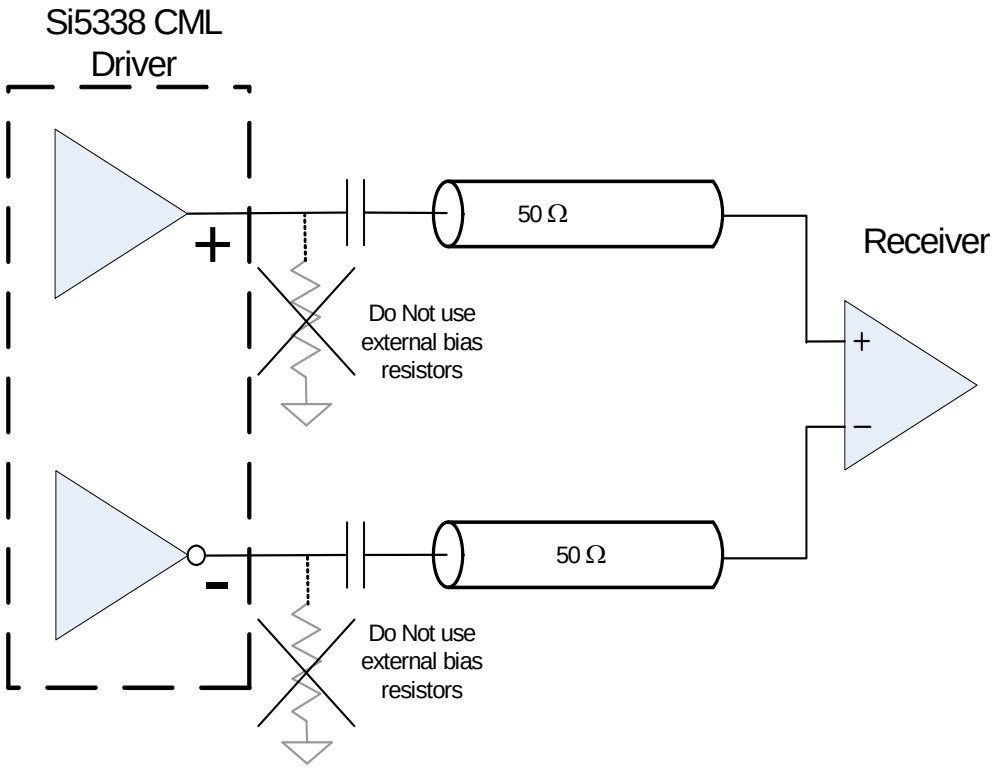


Figure 19. CML Driver Connection

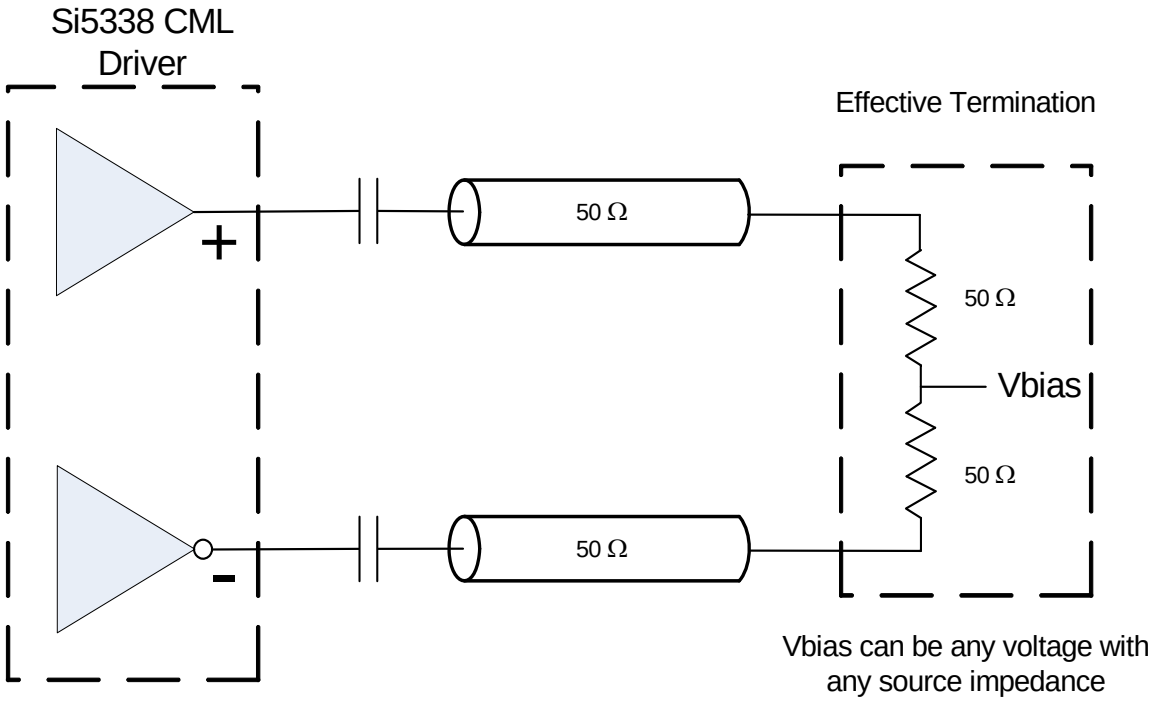
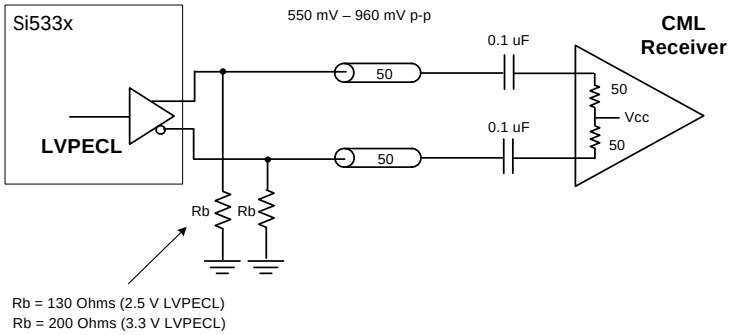


Figure 20. Terminations for Si5338 CML Driver

3.7. Interfacing the Si533x LVDS/LVPECL to a CML Receiver

Current mode logic (CML) is transmitted differentially and terminated to 50 Ω to Vcc as shown in Figure 21. A CML receiver can be driven with either an LVPECL or an LVDS output depending on the signal swing required by the receiver. A single-ended output swing from 550 mV to 960 mV is achieved when driving a CML receiver with an LVPECL output. For a reduced output swing, LVDS mode is recommended for producing a single-ended swing between 250 mV and 450 mV.

Driving a CML Receiver Using the LVPECL Output



Driving a CML Receiver Using the LVDS Output

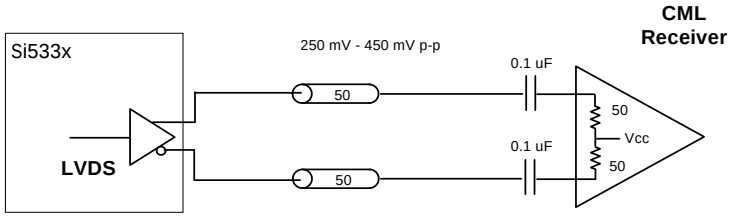


Figure 21. Terminating an LVPECL or an LVDS Output to a CML Receiver

DOCUMENT CHANGE LIST

Revision 0.3 to 0.4

- Updated Section 3.5.

Revision 0.4 to 0.5

- Updated Figure 10 on page 8.
  - Updated resistor values.
- Updated "2.2.4. Applying CMOS Level Signal to Differential Inputs" on page 8.
  - Added text to recomend max CMOS input frequency into a differential input.
- Updated "2.1.2. Single-Ended SSTL and HSTL Inputs" on page 4 and "2.1.3. Applying a Single-Ended Signal to a Differential Input" on page 5 to specify a max input frequency of 350 MHz.
- Removed R1 and R2 and 0.1 µf cap from Figures 15 and 16.
- Added maximum input frequency of 350 MHz to "2.1.2. Single-Ended SSTL and HSTL Inputs" on page 4 and "2.1.3. Applying a Single-Ended Signal to a Differential Input" on page 5.
- Added "3.6. CML Outputs" on page 15.
- Added "3.1.1. 1.5 and 1.2 V CMOS Outputs" on page 10.

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