80V V_{IN} and V_{OUT} Synchronous 4-Switch Buck-Boost DC/DC Controller

FEATURES

- **Single Inductor Allows V_{IN} Above, Below, or Equal to Regulated V_{OUT}**
- **V_{IN} Range 2.8V (Need $EXTV_{CC}$ > 6.4V) to 80V**
- **V_{OUT} Range: 1.3V to 80V**
- **Quad N-Channel MOSFET Gate Drivers**
- **Synchronous Rectification: Up to 98% Efficiency**
- **Input and Output Current Monitor Pins**
- **Synchronizable Fixed Frequency: 100kHz to 400kHz**
- **Integrated Input Current, Input Voltage, Output Current and Output Voltage Feedback Loops**
- Clock Output Usable To Monitor Die Temperature
- Available in 38-Lead (5mm × 7mm) QFN and TSSOP Packages with the TSSOP Modified for Improved High Voltage Operation

APPLICATIONS

- High Voltage Buck-Boost Converters
- Input or Output Current Limited Converters

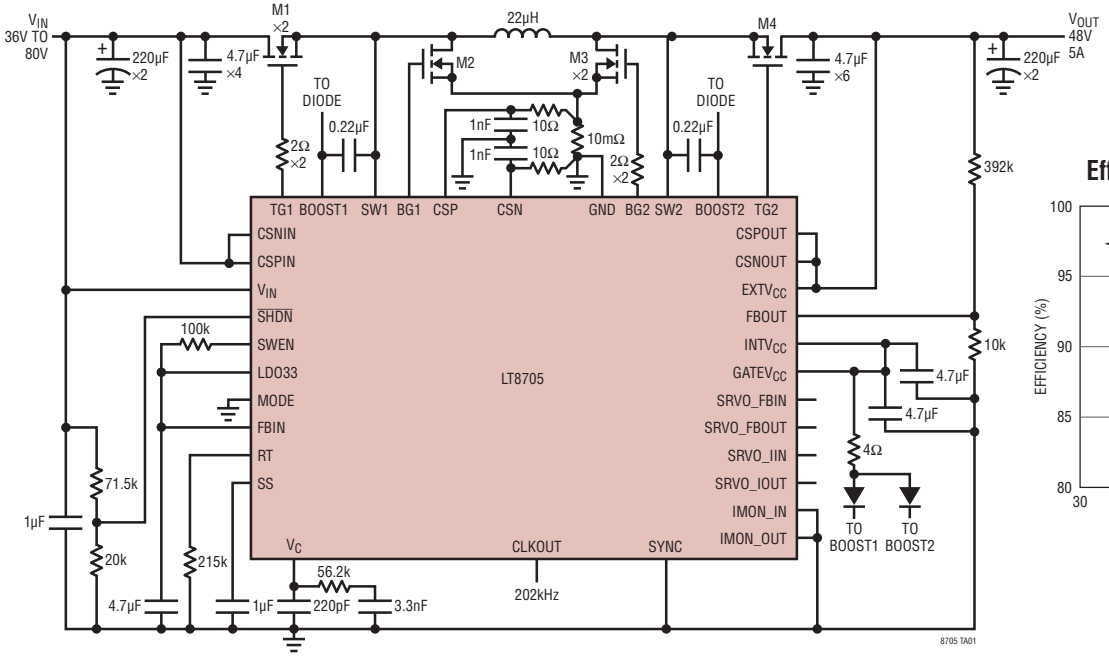
DESCRIPTION

The LT®8705 is a high performance buck-boost switching regulator controller that operates from input voltages above, below or equal to the output voltage. The part has integrated input current, input voltage, output current and output voltage feedback loops. With a wide 2.8V to 80V input and 1.3V to 80V output range, the LT8705 is compatible with most solar, automotive, telecom and battery-powered systems.

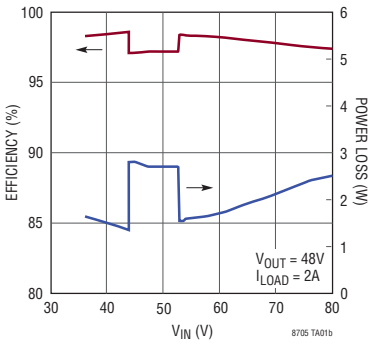
The LT8705 includes servo pins to indicate which feedback loops are active. The MODE pin selects among Burst Mode® operation, discontinuous or continuous conduction mode at light loads. Additional features include a 3.3V/12mA LDO, a synchronizable fixed operating frequency, onboard gate drivers, adjustable UVLO, along with input and output current monitoring with programmable maximum levels.

TYPICAL APPLICATION

Telecom Voltage Stabilizer



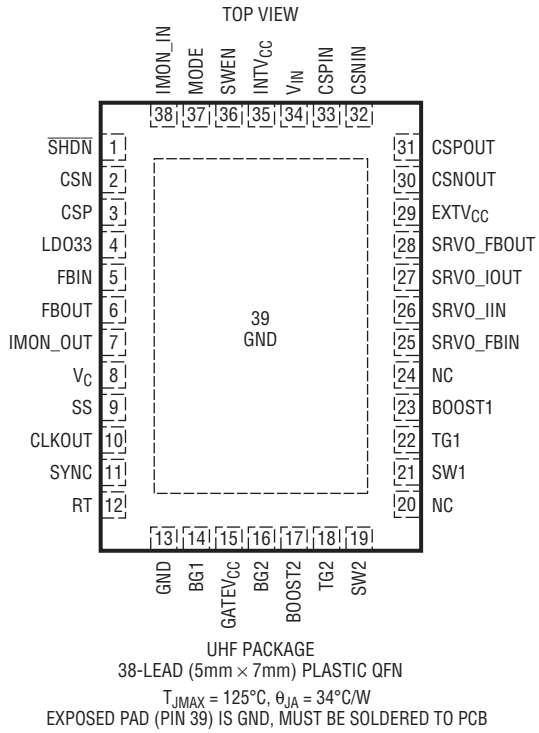
Efficiency and Power Loss



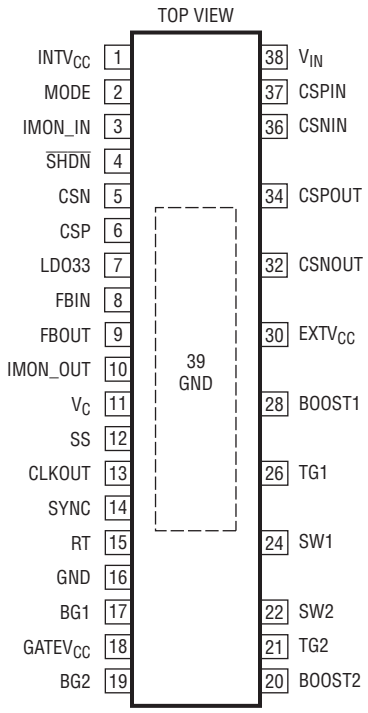
ABSOLUTE MAXIMUM RATINGS (Note 1)

V_{CSP}-V_{CSN}, V_{CSPIN}-V_{CSNIN}, V_{CSPOUT}-V_{CSNOUT} ..... –0.3V to 0.3V
SS, CLKOUT, CSP, CSN Voltage ..... –0.3V to 3V
V_C Voltage (Note 2) ..... –0.3V to 2.2V
RT, LDO33, FBOUT Voltage ..... –0.3V to 5V
IMON_IN, IMON_OUT Voltage ..... –0.3V to 5V
SYNC Voltage ..... –0.3V to 5.5V
$INTV_{CC}$, $GATEV_{CC}$ Voltage ..... –0.3V to 7V
V_{BOOST1}-V_{SW1}, V_{BOOST2}-V_{SW2} ..... –0.3V to 7V
SWEN, MODE Voltage ..... –0.3V to 7V
SRVO_FBIN, SRVO_FBOUT Voltage ..... –0.3V to 30V
SRVO_IIN, SRVO_IOUT Voltage ..... –0.3V to 30V
FBIN, $\overline{SHDN}$ Voltage ..... –0.3V to 30V
CSNIN, CSPIN, CSPOUT, CSNOUT Voltage .. –0.3V to 80V
V_{IN}, $EXTV_{CC}$ Voltage ..... –0.3V to 80V
SW1, SW2 Voltage ..... 81V (Note 7)
BOOST1, BOOST2 Voltage ..... –0.3V to 87V
BG1, BG2, TG1, TG2 ..... (Note 6)
Operating Junction Temperature Range
LT8705E (Notes 3, 8) ..... –40°C to 125°C
LT8705I (Notes 3, 8) ..... –40°C to 125°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)
FE Package ..... 300°C

PIN CONFIGURATION



UHF PACKAGE
38-LEAD (5mm × 7mm) PLASTIC QFN
T_{JMAX} = 125°C, θ_{JA} = 34°C/W
EXPOSED PAD (PIN 39) IS GND, MUST BE SOLDERED TO PCB



FE PACKAGE
VARIATION: FE38(31)
38-LEAD PLASTIC TSSOP
T_{JMAX} = 125°C, θ_{JA} = 25°C/W
EXPOSED PAD (PIN 39) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT8705EUHF#PBF	LT8705EUHF#TRPBF	8705	38-Lead (5mm × 7mm) Plastic QFN	–40°C to 125°C
LT8705IUHF#PBF	LT8705IUHF#TRPBF	8705	38-Lead (5mm × 7mm) Plastic QFN	–40°C to 125°C
LT8705EFE#PBF	LT8705EFE#TRPBF	LT8705FE	38-Lead Plastic TSSOP	–40°C to 125°C
LT8705IFE#PBF	LT8705IFE#TRPBF	LT8705FE	38-Lead Plastic TSSOP	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 12V, $\overline{SHDN}$ = 3V unless otherwise noted. (Note 3)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Voltage Supplies and Regulators						
V_{IN} Operating Voltage Range	$EXTV_{CC}$ = 0V $EXTV_{CC}$ = 7.5V	● ●	5.5 2.8		80 80	V V
V_{IN} Quiescent Current	Not Switching, V_{EXTVCC} = 0			2.65	4.2	mA
V_{IN} Quiescent Current in Shutdown	$V_{\overline{SHDN}}$ = 0V			0	1	µA
$EXTV_{CC}$ Switchover Voltage	I_{INTVCC} = 20mA, V_{EXTVCC} Rising	●	6.15	6.4	6.6	V
$EXTV_{CC}$ Switchover Hysteresis				0.18		V
$INTV_{CC}$ Current Limit	Maximum Current Draw from $INTV_{CC}$ and LDO33 Pins Combined. Regulated from V_{IN} or $EXTV_{CC}$ (12V) $INTV_{CC}$ = 5.25V $INTV_{CC}$ = 4.5V	 ● ●	 90 28	 127 42	 165 55	 mA mA
$INTV_{CC}$ Voltage	Regulated from V_{IN}, I_{INTVCC} = 20mA Regulated from $EXTV_{CC}$ (12V), I_{INTVCC} = 20mA	● ●	6.15 6.15	6.35 6.35	6.55 6.55	V V
$INTV_{CC}$ Load Regulation	I_{INTVCC} = 0mA to 50mA			–0.5	–1.5	%
$INTV_{CC}$, $GATEV_{CC}$ Undervoltage Lockout	$INTV_{CC}$ Falling, $GATEV_{CC}$ Connected to $INTV_{CC}$	●	4.45	4.65	4.85	V
$INTV_{CC}$, $GATEV_{CC}$ Undervoltage Lockout Hysteresis	$GATEV_{CC}$ Connected to $INTV_{CC}$			160		mV
$INTV_{CC}$ Regulator Dropout Voltage	V_{IN}-V_{INTVCC}, I_{INTVCC} = 20mA			245		mV
LDO33 Pin Voltage	5mA from LDO33 Pin	●	3.23	3.295	3.35	V
LDO33 Pin Load Regulation	I_{LDO33} = 0.1mA to 5mA			–0.25	–1	%
LDO33 Pin Current Limit		●	12	17.25	22	mA
LDO33 Pin Undervoltage Lockout	LDO33 Falling		2.96	3.04	3.12	V
LDO33 Pin Undervoltage Lockout Hysteresis				35		mV
Switching Regulator Control						
Maximum Current Sense Threshold (V_{CSP} – V_{CSN})	Boost Mode, Minimum M3 Switch Duty Cycle	●	102	117	132	mV
Maximum Current Sense Threshold (V_{CSN} – V_{CSP})	Buck Mode, Minimum M2 Switch Duty Cycle	●	69	86	102	mV
Gain from V_C to Maximum Current Sense Voltage (V_{CSP}-V_{CSN}) (A5 in the Block Diagram)	Boost Mode Buck Mode			150 –150		mV/V mV/V
$\overline{SHDN}$ Input Voltage High	$\overline{SHDN}$ Rising to Enable the Device	●	1.184	1.234	1.284	V
$\overline{SHDN}$ Input Voltage High Hysteresis				50		mV
$\overline{SHDN}$ Input Voltage Low	Device Disabled, Low Quiescent Current	●			0.35	V

ELECTRICAL CHARACTERISTICS

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PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$\overline{SHDN}$ Pin Bias Current	$V_{\overline{SHDN}}$ = 3V $V_{\overline{SHDN}}$ = 12V			0 11	1 22	µA µA
SWEN Rising Threshold Voltage (Note 5)		●	1.156	1.206	1.256	V
SWEN Threshold Voltage Hysteresis (Note 5)				22		mV
MODE Pin Forced Continuous Mode Threshold		●	0.4			V
MODE Pin Burst Mode Range		●	1.0		1.7	V
MODE Pin Discontinuous Mode Threshold		●			2.3	V
Soft-Start Charging Current	V_{SS} = 0.5V		13	19	25	µA
Soft-Start Discharge Current	V_{SS} = 0.5V			9.5		µA
Voltage Regulator Loops (Refer to Block Diagram to Locate Amplifiers)						
Regulation Voltage for FBOUT	V_C = 1.2V	●	1.193	1.207	1.222	V
Regulation Voltage for FBIN	V_C = 1.2V	●	1.184	1.205	1.226	V
Line Regulation for FBOUT and FBIN Error Amp Reference Voltage	V_{IN} = 12V to 80V			0.002	0.005	%/V
FBOUT Pin Bias Current	Current Out of Pin			15		nA
FBOUT Error Amp EA4 g_m				315		µmho
FBOUT Error Amp EA4 Voltage Gain				220		V/V
FBIN Pin Bias Current	Current Out of Pin			10		nA
FBIN Error Amp EA3 g_m				130		µmho
FBIN Error Amp EA3 Voltage Gain				90		V/V
SRVO_FBIN Activation Threshold (Note 5)	(V_{FBIN} Falling) – (Regulation Voltage for FBIN), V_{FBOUT} = V_{IMON_IN} = V_{IMON_OUT} = 0V		56	72	89	mV
SRVO_FBIN Activation Threshold Hysteresis (Note 5)	V_{FBOUT} = V_{IMON_IN} = V_{IMON_OUT} = 0V			33		mV
SRVO_FBOUT Activation Threshold (Note 5)	(V_{FBOUT} Rising) – (Regulation Voltage for FBOUT), V_{FBIN} = 3V, V_{IMON_IN} = V_{IMON_OUT} = 0V		–37	–29	–21	mV
SRVO_FBOUT Activation Threshold Hysteresis (Note 5)	V_{FBIN} = 3V, V_{IMON_IN} = 0V, V_{IMON_OUT} = 0V			15		mV
SRVO_FBIN, SRVO_FBOUT Low Voltage (Note 5)	I = 100µA	●		110	330	mV
SRVO_FBIN, SRVO_FBOUT Leakage Current (Note 5)	V_{SRVO_FBIN} = V_{SRVO_FBOUT} = 2.5V	●		0	1	µA
Current Regulation Loops (Refer to Block Diagram to Locate Amplifiers)						
Regulation Voltages for IMON_IN and IMON_OUT	V_C = 1.2V	●	1.187	1.208	1.229	V
Line Regulation for IMON_IN and IMON_OUT Error Amp Reference Voltage	V_{IN} = 12V to 80V			0.002	0.005	%/V
CSPIN, CSNIN Bias Current	BOOST Capacitor Charge Control Block Not Active I_{CSPIN} + I_{CSNIN}, V_{CSPIN} = V_{CSNIN} = 12V			31		µA
CSPIN, CSNIN Common Mode Operating Voltage Range		●	1.5		80	V
CSPIN, CSNIN Differential Operating Voltage Range		●	–100		100	mV
$V_{CSPIN-CSNIN}$ to IMON_IN Amplifier A7 g_m	V_{CSPIN} – V_{CSNIN} = 50mV, V_{CSPIN} = 5.025V	 ●	0.95 0.94	1 1	1.05 1.06	mmho mmho
IMON_IN Maximum Output Current		●	100			µA
IMON_IN Overvoltage Threshold		●	1.55	1.61	1.67	V
IMON_IN Error Amp EA2 g_m				185		µmho
IMON_IN Error Amp EA2 Voltage Gain				130		V/V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 12V, $\overline{SHDN}$ = 3V unless otherwise noted. (Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
CSPOUT, CSNOUT Bias Current	BOOST Capacitor Charge Control Block Not Active I_{CSPOUT} + I_{CSNOUT}, V_{CSPOUT} = V_{CSNOUT} = 12V I_{CSPOUT} + I_{CSNOUT}, V_{CSPOUT} = V_{CSNOUT} = 1.5V			 45 4		 µA µA
CSPOUT, CSNOUT Common Mode Operating Voltage Range		●	0		80	V
CSPOUT, CSNOUT Differential Mode Operating Voltage Range		●	–100		100	mV
$V_{CSPOUT-CSNOUT}$ to IMON_OUT Amplifier A6 g_m	V_{CSPOUT} – V_{CSNOUT} = 50mV, V_{CSPOUT} = 5.025V V_{CSPOUT} – V_{CSNOUT} = 50mV, V_{CSPOUT} = 5.025V V_{CSPOUT} – V_{CSNOUT} = 5mV, V_{CSPOUT} = 5.0025V V_{CSPOUT} – V_{CSNOUT} = 5mV, V_{CSPOUT} = 5.0025V	 ● ●	0.95 0.94 0.65 0.55	1 1 1 1	1.05 1.085 1.35 1.6	mmho mmho mmho mmho
IMON_OUT Maximum Output Current		●	100			µA
IMON_OUT Overvoltage Threshold		●	1.55	1.61	1.67	V
IMON_OUT Error Amp EA1 g_m				185		µmho
IMON_OUT Error Amp EA1 Voltage Gain				130		V/V
SRVO_IIN Activation Threshold (Note 5)	(V_{IMON_IN} Rising) – (Regulation Voltage for IMON_IN), V_{FBIN} = 3V, V_{FBOUT} = 0V, V_{IMON_OUT} = 0V		–60	–49	–37	mV
SRVO_IIN Activation Threshold Hysteresis (Note 5)	V_{FBIN} = 3V, V_{FBOUT} = 0V, V_{IMON_OUT} = 0V			22		mV
SRVO_IOUT Activation Threshold (Note 5)	(V_{IMON_OUT} Rising) – (Regulation Voltage for IMON_OUT), V_{FBIN} = 3V, V_{FBOUT} = 0V, V_{IMON_IN} = 0V		–62	–51	–39	mV
SRVO_IOUT Activation Threshold Hystersis (Note 5)	V_{FBIN} = 3V, V_{FBOUT} = 0V, V_{IMON_IN} = 0V			22		mV
SRVO_IIN, SRVO_IOUT Low Voltage (Note 5)	I = 100µA	●		110	330	mV
SRVO_IIN, SRVO_IOUT Leakage Current (Note 5)	V_{SRVO_IIN} = V_{SRVO_IOUT} = 2.5V	●		0	1	µA
NMOS Gate Drivers						
TG1, TG2 Rise Time	C_{LOAD} = 3300pF (Note 4)			20		ns
TG1, TG2 Fall Time	C_{LOAD} = 3300pF (Note 4)			20		ns
BG1, BG2 Rise Time	C_{LOAD} = 3300pF (Note 4)			20		ns
BG1, BG2 Fall Time	C_{LOAD} = 3300pF (Note 4)			20		ns
TG1 Off to BG1 On Delay	C_{LOAD} = 3300pF Each Driver			100		ns
BG1 Off to TG1 On Delay	C_{LOAD} = 3300pF Each Driver			80		ns
TG2 Off to BG2 On Delay	C_{LOAD} = 3300pF Each Driver			100		ns
BG2 Off to TG2 On Delay	C_{LOAD} = 3300pF Each Driver			80		ns
Minimum On-Time for Main Switch in Boost Operation ($t_{ON(M3,MIN)}$)	Switch M3, C_{LOAD} = 3300pF			265		ns
Minimum On-Time for Synchronous Switch in Buck Operation ($t_{ON(M2,MIN)}$)	Switch M2, C_{LOAD} = 3300pF			260		ns
Minimum Off-Time for Main Switch in Steady-State Boost Operation	Switch M3, C_{LOAD} = 3300pF			245		ns
Minimum Off-Time for Synchronous Switch in Steady-State Buck Operation	Switch M2, C_{LOAD} = 3300pF			245		ns
Oscillator						
Switch Frequency Range	SYNCing or Free Running		100		400	kHz
Switching Frequency, f_{OSC}	R_T = 365k R_T = 215k R_T = 124K	● ● ●	102 170 310	120 202 350	142 235 400	kHz kHz kHz

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 12V, $\overline{SHDN}$ = 3V unless otherwise noted. (Note 3)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
SYNC High Level for Synchronization		●	1.3			V
SYNC Low Level for Synchronization		●			0.5	V
SYNC Clock Pulse Duty Cycle	V_{SYNC} = 0V to 2V		20		80	%
Recommended Minimum SYNC Ratio f_{SYNC}/f_{OSC}				3/4		
CLKOUT Output Voltage High	1mA Out of CLKOUT Pin		2.3	2.45	2.55	V
CLKOUT Output Voltage Low	1mA Into CLKOUT Pin			25	100	mV
CLKOUT Duty Cycle	T_J = –40°C T_J = 25°C T_J = 125°C			22.7 44.1 77		% % %
CLKOUT Rise Time	C_{LOAD} = 200pF			30		ns
CLKOUT Fall Time	C_{LOAD} = 200pF			25		ns
CLKOUT Phase Delay	SYNC Rising to CLKOUT Rising, f_{OSC} = 100kHz	●	160	180	200	Deg

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Do not force voltage on the V_C pin.

Note 3: The LT8705E is guaranteed to meet performance specifications from 0°C to 125°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LT8705I is guaranteed over the full –40°C to 125°C junction temperature range.

Note 4: Rise and fall times are measured using 10% and 90% levels. Delay times are measured using 50% levels.

Note 5: This specification not applicable in the FE38 package.

Note 6: Do not apply a voltage or current source to these pins. They must be connected to capacitive loads only, otherwise permanent damage may occur.

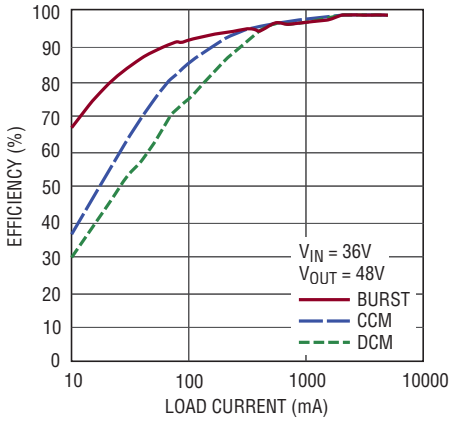
Note 7: Negative voltages on the SW1 and SW2 pins are limited, in an application, by the body diodes of the external NMOS devices, M2 and M3, or parallel Schottky diodes when present. The SW1 and SW2 pins are tolerant of these negative voltages in excess of one diode drop below ground, guaranteed by design.

Note 8: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed the maximum operating junction temperature when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

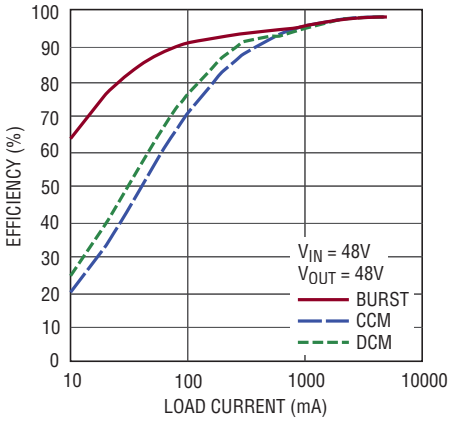
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C unless otherwise specified.

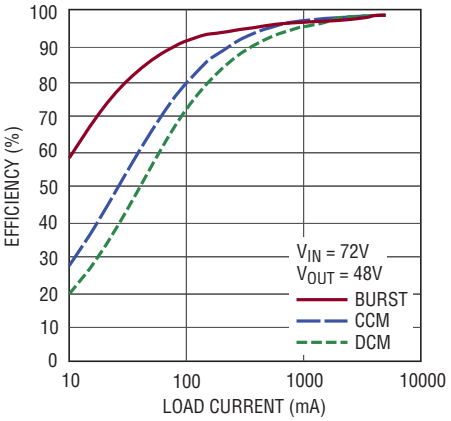
Efficiency vs Output Current (Boost Region-Figure 14)



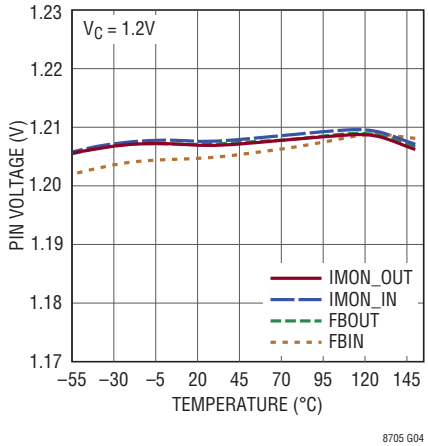
Efficiency vs Output Current (Buck-Boost Region-Figure 14)



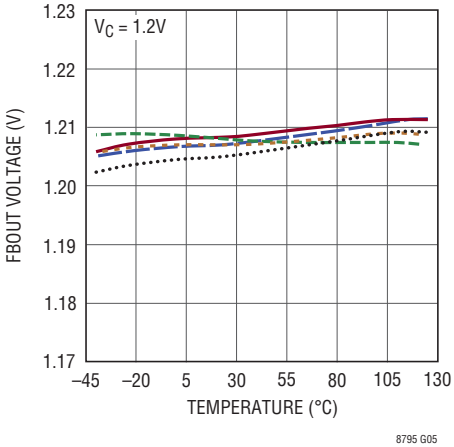
Efficiency vs Output Current (Buck Region-Figure 14)



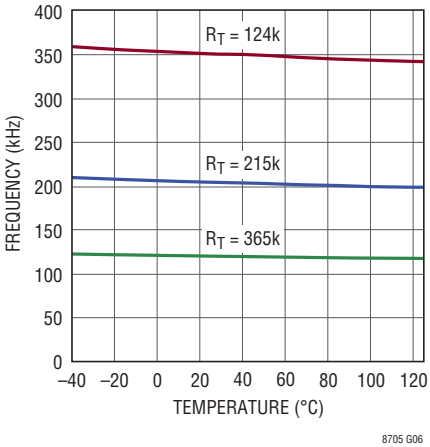
Feedback Voltages



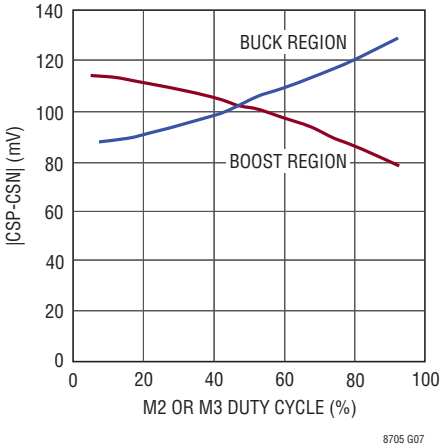
FBOUT Voltages (Five Parts)



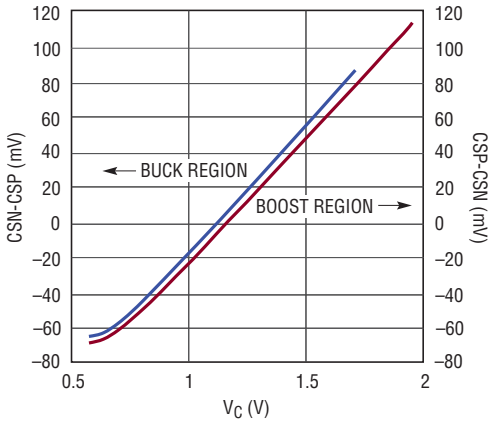
Oscillator Frequency



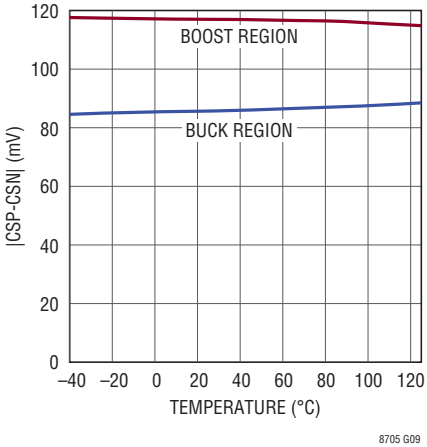
Maximum Inductor Current Sense Voltage vs Duty Cycle



Inductor Current Sense Voltage at Minimum Duty Cycle

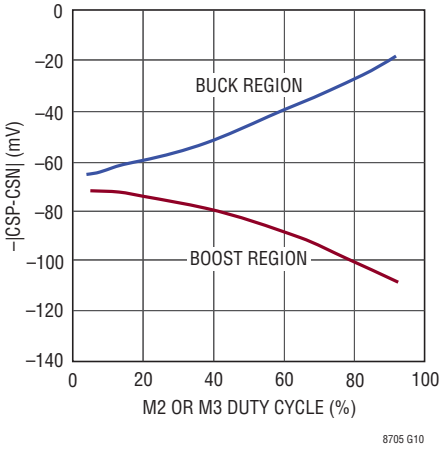


Maximum Inductor Current Sense Voltage at Minimum Duty Cycle

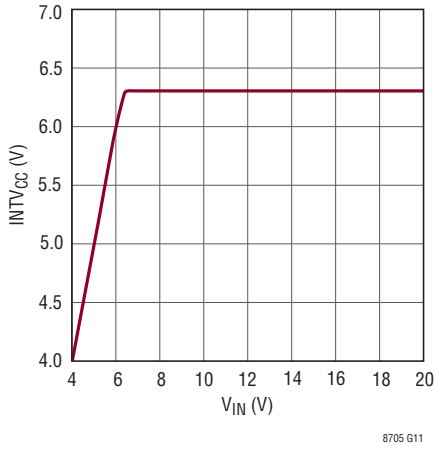


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C unless otherwise specified.

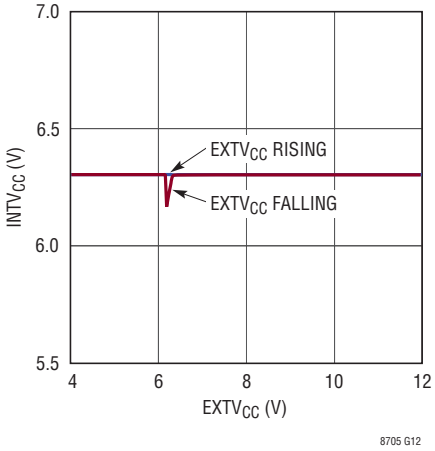
Minimum Inductor Current Sense Voltage in Forced Continuous Mode



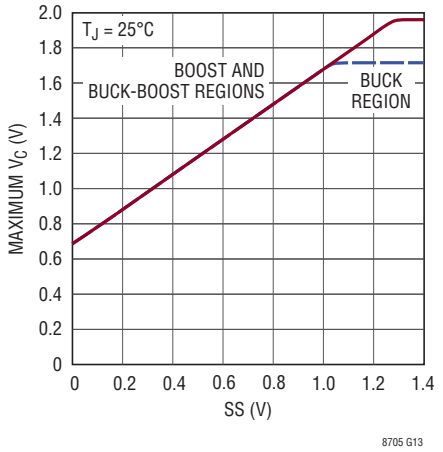
$INTV_{CC}$ Line Regulation ($EXTV_{CC}$ = 0V)



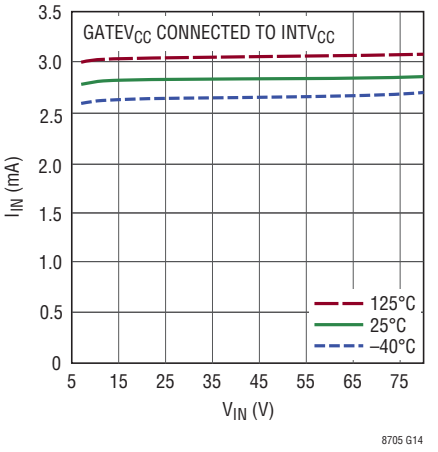
$INTV_{CC}$ Line Regulation (V_{IN} = 12V)



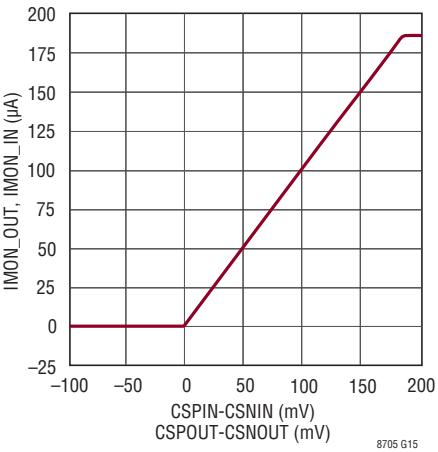
Maximum V_C vs SS



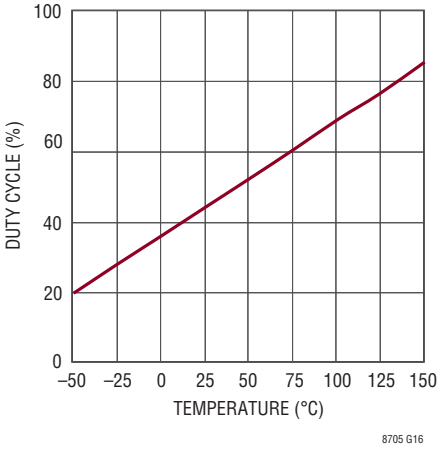
V_{IN} Supply Current vs Voltage (Not Switching)



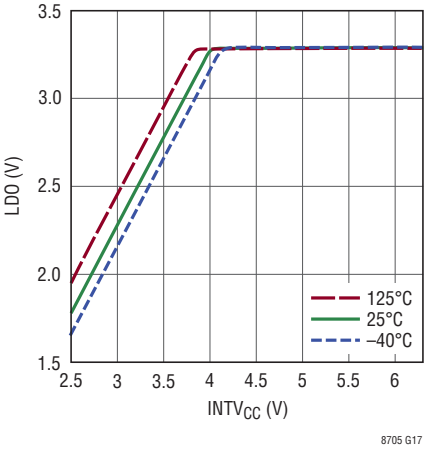
IMON Output Currents



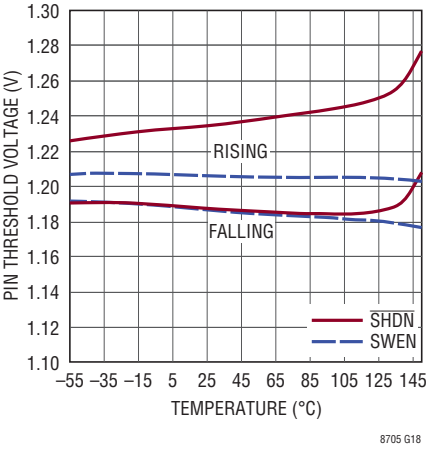
CLKOUT Duty Cycle



LDO33 Pin Regulation (I_{LDO33} = 1mA)



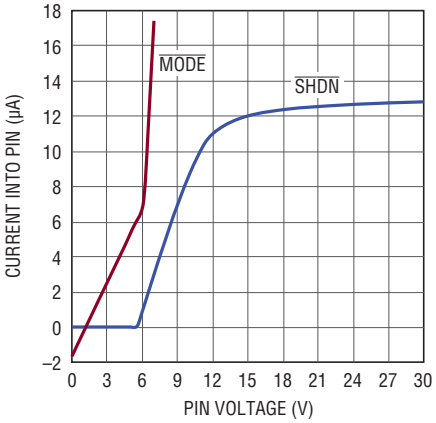
$\overline{SHDN}$ and SWEN Pin Thresholds vs Temperature



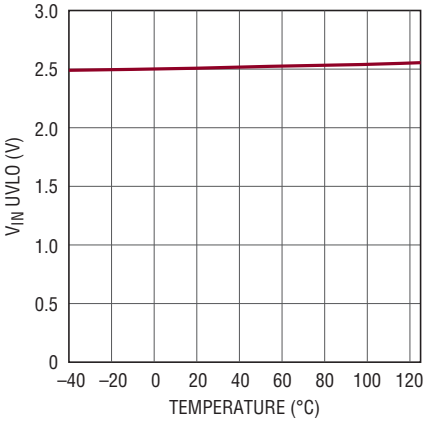
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C unless otherwise specified.

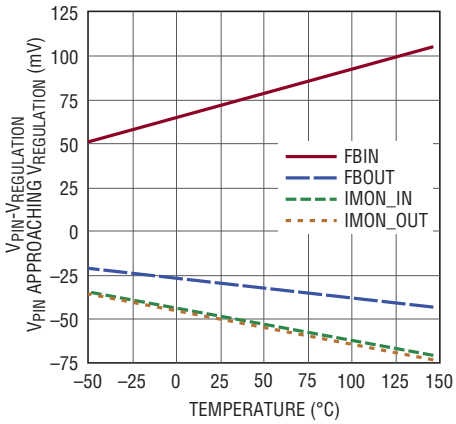
$\overline{SHDN}$ and MODE Pin Currents



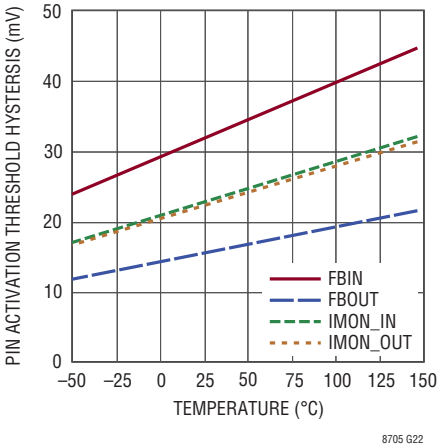
Internal V_{IN} UVLO



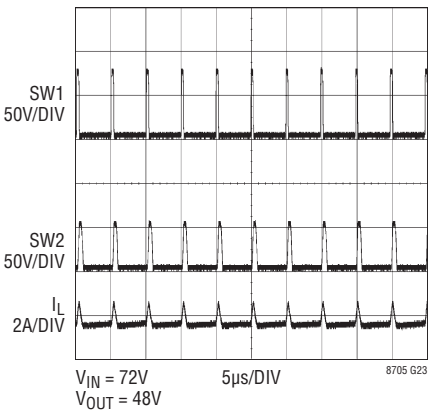
SRVO_xx Pin Activation Thresholds



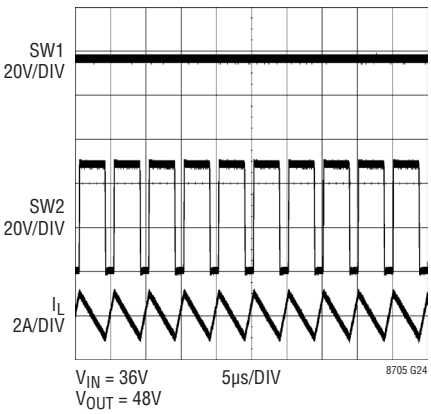
SRVO_xx Pin Activation Threshold Hysteresis



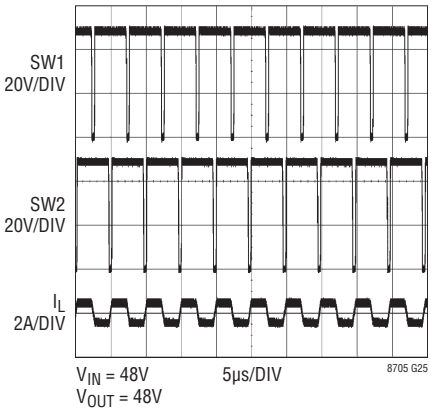
Discontinuous Mode (Figure 14)



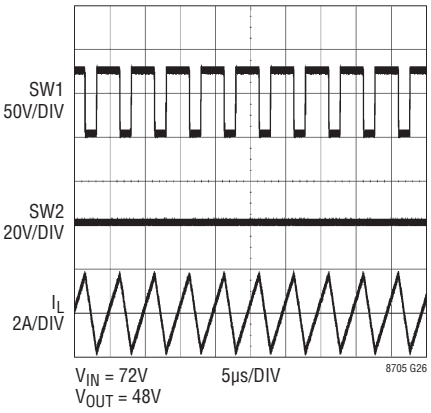
Forced Continuous Mode (Figure 14)



Forced Continuous Mode (Figure 14)

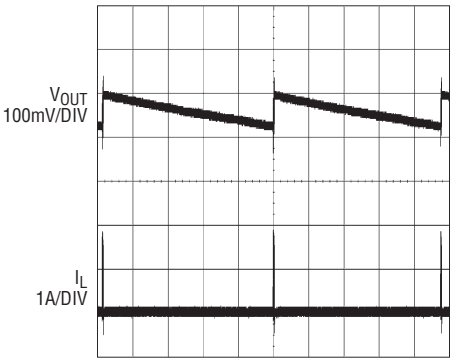


Forced Continuous Mode (Figure 14)

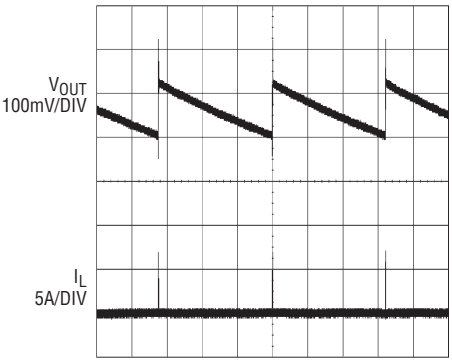


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C unless otherwise specified.

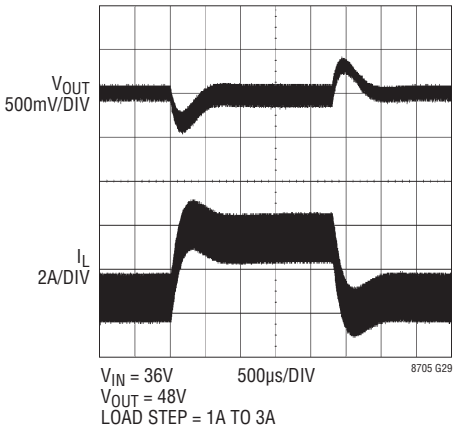
Burst Mode Operation (Figure 14)



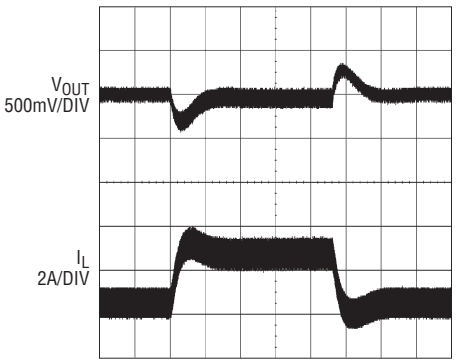
Burst Mode Operation (Figure 14)



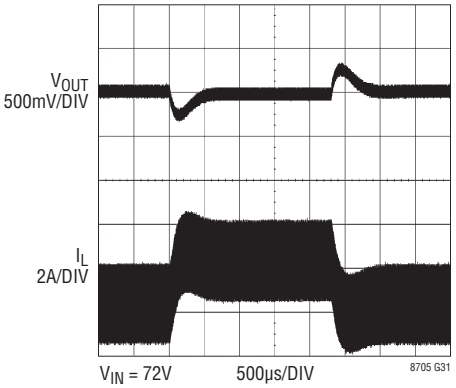
Load Step (Figure 14)



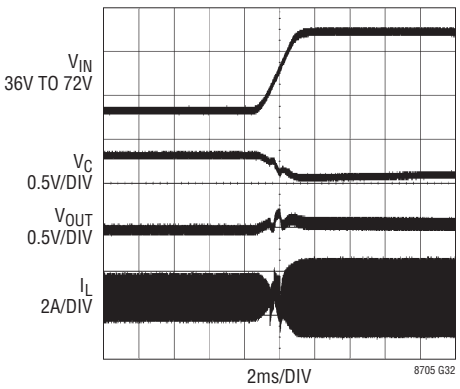
Load Step (Figure 14)



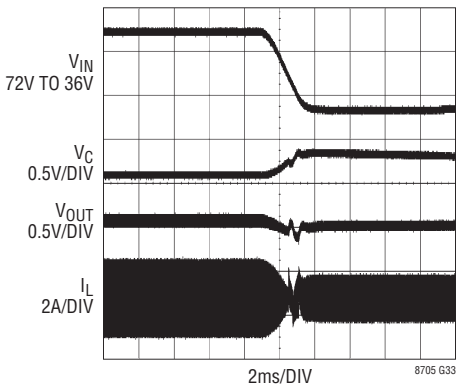
Load Step (Figure 14)



Line Transient (Figure 14)



Line Transient (Figure 14)



PIN FUNCTIONS (QFN/TSSOP)

$\overline{SHDN}$ (Pin 1/Pin 4): Shutdown Pin. Tie high to enable device. Ground to shut down and reduce quiescent current to a minimum. Do not float this pin.

CSN (Pin 2/Pin 5): The (–) Input to the Inductor Current Sense and Reverse-Current Detect Amplifier.

CSP (Pin 3/Pin 6): The (+) Input to the Inductor Current Sense and Reverse-Current Detect Amplifier. The V_C pin voltage and built-in offsets between CSP and CSN pins, in conjunction with the R_{SENSE} resistor value, set the current trip threshold.

LDO33 (Pin 4/Pin7): 3.3V Regulator Output. Bypass this pin to ground with a minimum 0.1µF ceramic capacitor.

FBIN (Pin 5/Pin 8): Input Feedback Pin. This pin is connected to the input error amplifier input.

FBOUT (Pin 6/Pin 9): Output Feedback Pin. This pin connects the error amplifier input to an external resistor divider from the output.

IMON_OUT (Pin 7/Pin 10): Output Current Monitor Pin. The current out of this pin is proportional to the output current. See the Operation and Applications Information sections.

V_C (Pin 8/Pin 11): Error Amplifier Output Pin. Tie external compensation network to this pin.

SS (Pin 9/Pin 12): Soft-Start Pin. Place at least 100nF of capacitance here. Upon start-up, this pin will be charged by an internal resistor to 2.5V.

CLKOUT (Pin 10/Pin 13): Clock Output Pin. Use this pin to synchronize one or more compatible switching regulator ICs to the LT8705. CLKOUT toggles at the same frequency as the internal oscillator or as the SYNC pin, but is approximately 180° out of phase. CLKOUT may also be used as a temperature monitor since the CLKOUT duty cycle varies linearly with the part's junction temperature. The CLKOUT pin can drive capacitive loads up to 200pF.

SYNC (Pin 11/Pin 14): To synchronize the switching frequency to an outside clock, simply drive this pin with a clock. The high voltage level of the clock needs to exceed 1.3V, and the low level should be less than 0.5V. Drive this pin to less than 0.5V to revert to the internal free-running clock. See the Applications Information section for more information.

RT (Pin 12/Pin 15): Timing Resistor Pin. Adjusts the switching frequency. Place a resistor from this pin to ground to set the free-running frequency. Do not float this pin.

BG1, BG2 (Pins 14, 16/Pins 17, 19): Bottom Gate Drive. Drives the gates of the bottom N-channel MOSFETs between ground and $GATEV_{CC}$.

$GATEV_{CC}$ (Pin 15/Pin 18): Power Supply for Gate Drivers. Must be connected to the $INTV_{CC}$ pin. Do not power from any other supply. Locally bypass to GND.

BOOST1, BOOST2 (Pins 23, 17/Pins 28, 20): Boosted Floating Driver Supply. The (+) terminal of the bootstrap capacitor connects here. The BOOST1 pin swings from a diode voltage below $GATEV_{CC}$ up to V_{IN} + $GATEV_{CC}$. The BOOST2 pin swings from a diode voltage below $GATEV_{CC}$ up to V_{OUT} + $GATEV_{CC}$

TG1, TG2 (Pins 22, 18/Pins 26, 21): Top Gate Drive. Drives the top N-channel MOSFETs with voltage swings equal to $GATEV_{CC}$ superimposed on the switch node voltages.

SW1, SW2 (Pins 21, 19/Pins 24, 22): Switch Nodes. The (–) terminals of the bootstrap capacitors connect here.

SRVO_FBIN (Pin 25 QFN Only): Open-Drain Logic Output. This pin is pulled to ground when the input voltage feedback loop is active.

SRVO_IIN (Pin 26 QFN Only): Open-Drain Logic Output. The pin is pulled to ground when the input current loop is active.

SRVO_IOUT (Pin 27 QFN Only): Open-Drain Logic Output. The pin is pulled to ground when the output current feedback loop is active.

SRVO_FBOUT (Pin 28 QFN Only): Open-Drain Logic Output. This pin is pulled to ground when the output voltage feedback loop is active.

$EXTV_{CC}$ (Pin 29/Pin 30): External V_{CC} Input. When $EXTV_{CC}$ exceeds 6.4V (typical), $INTV_{CC}$ will be powered from this pin. When $EXTV_{CC}$ is lower than 6.22V (typical), $INTV_{CC}$ will be powered from V_{IN}.

CSNOUT (Pin 30/Pin 32): The (–) Input to the Output Current Monitor Amplifier. Connect this pin to V_{OUT} when not in use. See Applications Information section for proper use of this pin.

PIN FUNCTIONS (QFN/TSSOP)

CSPOUT (Pin 31/Pin 34): The (+) Input to the Output Current Monitor Amplifier. This pin and the CSNOUT pin measure the voltage across the sense resistor, R_{SENSE2}, to provide the output current signals. Connect this pin to V_{OUT} when not in use. See Applications Information section for proper use of this pin.

CSNIN (Pin 32/Pin 36): The (–) Input to the Input Current Monitor Amplifier. This pin and the CSPIN pin measure the voltage across the sense resistor, R_{SENSE1}, to provide the input current signals. Connect this pin to V_{IN} when not in use. See Applications Information section for proper use of this pin.

CSPIN (Pin 33/Pin 37): The (+) Input to the Input Current Monitor Amplifier. Connect this pin to V_{IN} when not in use. See Applications Information section for proper use of this pin.

V_{IN} (Pin 34/Pin 38): Main Input Supply Pin. It must be locally bypassed to ground.

$INTV_{CC}$ (Pin 35/Pin 1): Internal 6.35V Regulator Output. Must be connected to the $GATEV_{CC}$ pin. $INTV_{CC}$ is powered from $EXTV_{CC}$ when the $EXTV_{CC}$ voltage is higher than 6.4V, otherwise $INTV_{CC}$ is powered from V_{IN} . Bypass this pin to ground with a minimum 4.7µF ceramic capacitor.

SWEN (Pin 36 QFN Only): Switch Enable Pin. Tie high to enable switching. Ground to disable switching. Don't float this pin. This pin is internally tied to $INTV_{CC}$ in the TSSOP package.

IMON_IN (Pin 38/Pin 3): Input Current Monitor Pin. The current out of this pin is proportional to the input current. See the Operation and Applications Information sections.

MODE (Pin 37/Pin 2): Mode Pin. The voltage applied to this pin sets the operating mode of the controller. When the applied voltage is less than 0.4V, the forced continuous current mode is active. When this pin is allowed to float, Burst Mode operation is active. When the MODE pin voltage is higher than 2.3V, discontinuous mode is active.

GND (Pin 13, Exposed Pad Pin 39/Pin 16, Exposed Pad Pin 39): Ground. Tie directly to local ground plane.

BLOCK DIAGRAM

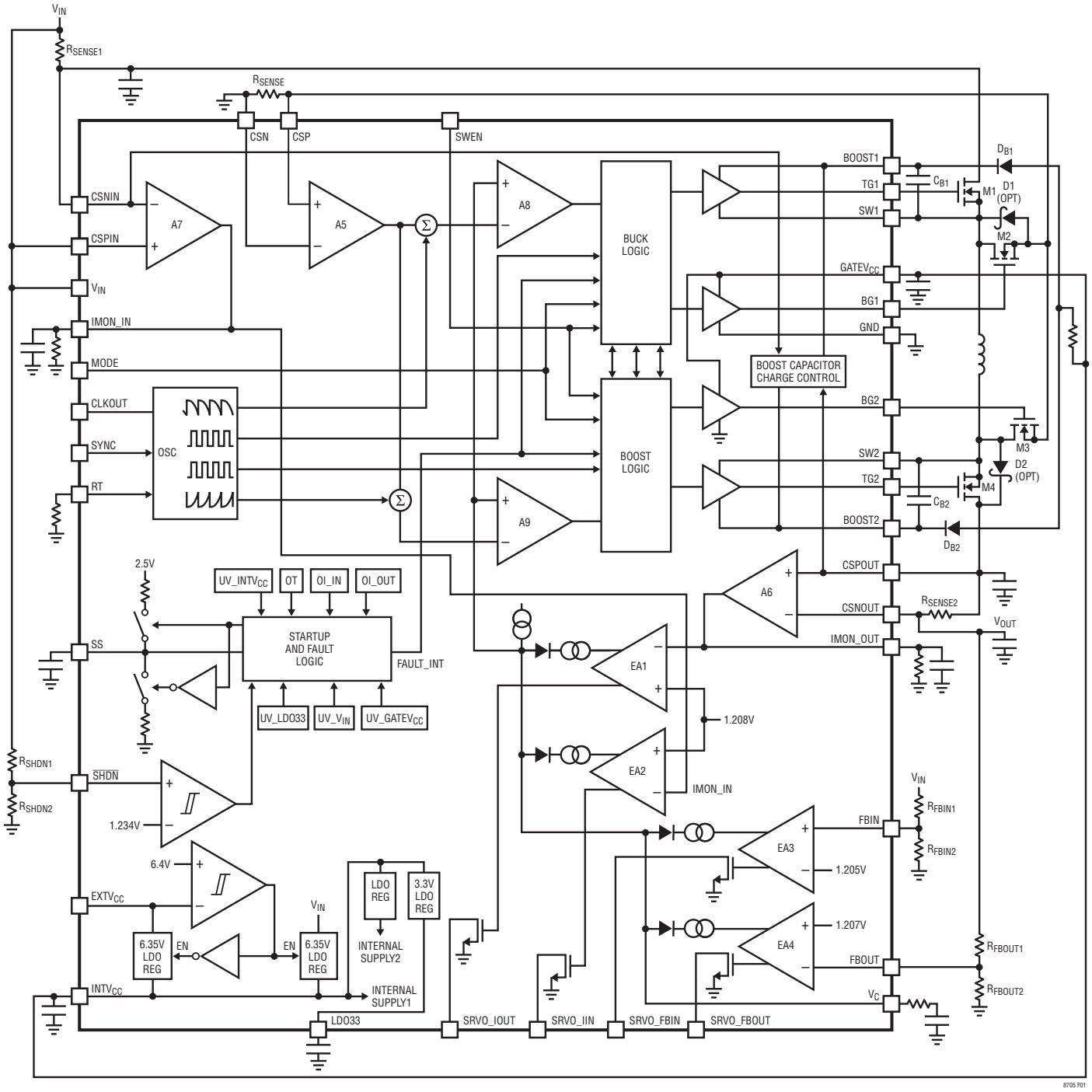


Figure 1. Block Diagram

OPERATION

Refer to the Block Diagram (Figure 1) when reading the following sections about the operation of the LT8705.

Main Control Loop

The LT8705 is a current mode controller that provides an output voltage above, equal to or below the input voltage. The LTC proprietary topology and control architecture employs a current-sensing resistor (R_{SENSE}) in buck or boost modes. The inductor current is controlled by the voltage on the V_C pin, which is the diode-AND of error amplifiers EA1-EA4. In the simplest form, where the output is regulated to a constant voltage, the FBOUT pin receives the output voltage feedback signal, which is compared to the internal reference voltage by EA4. Low output voltages would create a higher V_C voltage, and thus more current would flow into the output. Conversely, higher output voltages would cause V_C to drop, thus reducing the current fed into the output.

The LT8705 contains four error amplifiers (EA1-EA4) allowing it to regulate or limit the output current (EA1), input current (EA2), input voltage (EA3) and/or output voltage (EA4). In a typical application, the output voltage might be regulated using EA4, while the remaining error amplifiers are monitoring for excessive input or output current or an input undervoltage condition. In other applications, such as a battery charger, the output current regulator (EA1) can facilitate constant current charging until a predetermined voltage is reached where the output voltage (EA4) control would take over.

$INTV_{CC}$/$EXTV_{CC}$/$GATEV_{CC}$/LDO33 Power

Power for the top and bottom MOSFET drivers, the LDO33 pin and most internal circuitry is derived from the $INTV_{CC}$ pin. $INTV_{CC}$ is regulated to 6.35V (typical) from either the V_{IN} or $EXTV_{CC}$ pin. When the $EXTV_{CC}$ pin is left open or tied to a voltage less than 6.22V (typical), an internal low dropout regulator regulates $INTV_{CC}$ from V_{IN}. If $EXTV_{CC}$ is taken above 6.4V (typical), another low dropout regulator will instead regulate $INTV_{CC}$ from $EXTV_{CC}$. Regulating $INTV_{CC}$ from $EXTV_{CC}$ allows the power to be derived from the lowest supply voltage (highest efficiency) such as the LT8705 switching regulator output (see $INTV_{CC}$ Regulators and $EXTV_{CC}$ Connection in the Applications Information section for more details).

The $GATEV_{CC}$ pin directly powers the bottom MOSFET drivers for switches M2 and M3. $GATEV_{CC}$ should always be connected to $INTV_{CC}$ and should not be powered or connected to any other source. Undervoltage lock outs (UVLOs) monitoring $INTV_{CC}$ and $GATEV_{CC}$ disable the switching regulator when the pins are below 4.65V (typical).

The LDO33 pin is available to provide power to external components such as a microcontroller and/or to provide an accurate bias voltage. Load current is limited to 17.25mA (typical). As long as $\overline{SHDN}$ is high the LDO33 output is linearly regulated from the $INTV_{CC}$ pin and is not affected by the $INTV_{CC}$ or $GATEV_{CC}$ UVLOs or the SWEN pin voltage. LDO33 will remain regulated as long as $\overline{SHDN}$ is high and sufficient voltage is available on $INTV_{CC}$ (typically > 4.0V). An undervoltage lockout, monitoring LDO33, will disable the switching regulator when LDO33 is below 3.04V (typical).

Start-Up

Figure 2 illustrates the start-up sequence for the LT8705. The master shutdown pin for the chip is $\overline{SHDN}$. When driven below 0.4V the chip is disabled (chip off state) and quiescent current is minimal. Increasing the $\overline{SHDN}$ voltage can increase quiescent current but will not enable the chip until $\overline{SHDN}$ is driven above 1.234V (typical) after which the $INTV_{CC}$ and LDO33 regulators are enabled (switcher off state). External devices powered by the LDO33 pin can become active at this time if enough voltage is available on V_{IN} or $EXTV_{CC}$ to raise $INTV_{CC}$, and thus LDO33, to an adequate voltage.

Starting up the switching regulator happens after SWEN (switcher enable) is also driven above 1.206V (typical), $INTV_{CC}$ and $GATEV_{CC}$ have risen above 4.81V (typical) and the LDO33 pin has risen above 3.08V (typical) (initialize state). The SWEN pin is not available in the TSSOP package. In this package the SWEN pin is internally connected to $INTV_{CC}$.

Start-Up: Soft-Start of Switch Current

In the initialize state, the SS (soft-start) pin is pulled low to prepare for soft starting the regulator. If forced continuous mode is selected (MODE pin low), the part is put into discontinuous mode during soft-start to prevent current

OPERATION

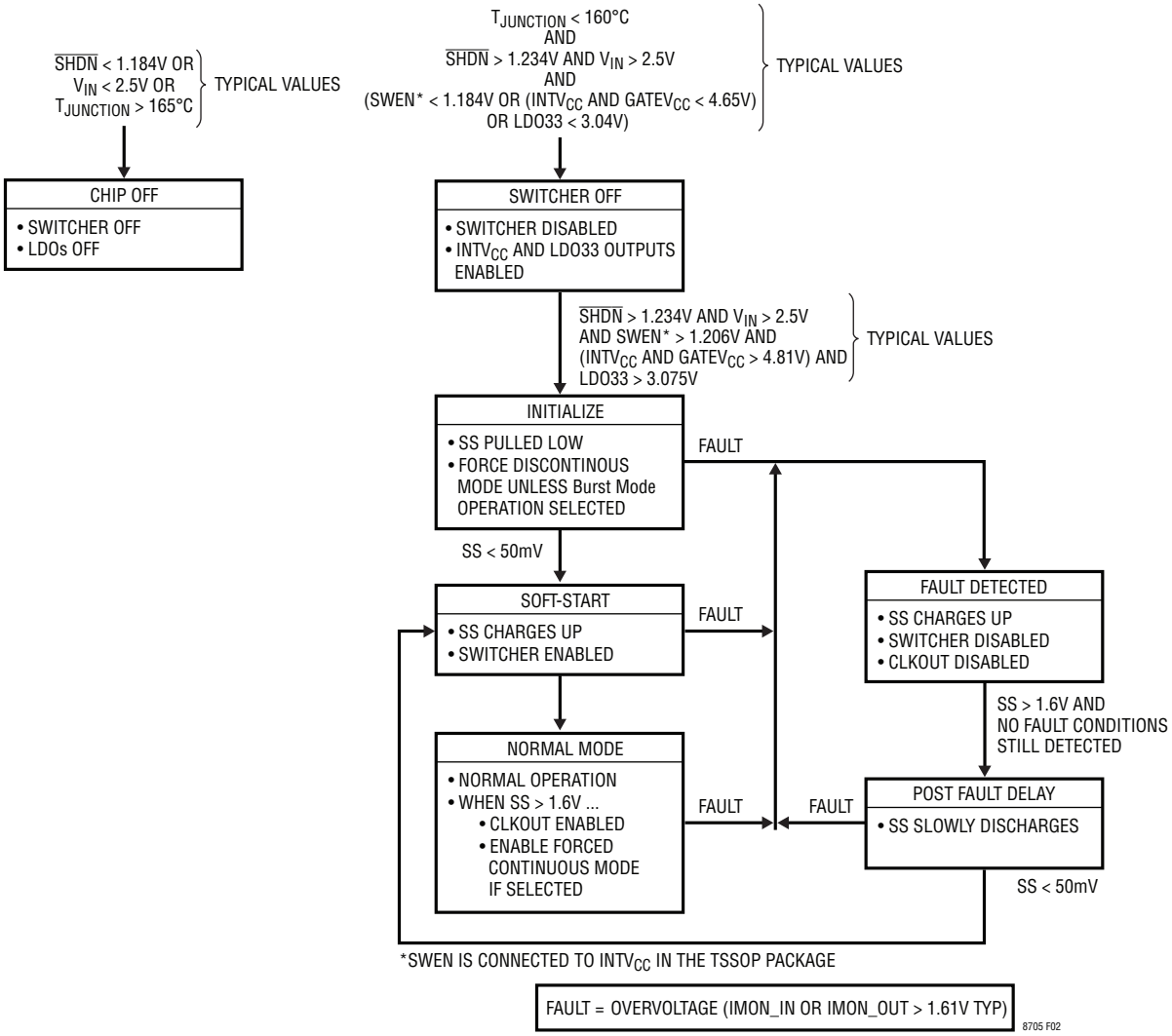


Figure 2. Start-Up and Fault Sequence

from being drawn out of the output and forced into the input. After SS has been discharged to less than 50mV, a soft-start of the switching regulator begins (soft-start state). The soft-start circuitry provides for a gradual ramp-up of the inductor current by gradually allowing the V_C voltage to rise (refer to V_C vs SS Voltage in the Typical Performance Characteristics). This prevents abrupt surges of current from being drawn out of the input power supply. An integrated 100k resistor pulls the SS pin to ≅2.5V. The ramp rate of the SS pin voltage is set by this 100k resistor and the external capacitor connected to this pin. Once SS gets to 1.6V, the CLKOUT pin is enabled, the part is allowed to enter forced continuous mode (if MODE is low) and an internal regulator pulls SS up quickly to ≅2.5V. Typical values for the external soft-start capacitor range from 100nF to 1µF. A minimum of 100nF is recommended.

Fault Conditions

The LT8705 activates a fault sequence under certain operating conditions. If any of these conditions occur (see Figure 2) the CLKOUT pin and internal switching activity are disabled. At the same time, a timeout sequence commences where the SS pin is charged up to a minimum of 1.6V (fault detected state). The SS pin will continue

OPERATION

charging up to 2.5V and be held there in the case of a fault event that persists. After the fault condition had ended and SS is greater than 1.6V, SS will then slowly discharge to 50mV (post fault delay state). This timeout period relieves the part and other downstream power components from electrical and thermal stress for a minimum amount of time as set by the voltage ramp rate on the SS pin. After SS has discharged to < 50mV, the LT8705 will enter the soft-start state and restart switching activity.

Power Switch Control

Figure 3 shows a simplified diagram of how the four power switches are connected to the inductor, V_{IN}, V_{OUT} and ground. Figure 4 shows the regions of operation for the LT8705 as a function of V_{OUT}-V_{IN} or switch duty cycle DC. The power switches are properly controlled so the transfer between modes is continuous.

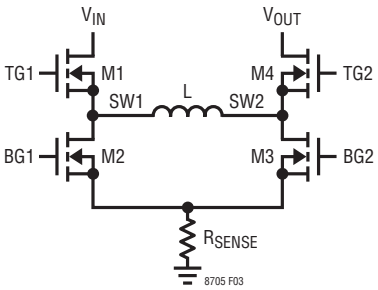


Figure 3. Simplified Diagram of the Output Switches

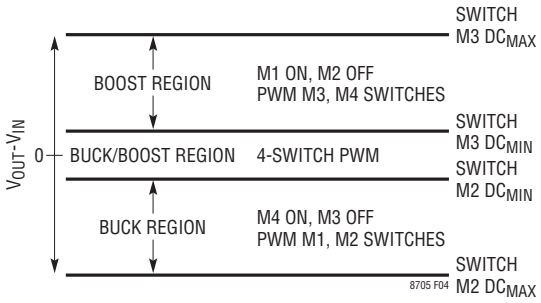


Figure 4. Operating Regions vs V_{OUT}-V_{IN}

Power Switch Control: Buck Region (V_{IN} >> V_{OUT})

When V_{IN} is significantly higher than V_{OUT}, the part will run in the buck region. In this region switch M3 is always off. Also, switch M4 is always on unless reverse current is detected while in Burst Mode operation or discontinuous mode. At the start of every cycle, synchronous switch M2 is turned on first. Inductor current is sensed by amplifier A5 while switch M2 is on. A slope compensation ramp is added to the sensed voltage which is then compared by A8 to a reference that is proportional to V_C. After the sensed inductor current falls below the reference, switch M2 is turned off and switch M1 is turned on for the remainder of the cycle. Switches M1 and M2 will alternate, behaving like a typical synchronous buck regulator.

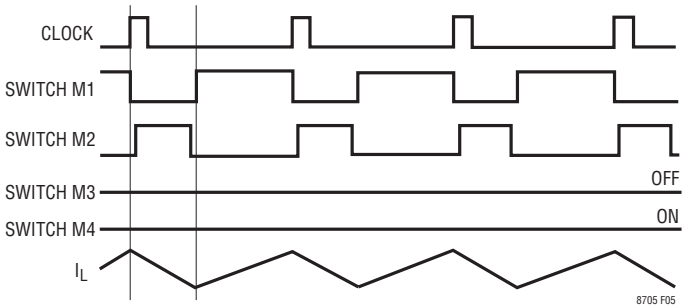


Figure 5. Buck Region (V_{IN} >> V_{OUT})

The part will continue operating in the buck region over a range of switch M2 duty cycles. The duty cycle of switch M2 in the buck region is given by:

$$DC_{(M2,BUCK)} = \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \bullet 100\%$$

As V_{IN} and V_{OUT} get closer to each other, the duty cycle decreases until the minimum duty cycle of the converter in buck mode reaches $DC_{(ABSMIN,M2,BUCK)}$. If the duty cycle becomes lower than $DC_{(ABSMIN,M2,BUCK)}$ the part will move to the buck-boost region.

$$DC_{(ABSMIN,M2,BUCK)} \cong t_{ON(M2,MIN)} \bullet f \bullet 100\%$$

where:

$t_{ON(M2,MIN)}$ is the minimum on-time for the synchronous switch in buck operation (260ns typical, see Electrical Characteristics).

f is the switching frequency

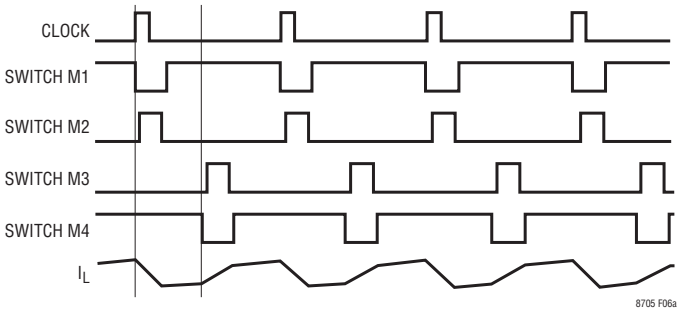
When V_{IN} is much higher than V_{OUT} the duty cycle of switch M2 will increase, causing the M2 switch off-time to decrease. The M2 switch off-time should be kept above 245ns (typical, see Electrical Characteristics) to maintain steady-state operation, avoid duty cycle jitter, increased output ripple and reduction in maximum output current.

OPERATION

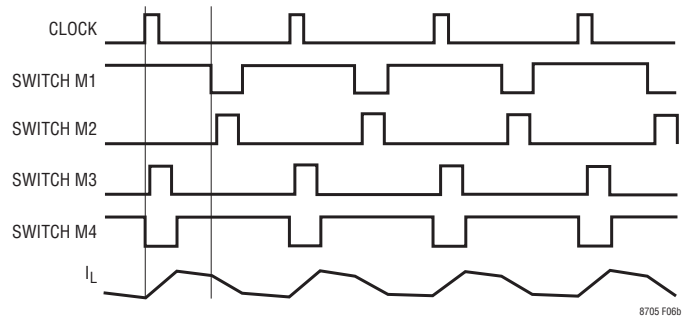
Power Switch Control: Buck-Boost ($V_{IN} \cong V_{OUT}$)

When V_{IN} is close to V_{OUT}, the controller enters the buck-boost region. Figure 6 shows typical waveforms in this region. Every cycle, if the controller starts with switches M2 and M4 turned on, the controller first operates as if in the buck region. When A8 trips, switch M2 is turned off and M1 is turned on until the middle of the clock cycle. Next, switch M4 turns off and M3 turns on. The LT8705 then operates as if in boost mode until A9 trips. Finally switch M3 turns off and M4 turns on until the end of the cycle.

If the controller starts with switches M1 and M3 turned on, the controller first operates as if in the boost region. When A9 trips, switch M3 is turned off and M4 is turned on until the middle of the clock cycle. Next, switch M1 turns off and M2 turns on. The LT8705 then operates as if in buck mode until A8 trips. Finally switch M2 turns off and M1 turns on until the end of the cycle.



(6a) Buck-Boost Region ($V_{IN} \geq V_{OUT}$)



(6b) Buck-Boost Region ($V_{IN} \leq V_{OUT}$)

Figure 6. Buck-Boost Region

Power Switch Control: Boost Region ($V_{IN} << V_{OUT}$)

When V_{OUT} is significantly higher than V_{IN}, the part will run in the boost region. In this region switch M1 is always on and switch M2 is always off. At the start of every cycle, switch M3 is turned on first. Inductor current is sensed by amplifier A5 while switch M3 is on. A slope compensation ramp is added to the sensed voltage which is then compared (A9) to a reference that is proportional to V_C. After the sensed inductor current rises above the reference voltage, switch M3 is turned off and switch M4 is turned on for the remainder of the cycle. Switches M3 and M4 will alternate, behaving like a typical synchronous boost regulator.

The part will continue operating in the boost region over a range of switch M3 duty cycles. The duty cycle of switch M3 in the boost region is given by:

$$DC_{(M3,BOOST)} = \left(1 - \frac{V_{IN}}{V_{OUT}}\right) \bullet 100\%$$

As V_{IN} and V_{OUT} get closer to each other, the duty cycle decreases until the minimum duty cycle of the converter in boost mode reaches $DC_{(ABSMIN,M3,BOOST)}$. If the duty cycle becomes lower than $DC_{(ABSMIN,M3,BOOST)}$ the part will move to the buck-boost region:

$$DC_{(ABSMIN,M3,BOOST)} \cong t_{ON(M3,MIN)} \bullet f \bullet 100\%$$

where:

$t_{ON(M3,MIN)}$ is the minimum on-time for the main switch in boost operation (265ns typical, see Electrical Characteristics)

f is the switching frequency

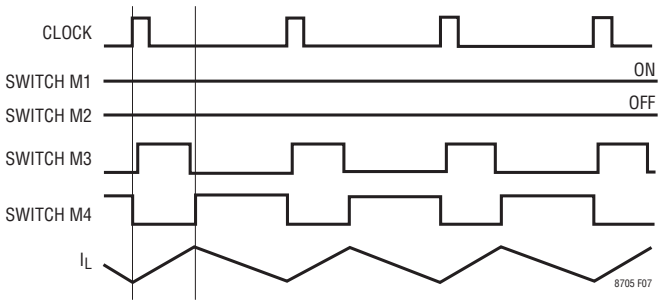


Figure 7. Boost Region ($V_{IN} << V_{OUT}$)

OPERATION

When V_{OUT} is much higher than V_{IN} the duty cycle of switch M3 will increase, causing the M3 switch off-time to decrease. The M3 switch off-time should be kept above 245ns (typical, see Electrical Characteristics) to maintain steady-state operation, avoid duty cycle jitter, increased output ripple and reduction in maximum output current.

Light Load Current Operation (MODE Pin)

Under light current load conditions, the LT8705 can be set to operate in discontinuous mode, forced continuous mode, or Burst Mode operation. To select forced continuous mode, tie the MODE pin to a voltage below 0.4V (i.e., ground). To select discontinuous mode, tie MODE to a voltage above 2.3V (i.e., LDO33). To select Burst Mode operation, float the MODE pin or tie it between 1.0V and 1.7V.

Discontinuous Mode: When the LT8705 is in discontinuous mode, synchronous switch M4 is held off whenever reverse current in the inductor is detected. This is to prevent current draw from the output and/or feeding current to the input supply. Under very light loads, the current comparator may also remain tripped for several cycles and force switches M1 and M3 to stay off for the same number of cycles (i.e., skipping pulses). Synchronous switch M2 will remain on during the skipped cycles, but since switch M4 is off, the inductor current will not reverse.

Burst Mode Operation: Burst Mode operation sets a V_C level, with about 25mV of hysteresis, below which switching activity is inhibited and above which switching activity is re-enabled. A typical example is when, at light output currents, V_{OUT} rises and forces the V_C pin below the threshold that temporarily inhibits switching. After V_{OUT} drops slightly and V_C rises ~25mV the switching is resumed, initially in the buck-boost region. Burst Mode operation can increase efficiency at light load currents by eliminating unnecessary switching activity and related power losses. Burst Mode operation handles reverse-current detection similar to discontinuous mode. The M4 switch is turned off when reverse current is detected.

Forced Continuous Mode: The forced continuous mode allows the inductor current to reverse directions without any switches being forced "off" to prevent this from happening. At very light load currents the inductor current will swing positive and negative as the appropriate average current is delivered to the output. During soft-start, when the SS pin is below 1.6V, the part will be forced into discontinuous mode to prevent pulling current from the output to the input. After SS rises above 1.6V, forced continuous mode will be enabled.

Voltage Regulation Loops

The LT8705 provides two constant-voltage regulation loops, one for output voltage and one for input voltage. A resistor divider between V_{OUT}, FBOUT and GND senses the output voltage. As with traditional voltage regulators, when FBOUT rises near or above the reference voltage of EA4 (1.207V typical, see Block Diagram), the V_C voltage is reduced to command the amount of current that keeps V_{OUT} regulated to the desired voltage.

The input voltage can also be sensed by connecting a resistor divider between V_{IN}, FBIN and GND. When the FBIN voltage falls near or below the reference voltage of EA3 (1.205V typical, see Block Diagram), the V_C voltage is reduced to also reduce the input current. For applications with a high input source impedance (i.e., a solar panel), the input voltage regulation loop can prevent the input voltage from becoming too low under high output load conditions. For applications with a lower input source impedance (i.e., batteries and voltage supplies), the FBIN pin can be used to stop switching activity when the input power supply voltage gets too low for proper system operation. See the Applications Information section for more information about setting up the voltage regulation loops.

Current Monitoring and Regulation

The LT8705 provides two constant-current regulation loops, one for input current and one for output current. A sensing resistor close to the input capacitor, sensed by CSPIN and CSNIN, monitors the input current. A current, linearly proportional to the sense voltage (V_{CSPIN}-V_{CSNIN}), is forced out of the IMON_IN pin and into an external resistor. The resulting voltage V_{IMON_IN} is therefore linearly proportional to the input current. Similarly, a sensing resistor close to the output capacitor, and sensed by CSPOUT and CSNOUT will monitor the output current and generate a voltage V_{IMON_OUT} that is linearly proportional to the output current.

OPERATION

When the input or output current causes the respective IMON_IN or IMON_OUT voltage to rise near or above 1.208V (typical), the V_C pin voltage will be pulled down to maintain the desired maximum input and/or output current (see EA1 and EA2 on the Block Diagram). The input current limit function prevents overloading the DC input source, while the output current limit provides a building block for battery charger or LED driver applications. It can also serve as short-circuit protection for a constant-voltage regulator. See the Applications Information section for more information about setting up the current regulation loops.

SRVO Pins

The QFN package has four open-drain SRVO pins: SRVO_FBIN, SRVO_FBOUT, SRVO_IIN, SRVO_IOUT. Place pull-up resistors from the desired SRVO pin(s) to a power supply less than 30V (i.e., the LDO33 pin) to enable reading of their logic states. The SRVO_FBOUT, SRVO_IIN and SRVO_IOUT pins are pulled low when their associated error amp (EA4, EA2, EA1) input voltages are near or greater than their regulation voltages (≅1.2V typical). SRVO_FBIN is pulled low when FBIN is near or lower than its regulation voltage (≅1.2V typical). The SRVO pins can therefore be used as indicators of when their respective feedback loops are active. For example, the SRVO_FBOUT pin pulls low when FBOUT rises to within 29mV (typical, see Electrical Characteristics) of its regulation voltage (1.207V typical). The pull-down turns off after FBOUT falls to more than 44mV (typical) lower than its regulation voltage. As another example, the SRVO_IOUT pin can be read to determine when the output current has nearly reached its predetermined limit. A logic "1" on SRVO_IOUT indicates that the output current has not reached the current limit and a logic "0" indicates that it has.

CLKOUT and Temperature Sensing

The CLKOUT pin toggles at the LT8705's internal clock frequency whether the internal clock is synchronized to an external source or is free-running based on the external R_T resistor. The CLKOUT pin can be used to synchronize other devices to the LT8705's switching frequency. Also, the duty cycle of CLKOUT is proportional to the die temperature and can be used to monitor the die for thermal issues.

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The first page shows a typical LT8705 application circuit. After the switching frequency is selected, external component selection continues with the selection of R_{SENSE} and the inductor value. Next, the power MOSFETs are selected. Finally, C_{IN} and C_{OUT} are selected. The following examples and equations assume continuous conduction mode unless otherwise specified. The circuit can be configured for operation up to an input and/or output voltage of 80V.

Operating Frequency Selection

The LT8705 uses a constant frequency architecture between 100kHz and 400kHz. The frequency can be set using the internal oscillator or can be synchronized to an external clock source. Selection of the switching frequency is a trade-off between efficiency and component size. Low frequency operation increases efficiency by reducing MOSFET switching losses, but requires more inductance and/or capacitance to maintain low output ripple voltage. For high power applications, consider operating at lower frequencies to minimize MOSFET heating from switching losses. The switching frequency can be set by placing an appropriate resistor from the RT pin to ground and tying the SYNC pin low. The frequency can also be synchronized to an external clock source driven into the SYNC pin. The following sections provide more details.

Internal Oscillator

The operating frequency of the LT8705 can be set using the internal free-running oscillator. When the SYNC pin is driven low (<0.5V), the frequency of operation is set by the value of a resistor from the RT pin to ground. An internally trimmed timing capacitor resides inside the IC. The oscillator frequency is calculated using the following formula:

$$f_{OSC} = \left(\frac{43{,}750}{R_T + 1} \right) kHz$$

where f_{OSC} is in kHz and R_T is in kΩ. Conversely, R_T (in kΩ) can be calculated from the desired frequency (in kHz) using:

$$R_T = \left(\frac{43{,}750}{f_{OSC}} - 1 \right) k\Omega$$

SYNC Pin and Clock Synchronization

The operating frequency of the LT8705 can be synchronized to an external clock source. To synchronize to the external source, simply provide a digital clock signal into the SYNC pin. The LT8705 will operate at the SYNC clock frequency.

The duty cycle of the SYNC signal must be between 20% and 80% for proper operation. Also, the frequency of the SYNC signal must meet the following two criteria:

1. SYNC may not toggle outside the frequency range of 100kHz to 400KHz unless it is stopped low to enable the free-running oscillator.
2. The SYNC pin frequency can always be higher than the free-running oscillator set frequency, f_{OSC}, but should not be less than 25% below f_{OSC}.

After SYNC begins toggling, it is recommended that switching activity is stopped before the SYNC pin stops toggling. Excess inductor current can result when SYNC stops toggling as the LT8705 transitions from the external SYNC clock source to the internal free-running oscillator clock. Switching activity can be stopped by driving either the SWEN or $\overline{SHDN}$ pin low.

CLKOUT Pin and Clock Synchronization

The CLKOUT pin can drive up to 200pF and toggles at the LT8705's internal clock frequency whether the internal clock is synchronized to the SYNC pin or is free-running based on the external R_T resistor. The rising edge of CLKOUT is approximately 180° out of phase from the internal clock's

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rising edge or the SYNC pin's rising edge if it is toggling. CLKOUT toggles only in normal mode (see Figure 2).

The CLKOUT pin can be used to synchronize other devices to the LT8705's switching frequency. For example, the CLKOUT pin can be tied to the SYNC pin of another LT8705 regulator which will operate approximately 180° out of phase of the master LT8705 due to the CLKOUT phase shift. The frequency of the master LT8705 can be set by the external R_T resistor or by toggling the SYNC pin. CLKOUT will begin oscillating after the master LT8705 enters normal mode (see Figure 2). Note that the RT pin of the slave LT8705 must have a resistor tied to ground. In general, use the same value R_T resistor for all of the synchronized LT8705s.

The duty cycle of CLKOUT is proportional to the die temperature and can be used to monitor the die for thermal issues. See the Junction Temperature Measurement section for more information.

Inductor Current Sensing and Slope Compensation

The LT8705 operates using inductor current mode control. As described previously in the Power Switch Control section, the LT8705 measures the peak of the inductor current waveform in the boost region and the valley of the inductor current waveform in the buck region. The inductor current is sensed across the R_{SENSE} resistor with pins CSP and CSN. During any given cycle, the peak (boost region) or valley (buck region) of the inductor current is controlled by the V_C pin voltage.

Slope compensation provides stability in constant-frequency current mode control architectures by preventing subharmonic oscillations at high duty cycles. This is accomplished internally by adding a compensating ramp to the inductor current signal in the boost region, or subtracting a ramp from the inductor current signal in the buck region. At higher duty cycles, this results in a reduction of maximum inductor current in the boost region, and an increase of the maximum inductor current in the buck region. For example, refer to the Maximum Inductor Current Sense Voltage vs Duty Cycle graph in the Typical Performance Characteristics section. The graph shows that, with V_C at its maximum voltage, the maximum inductor sense voltage V_{RSENSE} is between 78mV and 117mV depending on the duty cycle. It also shows that the maximum inductor valley current in the buck region is 86mV increasing to ~130mV at higher duty cycles.

R_{SENSE} Selection and Maximum Current

The R_{SENSE} resistance must be chosen properly to achieve the desired amount of output current. Too much resistance can limit the output current below the application requirements. Start by determining the maximum allowed R_{SENSE} resistance in the boost region, $R_{SENSE(MAX,BOOST)}$. Follow this by finding the maximum allowed R_{SENSE} resistance in the buck region, $R_{SENSE(MAX,BUCK)}$. The selected R_{SENSE} resistance must be smaller than both.

Boost Region: In the boost region, the maximum output current capability is the least when V_{IN} is at its minimum and V_{OUT} is at its maximum. Therefore R_{SENSE} must be chosen to meet the output current requirements under these conditions.

Start by finding the boost region duty cycle when V_{IN} is minimum and V_{OUT} is maximum using:

$$DC_{(MAX,M3,BOOST)} \cong \left(1 - \frac{V_{IN(MIN)}}{V_{OUT(MAX)}}\right) \bullet 100\%$$

For example, an application with a V_{IN} range of 12V to 48V and V_{OUT} set to 36V will have:

$$DC_{(MAX,M3,BOOST)} \cong \left(1 - \frac{12V}{36V}\right) \bullet 100\% = 67\%$$

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Referring to the Maximum Inductor Current Sense Voltage graph in the Typical Performance Characteristics section, the maximum R_{SENSE} voltage at 67% duty cycle is ≅93mV, or:

$V_{RSENSE(MAX,BOOST,\ MAX)} \cong 93mV$

for V_{IN} = 12V, V_{OUT} = 36V.

Next, the inductor ripple current in the boost region must be determined. If the main inductor L is not known, the maximum ripple current $\Delta I_{L(MAX,BOOST)}$ can be estimated by choosing $\Delta I_{L(MAX,BOOST)}$ to be 30% to 50% of the maximum inductor current in the boost region as follows:

$$\Delta I_{L(MAX,BOOST)} \cong \frac{V_{OUT(MAX)} \bullet I_{OUT(MAX,BOOST)}}{V_{IN(MIN)} \bullet \left(\frac{100\%}{\%Ripple} - 0.5\right)} A$$

where:

$I_{OUT(MAX,BOOST)}$ is the maximum output load current required in the boost region

%Ripple is 30% to 50%

For example, using $V_{OUT(MAX)}$ = 36V, $V_{IN(MIN)}$ = 12V, $I_{OUT(MAX,BOOST)}$ = 2A and %Ripple = 40% we can estimate:

$$\Delta I_{L(MAX,BOOST)} \cong \frac{36V \bullet 2A}{12V \bullet \left(\frac{100\%}{40\%} - 0.5\right)} = 3A$$

Otherwise, if the inductor value is already known then $\Delta I_{L(MAX,BOOST)}$ can be more accurately calculated as follows:

$$\Delta I_{L(MAX,BOOST)} = \frac{\left(\frac{DC_{(MAX,M3,BOOST)}}{100\%}\right) \bullet V_{IN(MIN)}}{f \bullet L} A$$

where:

$DC_{(MAX,M3,BOOST)}$ is the maximum duty cycle percentage in the boost region as calculated previously.

f is the switching frequency

L is the inductance of the main inductor

After the maximum ripple current is known, the maximum allowed R_{SENSE} in the boost region can be calculated as follows:

$$R_{SENSE(MAX,BOOST)} = \frac{2 \bullet V_{RSENSE(MAX,BOOST,MAX)} \bullet V_{IN(MIN)}}{\left(2 \bullet I_{OUT(MAX,BOOST)} \bullet V_{OUT(MIN)}\right) + \left(\Delta I_{L(MAX,BOOST)} \bullet V_{IN(MIN)}\right)} \Omega$$

where $V_{RSENSE(MAX,BOOST,MAX)}$ is the maximum inductor current sense voltage as discussed in the previous section.

Using values from the previous examples:

$$R_{SENSE(MAX,BOOST)} = \frac{2 \bullet 93mV \bullet 12}{(2 \bullet 2A \bullet 36V) + (3A \bullet 12V)} = 12.4m\Omega$$

Buck Region: In the buck region, the maximum output current capability is the least when operating at the minimum duty cycle. This is because the slope compensation ramp increases the maximum R_{SENSE} voltage with increasing duty cycle. The minimum duty cycle for buck operation can be calculated using:

$DC_{(MIN,M2,BUCK)} \cong t_{ON(M2,MIN)} \bullet f \bullet 100\%$

where $t_{ON(M2,MIN)}$ is 260ns (typical value, see Electrical Characteristics)

Before calculating the maximum R_{SENSE} resistance, however, the inductor ripple current must be determined. If the main inductor L is not known, the ripple current $\Delta I_{L(MIN,BUCK)}$ can be estimated by choosing $\Delta I_{L(MIN,BUCK)}$ to be 10% of the maximum inductor current in the buck region as follows:

$$\Delta I_{L(MIN,BUCK)} \cong \frac{I_{OUT(MAX,BUCK)}}{\left(\frac{100\%}{10\%} - 0.5\right)} A$$

where:

$I_{OUT(MAX,BUCK)}$ is the maximum output load current required in the buck region.

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If the inductor value is already known then $\Delta I_{L(MIN,BUCK)}$ can be calculated as follows:

$$\Delta I_{L(MIN,BUCK)} = \frac{\left(\frac{DC_{(MIN,M2,BUCK)}}{100\%}\right) \bullet V_{OUT(MIN)}}{f \bullet L} A$$

where:

$DC_{(MIN,M2,BUCK)}$ is the minimum duty cycle percentage in the buck region as calculated previously.

f is the switching frequency

L is the inductance of the main inductor

After the inductor ripple current is known, the maximum allowed R_{SENSE} in the buck region can be calculated as follows:

$$R_{SENSE(MAX,BUCK)} = \frac{2 \bullet 86mV}{\left(2 \bullet I_{OUT(MAX,BUCK)}\right) - \Delta I_{L(MIN,BUCK)}}$$

Final R_{SENSE} Value: The final R_{SENSE} value should be lower than both $R_{SENSE(MAX,BOOST)}$ and $R_{SENSE(MAX,BUCK)}$. A margin of 30% or more is recommended.

Figure 8 shows approximately how the maximum output current and maximum inductor current would vary with V_{IN}/V_{OUT} while all other operating parameters remain constant (frequency = 350kHz, inductance = 10µH, R_{SENSE} = 10mΩ). This graph is normalized and accounts for changes in maximum current due to the slope compensation ramps and the effects of changing ripple current. The curve is theoretical, but can be used as a guide to predict relative changes in maximum output and inductor current over a range of V_{IN}/V_{OUT} voltages.

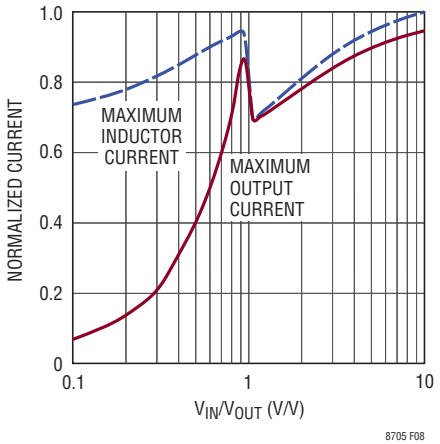

Figure 8. Currents vs V_{IN}/V_{OUT} Ratio

Reverse Current Limit

When the forced continuous mode is selected (MODE pin low), inductor current is allowed to reverse directions and flow from the V_{OUT} side to the V_{IN} side. This can lead to current sinking from the output and being forced into the input. The reverse current is at a maximum magnitude when V_C is lowest. The graph of Minimum Inductor Current Sense Voltage in FCM in the Typical Performance Characteristics section can help to determine the maximum reverse current capability.

Inductor Selection

For high efficiency, choose an inductor with low core loss, such as ferrite. Also, the inductor should have low DC resistance to reduce the I^2R losses, and must be able to handle the peak inductor current without saturating. To minimize radiated noise, use a toroid, pot core or shielded bobbin inductor.

The operating frequency and inductor selection are interrelated in that higher operating frequencies allow the use of smaller inductor and capacitor values. The following sections discuss several criteria to consider when choosing an inductor value. For optimal performance, choose an inductor that meets all of the following criteria.

Inductor Selection: Adequate Load Current in the Boost Region

Small value inductors result in increased ripple currents and thus, due to the limited peak inductor current, decrease the maximum average current that can be provided to the load (I_{OUT}) while operating in the boost region.

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In order to provide adequate load current at low V_{IN} voltages in the boost region, L should be at least:

$$L_{(MIN1,BOOST)} \cong \frac{V_{IN(MIN)} \bullet \left(\frac{DC_{(MAX,M3,BOOST)}}{100\%}\right)}{2 \bullet f \bullet \left(\frac{V_{RSENSE(MAX,BOOST,MAX)}}{R_{SENSE}} - \frac{I_{OUT(MAX)} \bullet V_{OUT(MAX)}}{V_{IN(MIN)}}\right)}$$

where:

$DC_{(MAX,M3,BOOST)}$ is the maximum duty cycle percentage of the M3 switch (see R_{SENSE} Selection and Maximum Current section).

f is the switching frequency

$V_{RSENSE(MAX,BOOST,MAX)}$ is the maximum current sense voltage in the boost region at maximum duty cycle (see R_{SENSE} Selection and Maximum Current section)

Negative values of $L_{(MIN1,BOOST)}$ indicate that the output load current I_{OUT} can't be delivered in the boost region because the inductor current limit is too low. If $L_{(MIN1,BOOST)}$ is too large or is negative, consider reducing the R_{SENSE} resistor value to increase the inductor current limit.

Inductor Selection: Subharmonic Oscillations

The LT8705's internal slope compensation circuits will prevent subharmonic oscillations that can otherwise occur when V_{IN}/V_{OUT} is less than 0.5 or greater than 2. The slope compensation circuits will prevent these oscillations provided that the inductance exceeds a minimum value (see the earlier section Inductor Current Sensing and Slope Compensation for more information). Choose an inductance greater than all of the relevant $L_{(MIN)}$ limits discussed below. Negative results can be interpreted as zero.

In the boost region, if V_{OUT} can be greater than twice V_{IN}, calculate $L_{(MIN2,BOOST)}$ as follows:

$$L_{(MIN2,BOOST)} = \frac{\left[V_{OUT(MAX)} - \left(\frac{V_{IN(MIN)} \bullet V_{OUT(MAX)}}{V_{OUT(MAX)} - V_{IN(MIN)}}\right)\right] \bullet R_{SENSE}}{0.08 \bullet f} H$$

In the buck region, if V_{IN} can be greater than twice V_{OUT}, calculate $L_{(MIN1,BUCK)}$ as follows:

$$L_{(MIN1,BUCK)} = \frac{V_{IN(MAX)} \bullet \left(1 - \frac{V_{OUT(MAX)}}{V_{IN(MAX)} - V_{OUT(MIN)}}\right) \bullet R_{SENSE}}{0.08 \bullet f} H$$

Inductor Selection: Maximum Current Rating

The inductor must have a rating greater than its peak operating current to prevent inductor saturation resulting in efficiency loss. The peak inductor current in the boost region is:

$$I_{L(MAX,BOOST)} \cong I_{OUT(MAX)} \bullet \frac{V_{OUT(MAX)}}{V_{IN(MIN)}} + \left(\frac{V_{IN(MIN)} \bullet \left(\frac{DC_{(MAX,M3,BOOST}}{100\%}\right)}{2 \bullet L \bullet f}\right) A$$

where $DC_{(MAX,M3,BOOST)}$ is the maximum duty cycle percentage of the M3 switch (see R_{SENSE} Selection and Maximum Current section).

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The peak inductor current when operating in the buck region is:

$$I_{L(MAX,BUCK)} \cong I_{OUT(MAX)} + \left(\frac{V_{OUT(MIN)} \bullet \left(\frac{DC_{(MAX,M2,BUCK}}{100\%} \right)}{2 \bullet L \bullet f} \right) A$$

where $DC_{(MAX,M2,BUCK)}$ is the maximum duty cycle percentage of the M2 switch in the buck region given by:

$$DC_{(MAX,M2,BUCK)} \cong \left(1 - \frac{V_{OUT(MIN)}}{V_{IN(MAX)}} \right) \bullet 100\%$$

Note that the inductor current can be higher during load transients and if the load current exceeds the expected maximum $I_{OUT(MAX)}$. It can also be higher during start-up if inadequate soft-start capacitance is used or during output shorts. Consider using the output current limiting to prevent the inductor current from becoming excessive. Output current limiting is discussed later in the Input/Output Current Monitoring and Limiting section. Careful board evaluation of the maximum inductor current is recommended.

Power MOSFET Selection and Efficiency Considerations

The LT8705 requires four external N-channel power MOSFETs, two for the top switches (switches M1 and M4, shown in Figure 3) and two for the bottom switches (switches M2 and M3, shown in Figure 3). Important parameters for the power MOSFETs are the breakdown voltage, $V_{BR,DSS}$, threshold voltage, $V_{GS,TH}$, on-resistance, $R_{DS(ON)}$, reverse-transfer capacitance, C_{RSS} (gate-to-drain capacitance), and maximum current, $I_{DS(MAX)}$. The gate drive voltage is set by the 6.35V GATEV_{CC} supply. Consequently, logic-level threshold MOSFETs must be used in LT8705 applications.

It is very important to consider power dissipation when selecting power MOSFETs. The most efficient circuit will use MOSFETs that dissipate the least amount of power. Power dissipation must be limited to avoid overheating that might damage the devices. For most buck-boost applications the M1 and M3 switches will have the highest power dissipation where M2 will have the lowest unless the output becomes shorted. In some cases it can be helpful to use two or more MOSFETs in parallel to reduce power dissipation in each device. This is most helpful when power is dominated by I^2R losses while the MOSFET is "on". The additional capacitance of connecting MOSFETs in parallel can sometimes slow down switching edge rates and consequently increase total switching power losses.

The following sections provide guidelines for calculating power consumption of the individual MOSFETs. From a known power dissipation, the MOSFET junction temperature can be obtained using the following formula:

$$T_J = T_A + P \bullet R_{TH(JA)}$$

where:

T_J is the junction temperature of the MOSFET

T_A is the ambient air temperature

P is the power dissipated in the MOSFET

$R_{TH(JA)}$ is the MOSFET's thermal resistance from the junction to the ambient air. Refer to the manufacturer's data sheet.

$R_{TH(JA)}$ normally includes the $R_{TH(JC)}$ for the device plus the thermal resistance from the case to the ambient temperature $R_{TH(JC)}$. Compare the calculated value of T_J to the manufacturer's data sheets to help choose MOSFETs that will not overheat.

Switch M1: The power dissipation in switch M1 comes from two primary components: (1) I^2R power when the switch is fully turned "on" and inductor current is flowing through the drain to source connections and (2) power

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dissipated while the switch is turning “on” or “off”. As the switch turns “on” and “off” a combination of high current and high voltage causes high power dissipation in the MOSFET. Although the switching times are short, the average power dissipation can still be significant and is often the dominant source of power in the MOSFET. Depending on the application, the maximum power dissipation in the M1 switch can happen in the buck region when V_{IN} is highest, V_{OUT} is highest, and switching power losses are greatest or in the boost region when V_{IN} is smallest, V_{OUT} is highest and M1 is always on. Switch M1 power consumption can be approximated as:

$$P_{M1} = P_{I^2R} + P_{SWITCHING}$$

$$\cong \left(\left(\frac{V_{OUT}}{V_{IN}} \bullet I_{OUT} \right)^2 \bullet R_{DS(ON)} \bullet \rho_\tau \right)$$

$$+ \left(V_{IN} \bullet I_{OUT} \bullet f \bullet t_{RF1} \right) W$$

where:

the $P_{SWITCHING}$ term is 0 in the boost region

t_{RF1} is the average of the SW1 pin rise and fall times. Typical values are 20ns to 40ns depending on the MOSFET capacitance and V_{IN} voltage.

ρ_τ is a normalization factor (unity at 25°C) accounting for the significant variation in MOSFET on-resistance with temperature, typically about 0.4%/°C, as shown in Figure 9. For a maximum junction temperature of 125°C, using a value ρ_τ = 1.5 is reasonable.

Since the switching power ($P_{SWITCHING}$) often dominates, look for MOSFETs with lower C_{RSS} or consider operating at a lower frequency to minimize power loss and increase efficiency.

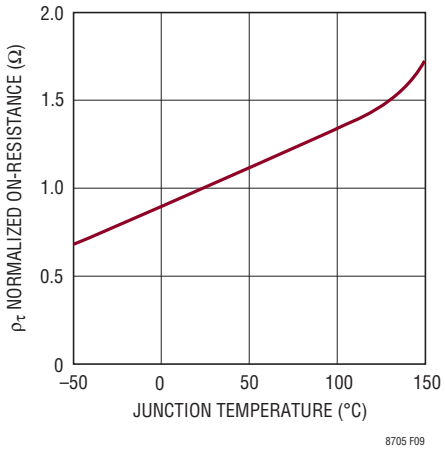

Figure 9. Normalized MOSFET $R_{DS(ON)}$ vs Temperature

Switch M2: In most cases the switching power dissipation in the M2 switch is quite small and I^2R power losses dominate. I^2R power is greatest in the buck region where the switch operates as the synchronous rectifier. Higher V_{IN} and lower V_{OUT} causes the M2 switch to be “on” for the most amount of time, leading to the highest power consumption. The M2 switch power consumption in the buck region can be approximated as:

$$P_{(M2,BUCK)} \cong \left(\frac{V_{IN} - V_{OUT}}{V_{IN}} \bullet I_{OUT(MAX)}^2 \bullet R_{DS(ON)} \bullet \rho_\tau \right) W$$

Switch M3: Switch M3 operates in the boost and buck-boost regions as a control switch. Similar to the M1 switch, the power dissipation comes from I^2R power and switching power. The maximum power dissipation is when V_{IN} is the lowest and V_{OUT} is the highest. The following

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expression approximates the power dissipation in the M3 switch under those conditions:

$$P_{M3} = P_{I^2R} + P_{SWITCHING} \cong$$

$$\left(\frac{(V_{OUT} - V_{IN}) \bullet V_{OUT}}{V_{IN}^2} \bullet I_{OUT}^2 \bullet R_{DS(ON)} \bullet \rho_{\tau} \right)$$

$$+ \left(V_{OUT}^2 \bullet I_{OUT} \bullet f \bullet \frac{t_{RF2}}{V_{IN}} \right) W$$

where the total power is 0 in the buck region.

t_{RF2} is the average of the SW2 pin rise and fall times and, similar to t_{RF1}, is typically 20ns to 40ns.

As with the M1 switch, the switching power ($P_{SWITCHING}$) often dominates. Look for MOSFETs with lower C_{RSS} or consider operating at a lower frequency to minimize power loss and increase efficiency.

Switch M4: In most cases the switching power dissipation in the M4 switch is quite small and I^2R power losses dominate. I^2R power is greatest in the boost region where the switch operates as the synchronous rectifier. Lower V_{IN} and higher V_{OUT} increases the inductor current for a given I_{OUT}, leading to the highest power consumption. The M4 switch power consumption in the boost region can be approximated as:

$$P_{(M4,BOOST)} \cong \left(\frac{V_{OUT}}{V_{IN}} \bullet I_{OUT}^2 \bullet \rho_{\tau} \bullet R_{DS(ON)} \right) W$$

Gate Resistors: In some cases it can be beneficial to add 1Ω to 10Ω of resistance between some of the NMOS gate pins and their respective gate driver pins on the LT8705 (i.e., TG1, BG1, TG2, BG2). Due to parasitic inductance and capacitance, ringing can occur on SW1 or SW2 when low capacitance MOSFETs are turned on/off too quickly. The ringing can be of greatest concern when operating the MOSFETs or the LT8705 near the rated voltage limits. Additional gate resistance slows the switching speed, minimizing the ringing.

Excessive gate resistance can have two negative side effects on performance:

1. Slowing the switch transition times can also increase power dissipation in the switch. This is described above in the Switch M1 and Switch M3 sections.
2. Capacitive coupling from the SW1 or SW2 pin to the switch gate node can turn it on when it's supposed to be off, thus increasing power dissipation. With too much gate resistance, this would most commonly happen to the M2 switch when SW1 is rising.

Careful board evaluation should be performed when optimizing the gate resistance values. SW1 and SW2 pin ringing can be affected by the inductor current levels, therefore board evaluation should include measurements at a wide range of load currents. When performing PCB measurements of the SW1 and SW2 pins, be sure to use a very short ground post from the PCB ground to the scope probe ground sleeve in order to minimize false inductive voltages readings.

C_{IN} and C_{OUT} Selection

Input and output capacitance is necessary to suppress voltage ripple caused by discontinuous current moving in and out of the regulator. A parallel combination of capacitors is typically used to achieve high capacitance and low ESR (equivalent series resistance). Dry tantalum, special

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polymer, aluminum electrolytic and ceramic capacitors are all available in surface mount packages. Capacitors with low ESR and high ripple current ratings, such as OS-CON and POSCAP are also available.

Ceramic capacitors should be placed near the regulator input and output to suppress high frequency switching spikes. A ceramic capacitor, of at least 1µF, should also be placed from V_{IN} to GND as close to the LT8705 pins as possible. Due to their excellent low ESR characteristics ceramic capacitors can significantly reduce input ripple voltage and help reduce power loss in the higher ESR bulk capacitors. X5R or X7R dielectrics are preferred, as these materials retain their capacitance over wide voltage and temperature ranges. Many ceramic capacitors, particularly 0805 or 0603 case sizes, have greatly reduced capacitance at the desired operating voltage.

Input Capacitance: Discontinuous input current is highest in the buck region due to the M1 switch toggling on and off. Make sure that the C_{IN} capacitor network has low enough ESR and is sized to handle the maximum RMS current. For buck operation, the input RMS current is given by:

$$I_{RMS} \cong I_{OUT(MAX)} \bullet \frac{V_{OUT}}{V_{IN}} \bullet \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT(MAX)}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief.

The maximum input ripple due to the voltage drop across the ESR is approximately:

$$\Delta V_{(BUCK,ESR)} \cong \frac{V_{IN(MAX)} \bullet I_{OUT(MAX)}}{V_{OUT(MIN)}} \bullet ESR$$

Output Capacitance: The output capacitance (C_{OUT}) is necessary to reduce the output voltage ripple caused by discontinuities and ripple in the output and load currents. The effects of ESR and the bulk capacitance must be considered when choosing the right capacitor for a given output ripple voltage. The steady-state output ripple due to charging and discharging the bulk output capacitance is given by the following equations:

$$\Delta V_{(BOOST,CAP)} \cong \frac{I_{OUT} \bullet (V_{OUT} - V_{IN})}{C_{OUT} \bullet V_{IN} \bullet f} V \text{ for } V_{OUT} > V_{IN}$$

$$\Delta V_{(BUCK,CAP)} \cong \frac{V_{OUT} \bullet \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}{8 \bullet L \bullet f^2 \bullet C_{OUT}} V \text{ for } V_{OUT} < V_{IN}$$

The maximum output ripple due to the voltage drop across the ESR is approximately:

$$\Delta V_{(BOOST,ESR)} \cong \frac{V_{OUT(MAX)} \bullet I_{OUT(MAX)}}{V_{IN(MIN)}} \bullet ESR$$

As with C_{IN}, multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirements.

Schottky Diode (D1, D2) Selection

The Schottky diodes, D1 and D2, shown in Figure 1, conduct during the dead time between the conduction of the power MOSFET switches. They are intended to prevent the body diodes of synchronous switches M2 and M4 from turning on and storing charge. For example, D2 significantly reduces reverse-recovery current between switch M4 turn-off and switch M3 turn-on, which improves converter efficiency, reduces switch M3 power dissipation and reduces noise in the inductor current sense resistor (R_{SENSE}) when M3 turns on. In order for the diode to be effective, the inductance between it and the synchronous switch must be as small as possible, mandating that these components be placed adjacently.

For applications with high input or output voltages (typically >40V) avoid Schottky diodes with excessive reverse-leakage currents particularly at high temperatures. Some ultralow V_F diodes will trade off increased high temperature leakage current for reduced forward voltage. Diode D1

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can have a reverse voltage up to V_{IN} and D2 can have a reverse voltage up to V_{OUT}. The combination of high reverse voltage and current can lead to self heating of the diode. Besides reducing efficiency, this can increase leakage current which increases temperatures even further. Choose packages with lower thermal resistance (θ_{JA}) to minimize self heating of the diodes.

Topside MOSFET Driver Supply (C_{B1}, D_{B1}, C_{B2}, D_{B2})

The top MOSFET drivers (TG1 and TG2) are driven digitally between their respective SW and BOOST pin voltages. The BOOST voltages are biased from floating bootstrap capacitors C_{B1} and C_{B2}, which are normally recharged through external silicon diodes D_{B1} and D_{B2} when the respective top MOSFET is turned off. The capacitors are charged to about 6.3V (about equal to $GATEV_{CC}$) forcing the $V_{BOOST1-SW1}$ and $V_{BOOST2-SW2}$ voltages to be about 6.3V. The boost capacitors C_{B1} and C_{B2} need to store about 100 times the gate charge required by the top switches M1 and M4. In most applications, a 0.1µF to 0.47µF, X5R or X7R dielectric capacitor is adequate. The bypass capacitance from $GATEV_{CC}$ to GND should be at least ten times the C_{B1} or C_{B2} capacitance.

Boost Capacitor Charge Control Block: When the LT8705 operates exclusively in the buck or boost region, one of the top MOSFETS, M1 or M4, can be constantly on. This prevents the respective bootstrap capacitor, C_{B1} or C_{B2}, from being recharged through the silicon diode, D_{B1} or D_{B2}. The Boost Capacitor Charge Control block (see Figure 1) keeps the appropriate BOOST pin charged in these cases. When the M1 switch is always on (boost region), current is automatically drawn from the CSPOUT and/or BOOST2 pins to charge the BOOST1 capacitor as needed. When the M4 switch is always on (buck region) current is drawn from the CSNIN and/or BOOST1 pins to charge the BOOST2 capacitor. Because of this function, CSPIN and CSNIN should be connected to a potential close to V_{IN}. Tie both pins to V_{IN} if they are not being used. Also, CSPOUT and CSNOUT should always be tied to a potential close to V_{OUT}, or be tied directly to V_{OUT} if not being used.

Boost Diodes D_{B1} and D_{B2}: Although Schottky diodes have the benefit of low forward voltage drops, they can exhibit high reverse current leakage and have the potential for thermal runaway under high voltage and temperature conditions. Silicon diodes are thus recommended for diodes D_{B1} and D_{B2}. Make sure that D_{B1} and D_{B2} have reverse breakdown voltage ratings higher than $V_{IN(MAX)}$ and $V_{OUT(MAX)}$ and have less than 1mA of reverse leakage current at the maximum operating junction temperature. Make sure that the reverse leakage current at high operating temperatures and voltages won't cause thermal runaway of the diode.

In some cases it is recommended that up to 5Ω of resistance is placed in series with D_{B1} and D_{B2}. The resistors reduce surge currents in the diodes and can reduce ringing at the SW and BOOST pins of the IC. Since SW pin ringing is highly dependent on PCB layout, SW pin edge rates and the type of diodes used, careful measurements directly at the SW pins of the IC are recommended. If required, a single resistor can be placed between $GATEV_{CC}$ and the common anodes of D_{B1} and D_{B2} (as in the front page application) or by placing separate resistors between the cathodes of each diode and the respective BOOST pins. Excessive resistance in series with D_{B1} and D_{B2} can reduce the BOOST-SW capacitor voltage when the M2 or M3 on-times are very short and should be avoided.

Output Voltage

The LT8705 output voltage is set by an external feedback resistive divider carefully placed across the output capacitor. The resultant feedback signal (FBOUT) is compared with the internal precision voltage reference (typically 1.207V) by the error amplifier EA4. The output voltage is given by the equation:

$$V_{OUT} = 1.207V \bullet \left(1 + \frac{R_{FBOUT1}}{R_{FBOUT2}}\right)$$

where R_{FBOUT1} and R_{FBOUT2} are shown in Figure 1.

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Input Voltage Regulation or Undervoltage Lockout

By connecting a resistor divider between V_{IN}, FBIN and GND, the FBIN pin provides a means to regulate the input voltage or to create an undervoltage lockout function. Referring to error amplifier EA3 in the Block Diagram, when FBIN is lower than the 1.205V reference V_C is pulled low. For example, if V_{IN} is provided by a relatively high impedance source (i.e., a solar panel) and the current draw pulls V_{IN} below a preset limit, V_C will be reduced, thus reducing current draw from the input supply and limiting the voltage drop. Note that using this function in forced continuous mode (MODE pin low) can result in current being drawn from the output and forced into the input. If this behavior is not desired then use discontinuous or Burst Mode operation.

To set the minimum or regulated input voltage use:

$$V_{IN(MIN)} = 1.205V \bullet \left(1 + \frac{R_{FBIN1}}{R_{FBIN2}}\right)$$

where R_{FBIN1} and R_{FBIN2} are shown in Figure 1. Make sure to select R_{FBIN1} and R_{FBIN2} such that FBIN doesn't exceed 30V (absolute maximum rating) under maximum V_{IN} conditions.

This same technique can be used to create an undervoltage lockout if the LT8705 is NOT in forced continuous mode. When in Burst Mode operation or discontinuous mode, forcing V_C low will stop all switching activity. Note that this does not reset the soft-start function, therefore resumption of switching activity will not be accompanied by a soft-start.

Input/Output Current Monitoring and Limiting

The LT8705 has independent input and output current monitor circuits that can be used to monitor and/or limit the respective currents. The current monitor circuits work as shown in Figures 10 and 11.

As described in the Topside MOSFET Driver Supply section, the CSNIN and CSPOUT pins are also connected to the Boost Capacitor Charge Control block (also see Figure 1) and can draw current in certain conditions. In addition,

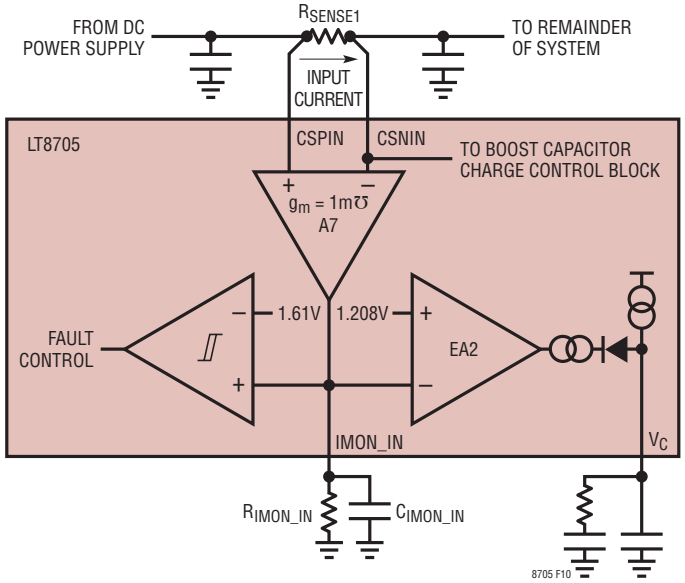

Figure 10. Input Current Monitor and Limit

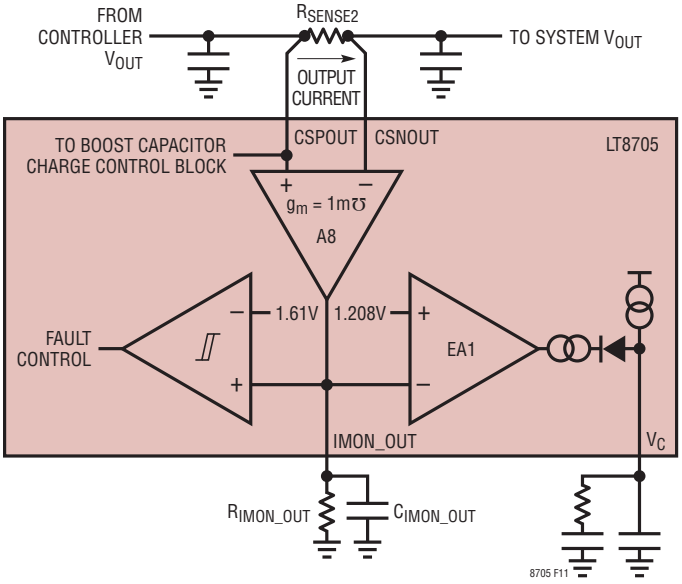

Figure 11. Output Current Monitor and Limit

all four of the current sense pins can draw bias current under normal operating conditions. As such, do not place resistors in series with any of the CSxIN or CSxOUT pins.

Also, because of their use with the Boost Capacitor Charge Control block, tie the CSPIN and CSNIN pins to V_{IN} and tie the IMON_IN pin to ground when the input current

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sensing is not in use. Similarly, the CSPOUT and CSNOUT pins should be tied to V_{OUT} and IMON_OUT should be grounded when not in use.

The remaining discussion refers to the input current monitor circuit. All discussion and equations are applicable to the output current monitor circuit, substituting pin and device names as appropriate.

Current Monitoring: For input current monitoring, current flowing through R_{SENSE1} develops a voltage across CSPIN and CSNIN which is multiplied by 1mA/V (typical), converting it to a current that is forced out of the IMON_IN pin and into resistor R_{IMON_IN} (Note: Negative CSPIN to CSNIN voltages are not multiplied and no current flows out of IMON_IN in that case). The resulting IMON_IN voltage is then proportional to the input current according to:

$$V_{IMON\_IN} = I_{RSENSE1} \bullet \left(R_{SENSE1} \bullet 1m\frac{A}{V} \bullet R_{IMON\_IN} \right)$$

For accurate current monitoring, the CSPIN and CSNIN voltages should be kept above 1.5V (CSPOUT and CSNOUT pins should be kept above 0V). Also, the differential voltage $V_{CSPIN-CSNIN}$ should be kept below 100mV due to the limited amount of current that can be driven out of IMON_IN. Finally, the IMON_IN voltage must be filtered with capacitor C_{IMON_IN} because the input current often has ripple and discontinuities depending on the LT8705's region of operation. C_{IMON_IN} should be chosen by the equation:

$$C_{IMON\_IN} > \left(\frac{100}{f \bullet R_{IMON\_IN}} \right) F$$

where f is the switching frequency, to achieve adequate filtering. Additional capacitance, bringing the C_{IMON_IN} total to 0.1µF to 1µF, may be necessary to maintain loop stability if the IMON_IN pin is used in a constant-current regulation loop.

Current Limiting: As shown in Figure 10, IMON_IN voltages exceeding 1.208V (typical) cause the V_C voltage to reduce, thus limiting the inductor and input currents. R_{IMON_IN} can be selected for a desired input current limit using:

$$R_{IMON\_IN} = \left(\frac{1.208V}{I_{RSENSE(LIMIT)} \bullet 1m\frac{A}{V} \bullet R_{SENSE1}} \right) \Omega$$

For example, if R_{SENSE1} is chosen to be 12.5mΩ and the desired input current limit is 4A then:

$$R_{IMON\_IN} = \frac{1.208V}{4A \bullet 1m\frac{A}{V} \bullet 12.5m\Omega} = 24.2k\Omega$$

Review the Electrical Characteristics and the IMON Output Currents graph in the Typical Performance Characteristics section to understand the operational limits of the IMON_OUT and IMON_IN currents.

Overcurrent Fault: If IMON_IN exceeds 1.61V (typical), a fault will occur and switching activity will stop (see Fault Conditions earlier in the data sheet). The fault current is determined by:

$$I_{RSENSE1(FAULT)} = \left(\frac{1.61V}{1.208V} \bullet I_{RSENSE1(LIMIT)} \right) A$$

For example, an input current limit set to 4A would have a fault current limit of 5.3A.

Output Overvoltage

If the output voltage is higher than the value set by the FBOUT resistor divider, the LT8705 will respond according to the mode and region of operation. In forced continuous mode, the LT8705 will sink current into the input (see the Reverse Current Limit discussion in the Applications Information section for more information). In discontinuous mode and Burst Mode operation, switching will stop and the output will be allowed to remain high.

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$INTV_{CC}$ Regulators and $EXTV_{CC}$ Connection

The LT8705 features two PNP LDOs (low dropout regulators) that regulate the 6.35V (typical) $INTV_{CC}$ pin from either the V_{IN} or $EXTV_{CC}$ supply pin. $INTV_{CC}$ powers the MOSFET gate drivers via the required $GATEV_{CC}$ connection and also powers the LDO33 pin regulator and much of the LT8705's internal control circuitry. The $INTV_{CC}$ LDO selection is determined automatically by the $EXTV_{CC}$ pin voltage. When $EXTV_{CC}$ is lower than 6.22V (typical), $INTV_{CC}$ is regulated from the V_{IN} LDO. After $EXTV_{CC}$ rises above 6.4V (typical), $INTV_{CC}$ is regulated by the $EXTV_{CC}$ LDO instead.

Overcurrent protection circuitry typically limits the maximum current draw from either LDO to 127mA. When $GATEV_{CC}$ and $INTV_{CC}$ are below 4.65V, during start-up or during an overload condition, the typical current limit is reduced to 42mA. The $INTV_{CC}$ pin must be bypassed to ground with a minimum 4.7µF ceramic capacitor placed as close as possible to the $INTV_{CC}$ and GND pins. An additional ceramic capacitor should be placed as close as possible to the $GATEV_{CC}$ and GND pins to provide good bypassing to supply the high transient current required by the MOSFET gate drivers. 1µF to 4.7µF is recommended.

Power dissipated in the $INTV_{CC}$ LDOs must be minimized to improve efficiency and prevent overheating of the LT8705. Since LDO power dissipation is proportional to the input voltage and V_{IN} can be as high as 80V in some applications, the $EXTV_{CC}$ pin is available to regulate $INTV_{CC}$ from a lower input voltage. The $EXTV_{CC}$ pin is connected to V_{OUT} in many applications since V_{OUT} is often regulated to a much lower voltage than the maximum V_{IN}. During start-up, power for the MOSFET drivers, control circuits and the LDO33 pin is derived from V_{IN} until V_{OUT}/$EXTV_{CC}$ rises above 6.4V, after which the power is derived from V_{OUT}/$EXTV_{CC}$. This works well, for example, in a case where V_{OUT} is regulated to 12V and the maximum V_{IN} voltage is 40V. $EXTV_{CC}$ can be floated or grounded when not in use or can also be connected to an external power supply if available.

The maximum current drawn through the $INTV_{CC}$ LDO occurs under the following conditions:

1. Large (capacitive) MOSFETs are being driven at high frequencies.
2. V_{IN} and/or V_{OUT} is high, thus requiring more charge to turn the MOSFET gates on and off.
3. The LDO33 pin output current is high.
4. In some applications, LDO current draw is maximum when the part is operating in the buck-boost region where V_{IN} is close to V_{OUT} since all four MOSFETs are switching.

To check for overheating find the operating conditions that consume the most power in the LT8705 (P_{LT8705}). This will often be under the same conditions just listed that maximize LDO current. Under these conditions monitor the CLKOUT pin duty cycle to measure the approximate die temperature. See the Junction Temperature Measurement section for more information.

Powering $INTV_{CC}$ from V_{OUT}/$EXTV_{CC}$ can also provide enough gate drive when V_{IN} drops as low as 2.8V. This allows the part to operate with a reduced input voltage after the output gets into regulation.

The following list summarizes the three possible connections for $EXTV_{CC}$:

1. $EXTV_{CC}$ left open (or grounded). This will cause $INTV_{CC}$ to be powered from V_{IN} through the internal 6.35V regulator at the cost of a small efficiency penalty.
2. $EXTV_{CC}$ connected directly to V_{OUT} (V_{OUT} > 6.4V). This is the normal connection for the regulator and usually provides the highest efficiency.
3. $EXTV_{CC}$ connected to an external supply. If an external supply is available greater than 6.4V (typical) it may be used to power $EXTV_{CC}$.

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Loop Compensation

The loop stability is affected by a number of factors including the inductor value, output capacitance, load current, V_{IN}, V_{OUT} and the V_C resistor and capacitors. The LT8705 uses internal transconductance error amplifiers driving V_C to help compensate the control loop. For most applications a 3.3nF series capacitor at V_C is a good value. The parallel capacitor (from V_C to GND) is typically 1/10th the value of the series capacitor to filter high frequency noise. A larger V_C series capacitor value may be necessary if the output capacitance is reduced. A good starting value for the V_C series resistor is 20k. Lower resistance will improve stability but will slow the loop response. Use a trim pot instead of a fixed resistor for initial bench evaluation to determine the optimum value.

LDO33 Pin Regulator

The LT8705 includes a low dropout regulator (LDO) to regulate the LDO33 pin to 3.3V. This pin can be used to power external circuitry such as a microcontroller or other desired peripherals. The input supply for the LDO33 pin regulator is $INTV_{CC}$. Therefore $INTV_{CC}$ must have sufficient voltage, typically >4.0V, to properly regulate LDO33. The LDO33 and $INTV_{CC}$ regulators are enabled by the $\overline{SHDN}$ pin and are not affected by SWEN. The LDO33 pin regulator has overcurrent protection circuitry that typically limits the output current to 17.25mA. An undervoltage lockout monitoring LDO disables switching activity when LDO33 falls below 3.04V (typical). LDO33 should be bypassed locally with 0.1µF or more.

Voltage Lockouts

The LT8705 contains several voltage detectors to make sure the chip is under proper operating conditions. Table 1 summarizes the pins that are monitored and also indicates the state that the LT8705 will enter if an under or overvoltage condition is detected.

The conditions are listed in order of priority from top to bottom. If multiple over/undervoltage conditions are detected, the chip will enter the state listed highest on the table.

Table 1: Voltage Lockout Conditions

PIN	APPROXIMATE VOLTAGE CONDITION	CHIP STATE (FIGURE 2)	READ SECTION
V_{IN}	<2.5V	Chip Off	Operation: Start-Up
$\overline{SHDN}$	<1.18V	Chip Off	
$INTV_{CC}$ and $GATEV_{CC}$	<4.65V	Switcher Off	
SWEN	<1.18V	Switcher Off	
LDO33	<3.04	Switcher Off	
IMON_IN	>1.61V	Fault	Operation: Fault Conditions
IMON_OUT	>1.61V	Fault	
FBIN	<1.205V	—	Applications Information: Input Voltage Regulation or Undervoltage Lockout

Due to their accurate thresholds, configurable undervoltage lockouts (UVLOs) can be implemented using the $\overline{SHDN}$, SWEN and in some cases, FBIN pin. The UVLO function sets the turn on/off of the LT8705 at a desired minimum input voltage. For example, a resistor divider can be connected between V_{IN}, $\overline{SHDN}$ and GND as shown in Figures 1 and 14. From the Electrical Characteristics, $\overline{SHDN}$ has typical rising and falling thresholds of 1.234V and 1.184V respectively. The falling threshold for turning off switching activity can be chosen using:

$$R_{SHDN1} = \frac{R_{SHDN2} \bullet \left(V_{(IN,CHIP\_OFF,FALLING)} - 1.184V\right)}{1.184V}\ \Omega$$

For example, choosing R_{SHDN2} = 20k and a falling V_{IN} threshold of 5.42V results in:

$$R_{SHDN1} = \frac{20k\Omega \bullet (5.42V - 1.184V)}{1.184V} = 71.5k\Omega$$

The rising threshold for enabling switching activity would be:

$$V_{(IN,CHIP\_OFF,RISING)} = V_{(IN,CHIP\_OFF,FALLING)} \bullet \frac{1.234V}{1.184V}$$

or 5.65V in this example.

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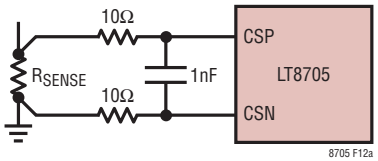
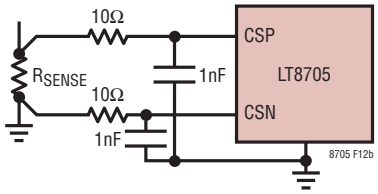
Similar calculations can be used to select a resistor divider connected to SWEN that would stop switching activity during an undervoltage condition. Make sure that the divider doesn't cause SWEN to exceed 7V (absolute maximum rating) under maximum V_{IN} conditions. Using the FBIN pin as an undervoltage lockout is discussed in the Input Voltage Regulation or Undervoltage Lockout section.

Inductor Current Sense Filtering

Certain applications may require filtering of the inductor current sense signals due to excessive switching noise that can appear across R_{SENSE}. Higher operating voltages, higher values of R_{SENSE}, and more capacitive MOSFETs will all contribute additional noise across R_{SENSE} when the SW pins transition. The CSP/CSN sense signals can be filtered by adding one of the RC networks shown in Figures 12a and 12b. Most PC board layouts can be drawn to accommodate either network on the same board. The network should be placed as close as possible to the IC. The network in Figure 12b can reduce common mode noise seen by the CSP and CSN pins of the LT8705 at the expense of some increased ground trace noise as current passes through the capacitors. A short direct path from the capacitor grounds to the IC ground should be used on the PC board. Resistors greater than 10Ω should be avoided as this can increase offset voltages at the CSP/CSN pins. The RC product should be kept to less than 30ns.



(12a)



(12b)

Figure 12. Inductor Current Sense Filter

Junction Temperature Measurement

The duty cycle of the CLKOUT signal is linearly proportional to the die junction temperature, T_J. Measure the duty cycle of the CLKOUT signal and use the following equation to approximate the junction temperature:

$$T_J \cong \frac{DC_{CLKOUT} - 35.9\%}{0.329\%} °C$$

where DC_{CLKOUT} is the CLKOUT duty cycle in % and T_J is the die junction temperature in °C. The actual die temperature can deviate from the above equation by ±10°C

Thermal Shutdown

If the die junction temperature reaches approximately 165°C, the part will go into thermal shutdown. The power switch will be turned off and the $INTV_{CC}$ and LDO33 regulators will be turned off (see Figure 2). The part will be re-enabled when the die temperature has dropped by ~5°C (nominal). After re-enabling, the part will start in the switcher off state as shown in Figure 2. The part will then initialize, perform a soft-start, then enter normal operation as long as the die temperature remains below approximately 165°C.

Efficiency Considerations

The efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Although all dissipative elements in the circuit produce losses, four main sources account for most of the losses in LT8705 circuits:

1. Switching losses. These losses arises from the brief amount of time switch M1 or switch M3 spends in the saturated region during switch node transitions. Power loss depends upon the input voltage, load current, driver strength and MOSFET capacitance, among other factors. See the Power MOSFET Selection and Efficiency Considerations section for more details.

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2. DC I^2R losses. These arise from the resistances of the MOSFETs, sensing resistors, inductor and PC board traces and cause the efficiency to drop at high output currents.

3. $INTV_{CC}$ current. This is the sum of the MOSFET driver current, LDO33 pin current and control currents. The $INTV_{CC}$ regulator's input voltage times the current represents lost power. This loss can be reduced by supplying $INTV_{CC}$ current through the $EXTV_{CC}$ pin from a high efficiency source, such as the output or alternate supply if available. Also, lower capacitance MOSFETs can reduce $INTV_{CC}$ current and power loss.

4. C_{IN} and C_{OUT} loss. The input capacitor has the difficult job of filtering the large RMS input current to the regulator in buck mode. The output capacitor has the more difficult job of filtering the large RMS output current in boost mode. Both C_{IN} and C_{OUT} are required to have low ESR to minimize the AC I^2R loss and sufficient capacitance to prevent the RMS current from causing additional upstream losses in fuses or batteries.

5. Other losses. Schottky diodes D1 and D2 are responsible for conduction losses during dead time and light load conduction periods. Inductor core loss occurs predominately at light loads.

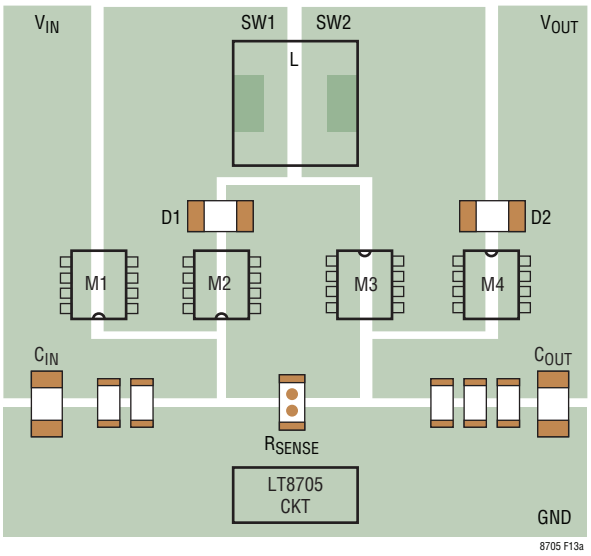
When making adjustments to improve efficiency, the input current is the best indicator of changes in efficiency. If one makes a change and the input current decreases, then the efficiency has increased. If there is no change in input current, then there is no change in efficiency.

Circuit Board Layout Checklist

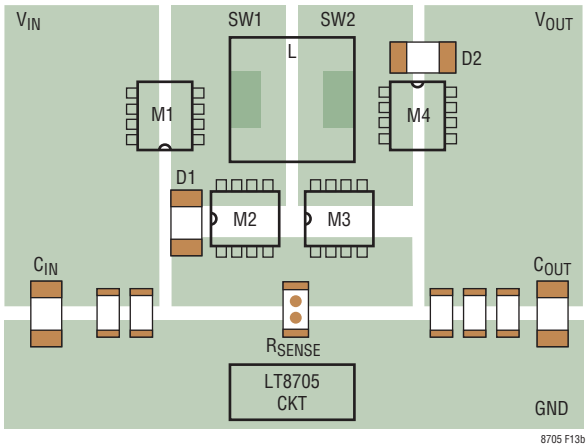
The basic circuit board layout requires a dedicated ground plane layer. Also, for high current, a multilayer board provides heat sinking for power components.

- The ground plane layer should not have any traces and should be as close as possible to the layer with the power MOSFETs.

- The high di/dt path formed by switch M1, switch M2, D1, R_{SENSE} and the C_{IN} capacitor should be compact with short leads and PC trace lengths. The high di/dt path formed by switch M3, switch M4, D2 and the C_{OUT} capacitor also should be compact with short leads and PC trace lengths. Two layout examples are shown in Figures 13a and 13b.



(13a)



(13b)

Figure 13. Switches Layout

APPLICATIONS INFORMATION

- Avoid running signal traces parallel to the traces that carry high di/dt current because they can receive inductively coupled voltage noise. This includes the SW1, SW2, TG1 and TG2 traces to the controller.
- Use immediate vias to connect the components (including the LT8705's GND pins) to the ground plane. Use several vias for each power component.
- Minimize parasitic SW pin capacitance by removing GND and V_{IN} copper from underneath the SW1 and SW2 regions.
- Except under the SW pin regions, flood all unused areas on all layers with copper. Flooding with copper will reduce the temperature rise of power components. Connect the copper areas to a DC net (e.g., quiet GND).
- Partition the power ground from the signal ground. The small-signal component grounds should not return to the IC GND through the power ground path.
- Place switch M2 and switch M3 as close to the controller as possible, keeping the GND, BG and SW traces short.
- Minimize inductance from the sources of M2 and M3 to R_{SENSE} by making the trace short and wide.
- Keep the high dV/dT nodes SW1, SW2, BOOST1, BOOST2, TG1 and TG2 away from sensitive small-signal nodes.
- The output capacitor (–) terminals should be connected as closely as possible to the (–) terminals of the input capacitor.
- Connect the top driver boost capacitor, C_{B1}, closely to the BOOST1 and SW1 pins. Connect the top driver boost capacitor, C_{B2}, closely to the BOOST2 and SW2 pins.
- Connect the input capacitors, C_{IN}, and output capacitors, C_{OUT}, closely to the power MOSFETs. These capacitors carry the MOSFET AC current in the boost and buck regions.
- Connect the FBOUT and FBIN pin resistor dividers to the (+) terminals of C_{OUT} and C_{IN} respectively. Small FBOUT/FBIN bypass capacitors may be connected closely to the LT8705's GND pin if needed. The resistor connections should not be along the high current or noise paths.
- Route current sense traces (CSP/CSN, CSPIN/CSNIN, CSPOUT/CSNOUT) together with minimum PC trace spacing. Avoid having sense lines pass through noisy areas, such as switch nodes. The optional filter network capacitor between CSP and CSN should be as close as possible to the IC. Ensure accurate current sensing with Kelvin connections at the R_{SENSE} resistors.
- Connect the V_C pin compensation network closely to the IC, between V_C and the signal ground pins. The capacitor helps to filter the effects of PCB noise and output voltage ripple voltage from the compensation loop.
- Connect the $INTV_{CC}$ and $GATEV_{CC}$ bypass capacitors close to the IC. The capacitors carry the MOSFET drivers' current peaks.

Design Example

V_{IN} = 8V to 25V

V_{OUT} = 12V

$I_{OUT(MAX)}$ = 5A

f = 350kHz

Maximum ambient temperature = 60°C

APPLICATIONS INFORMATION

R_T Selection: Choose the R_T resistor for the free-running oscillator frequency using:

$$R_T = \left(\frac{43{,}750}{f_{OSC}} - 1\right) k\Omega = \left(\frac{43{,}750}{350} - 1\right) = 124k\Omega$$

R_{SENSE} Selection: Start by calculating the maximum duty cycle in the boost region:

$$DC_{(MAX,M3,BOOST)} \cong \left(1 - \frac{V_{IN(MIN)}}{V_{OUT(MAX)}}\right) \bullet 100\%$$

$$= \left(1 - \frac{8V}{12V}\right) \bullet 100\% = 33\%$$

Next, from the Maximum Inductor Current Sense Voltage vs Duty Cycle graph in the Typical Performance Characteristics section:

$$V_{RSENSE(MAX,BOOST,MAX)} \cong 107mV$$

Next, estimate the maximum and minimum inductor current ripple in the boost and buck regions respectively:

$$\Delta I_{L(MAX,BOOST)} \cong \frac{V_{OUT(MAX)} \bullet I_{OUT(MAX,BOOST)}}{V_{IN(MIN)} \bullet \left(\frac{100\%}{\%Ripple} - 0.5\right)} A$$

$$= \frac{12V \bullet 5A}{8V \bullet \left(\frac{100\%}{40\%} - 0.5\right)} = 3.75A$$

$$\Delta I_{L(MIN,BUCK)} \cong \frac{I_{OUT(MAX,BUCK)}}{\left(\frac{100\%}{10\%} - 0.5\right)} A$$

$$= \frac{5A}{\left(\frac{100\%}{10\%} - 0.5\right)} = 0.53A$$

Now calculate the maximum R_{SENSE} values in the boost and buck regions to be:

$$R_{SENSE(MAX,BOOST)} =$$

$$\frac{2 \bullet V_{RSENSE(MAX,BOOST,MAX)} \bullet V_{IN(MIN)}}{\left(2 \bullet I_{OUT(MAX,BOOST)} \bullet V_{OUT(MIN)}\right) + \left(\Delta I_{L(MAX,BOOST)} \bullet V_{IN(MIN)}\right)} \Omega$$

$$= \frac{2 \bullet 107mV \bullet 8V}{(2 \bullet 5A \bullet 12V) + (3.75A \bullet 8V)} = 11.4m\Omega$$

$$R_{SENSE(MAX,BUCK)} = \frac{2 \bullet 86mV}{\left(2 \bullet I_{OUT(MAX,BUCK)}\right) - \Delta I_{L(MIN,BUCK)}} \Omega$$

$$= \frac{2 \bullet 86mV}{(2 \bullet 5A) - 0.53A} = 18.2m\Omega$$

Adding an additional 30% margin, choose R_{SENSE} to be 11.4mΩ/1.3 = 8.7mΩ.

Inductor Selection: With R_{SENSE} known, we can now determine the minimum inductor value that will provide adequate load current in the boost region using:

$$L_{(MIN1,BOOST)} \cong$$

$$\frac{V_{IN(MIN)} \bullet \frac{DC_{(MAX,M3,BOOST)}}{100\%}}{2 \bullet f \bullet \left(\frac{V_{RSENSE(MAX,BOOST,MAX)}}{R_{SENSE}} - \frac{I_{OUT(MAX)} \bullet V_{OUT(MAX)}}{V_{IN(MIN)}}\right)} H$$

$$= \frac{8V \bullet \left(\frac{33\%}{100\%}\right)}{2 \bullet 350kHz \bullet \left(\frac{107mV}{8.7m\Omega} - \frac{5A \bullet 12V}{8V}\right)} = 0.8\mu H$$

APPLICATIONS INFORMATION

To avoid subharmonic oscillations in the inductor current, choose the minimum inductance according to:

$$L_{(MIN2,BOOST)} = \frac{\left[V_{OUT(MAX)} - \left(\frac{V_{IN(MIN)} \bullet V_{OUT(MAX)}}{V_{OUT(MAX)} - V_{IN(MIN)}}\right)\right] \bullet R_{SENSE}}{0.08 \bullet f} H$$

$$= \frac{\left[12V - \left(\frac{8V \bullet 12V}{12V - 8V}\right)\right] \bullet 8.7m\Omega}{0.08 \bullet 350kHz} = -3.7\mu H$$

$$L_{(MIN1,BUCK)} = \frac{V_{IN(MAX)} \bullet \left(1 - \frac{V_{OUT(MAX)}}{V_{IN(MAX)} - V_{OUT(MIN)}}\right) \bullet R_{SENSE}}{0.08 \bullet f}$$

$$= \frac{25V \bullet \left(1 - \frac{12V}{25V - 12V}\right) \bullet 8.7m\Omega}{0.08 \bullet 350kHz} = 0.6\mu H$$

The inductance must be higher than all of the minimum values calculated above. We will choose a 10µH standard value inductor for improved margin.

MOSFET Selection: The MOSFETs are selected based on voltage rating, C_{RSS} and $R_{DS(ON)}$ value. It is important to ensure that the part is specified for operation with the available gate voltage amplitude. In this case, the amplitude is 6.35V and MOSFETs with an $R_{DS(ON)}$ value specified at V_{GS} = 4.5V can be used.

Select M1 and M2: With 25V maximum input voltage, MOSFETs with a rating of at least 30V are used. As we do not yet know the actual thermal resistance (circuit board design and airflow have a major impact) we assume that the MOSFET thermal resistance from junction to ambient is 50°C/W.

If we design for a maximum junction temperature, $T_{J(MAX)}$ = 125°C, the maximum allowable power dissipation can be calculated. First, calculate the maximum power dissipation:

$$P_{D(MAX)} = \frac{T_{J(MAX)} - T_{A(MAX)}}{R_{TH(JA)}}$$

$$P_{D(MAX)} = \frac{125°C - 60°C}{50°C/W} = 1.3W$$

Since maximum I^2R power dissipation in the boost region happens when V_{IN} is minimum, we can determine the maximum allowable $R_{DS(ON)}$ for the boost region using:

$$P_{M1} = P_{I^2R} \cong \left(\left(\frac{V_{OUT}}{V_{IN}} \bullet I_{OUT}\right)^2 \bullet R_{DS(ON)} \bullet \rho_\tau\right) W$$

$$1.3W \cong \left(\left(\frac{12V}{8V} \bullet 5A\right)^2 \bullet R_{DS(ON)} \bullet 1.5\right) W \text{ and therefore}$$

$$R_{DS(ON)} < 15.4m\Omega$$

The Fairchild FDMS7672 meets the specifications with a maximum $R_{DS(ON)}$ of ~6.9mΩ at V_{GS} = 4.5V (~10mΩ at 125°C). Checking the power dissipation in the buck region with V_{IN} maximum and V_{OUT} minimum yields:

$$P_{M1} = P_{I^2R} + P_{SWITCHING}$$

$$\cong \left(\left(\frac{V_{OUT}}{V_{IN}} \bullet I_{OUT}\right)^2 \bullet R_{DS(ON)} \bullet \rho_\tau\right) + \left(V_{IN} \bullet I_{OUT} \bullet f \bullet t_{RF1}\right) W$$

$$P_{M1} \cong \left(\left(\frac{12V}{25V} \bullet 5A\right)^2 \bullet 6.9m\Omega \bullet 1.5\right) + (25V \bullet 5A \bullet 350k \bullet 20ns)$$

$$= 0.06W + 0.88W = 0.94W$$

The maximum switching power of 0.88W can be reduced by choosing a slower switching frequency. Since this calculation is approximate, measure the actual rise and fall times on the PCB to obtain a better power estimate.

The maximum dissipation in M2 occurs at maximum input voltage when the circuit is operating in the buck region. Using the 6.9mΩ Fairchild FDMS7672 the dissipation is:

$$P_{(M2,BUCK)} \cong \left(\frac{V_{IN} - V_{OUT}}{V_{IN}} \bullet I_{OUT(MAX)}^2 \bullet R_{DS(ON)} \bullet \rho_\tau\right) W$$

$$P_{(M2,BUCK)} \cong \left(\frac{25V - 12V}{25V} \bullet (5A)^2 \bullet 6.9m\Omega \bullet 1.5\right) = 0.13W$$

APPLICATIONS INFORMATION

Select M3 and M4: With 12V output voltage we need MOSFETs with 20V or higher rating.

The highest dissipation occurs in the boost region when input voltage is minimum and output current is highest. For switch M3 the dissipation is:

$$P_{M3} = P_I{}^2R + P_{SWITCHING} \cong$$

$$\left(\frac{(V_{OUT} - V_{IN}) \bullet V_{OUT}}{V_{IN}{}^2} \bullet I_{OUT}{}^2 \bullet R_{DS(ON)} \bullet \rho_\tau \right)$$

$$+ \left(V_{OUT}{}^2 \bullet I_{OUT} \bullet f \bullet \frac{t_{RF2}}{V_{IN}} \right) W$$

as described in the Power MOSFET Selection and Efficiency Considerations section.

The maximum dissipation in switch M4 is:

$$P_{(M4,BOOST)} \cong \left(\frac{V_{OUT(MAX)}}{V_{IN(MIN)}} \bullet I_{OUT}{}^2 \bullet \rho_\tau \bullet R_{DS(ON)} \right) W$$

The Fairchild FDMS7672 can also be used for M3 and M4. Assuming 20ns rise and fall times, the calculated power loss at the minimum 8V input voltage is then 0.82W for M3 and 0.39W for M4

Output Voltage: Output voltage is 12V. Select R_{FBOUT2} as 20k. R_{FBOUT1} is:

$$R_{FBOUT1} = \left(\frac{V_{OUT}}{1.207V} - 1 \right) \bullet R_{FBOUT2}$$

Select R_{FBOUT1} as 178k. Both R_{FBOUT1} and R_{FBOUT2} should have a tolerance of no more than 1%.

Capacitors: A low ESR (5mΩ) capacitor network for C_{IN} is selected. In this mode, the maximum ripple is:

$$\Delta V_{(BUCK,ESR)} \cong \frac{V_{IN(MAX)} \bullet I_{OUT(MAX)}}{V_{OUT(MIN)}} \bullet ESR$$

$$\Delta V_{(BUCK,ESR)} \cong \frac{25V \bullet 5A}{12V} \bullet 5m\Omega = 52mV$$

assuming ESR dominates the ripple.

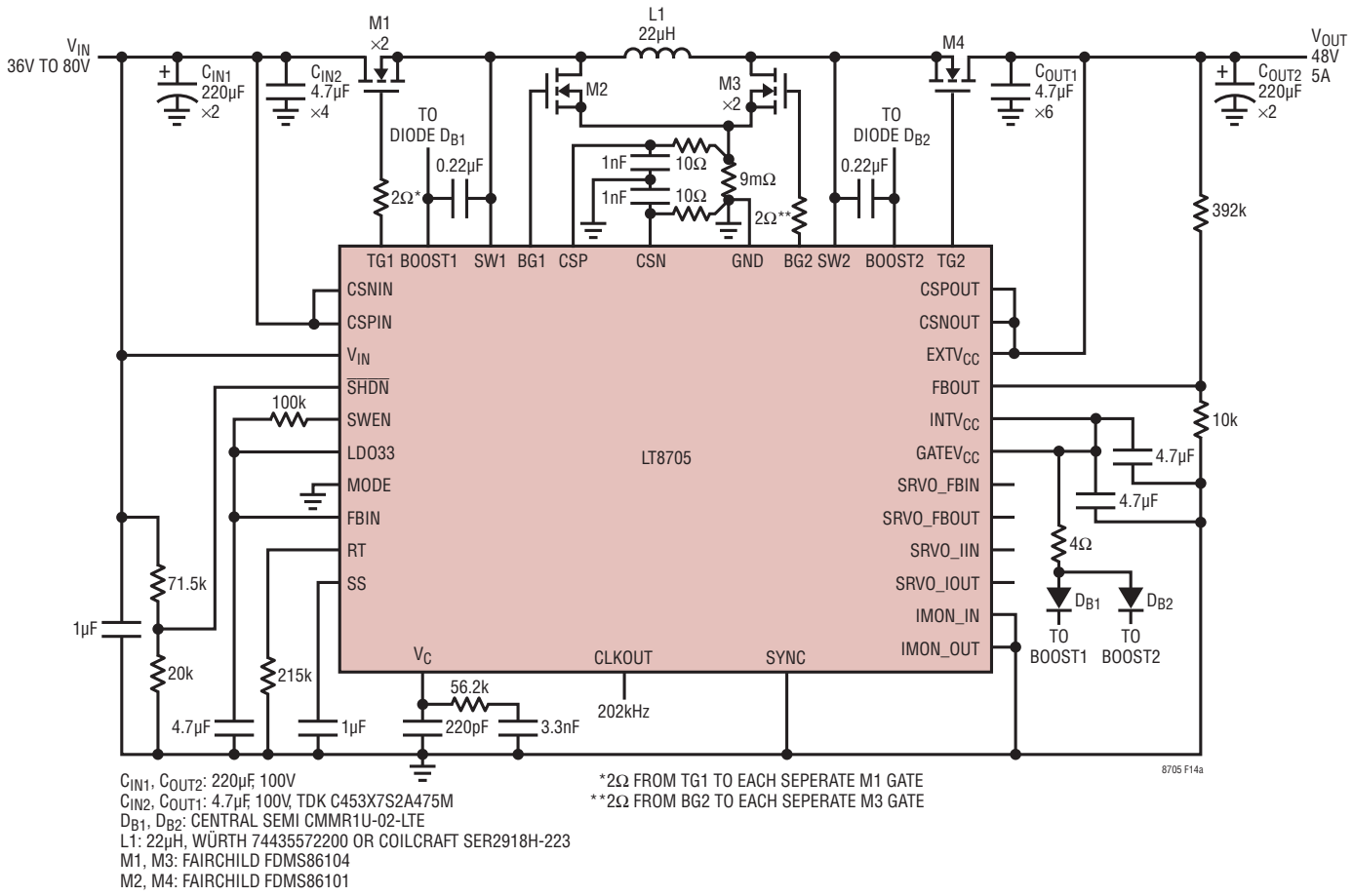
Having 5mΩ of ESR for the C_{OUT} network sets the maximum output voltage ripple at:

$$\Delta V_{(BOOST,ESR)} \cong \frac{V_{OUT(MAX)} \bullet I_{OUT(MAX)}}{V_{IN(MIN)}} \bullet ESR$$

$$\Delta V_{(BOOST,ESR)} \cong \frac{12V \bullet 5A}{8V} \bullet 5m\Omega = 37.5mV$$

assuming ESR dominates the ripple.

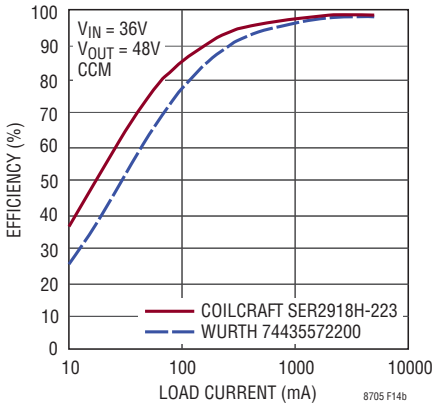
TYPICAL APPLICATIONS



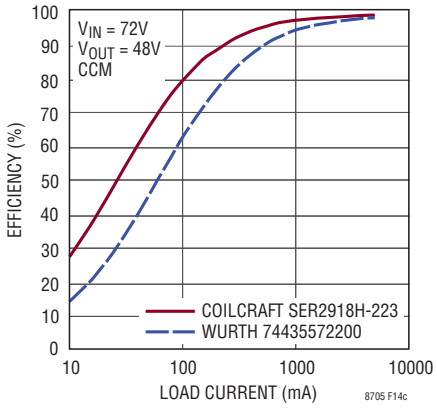
CIN1, COUT2: 220µF, 100V
CIN2, COUT1: 4.7µF, 100V, TDK C453X7S2A475M
DB1, DB2: CENTRAL SEMI CMMR1U-02-LTE
L1: 22µH, WÜRTH 74435572200 OR COILCRAFT SER2918H-223
M1, M3: FAIRCHILD FDMS86104
M2, M4: FAIRCHILD FDMS86101

*2Ω FROM TG1 TO EACH SEPERATE M1 GATE
**2Ω FROM BG2 TO EACH SEPERATE M3 GATE

Efficiency vs Output Current (Boost Region)



Efficiency vs Output Current (Buck Region)

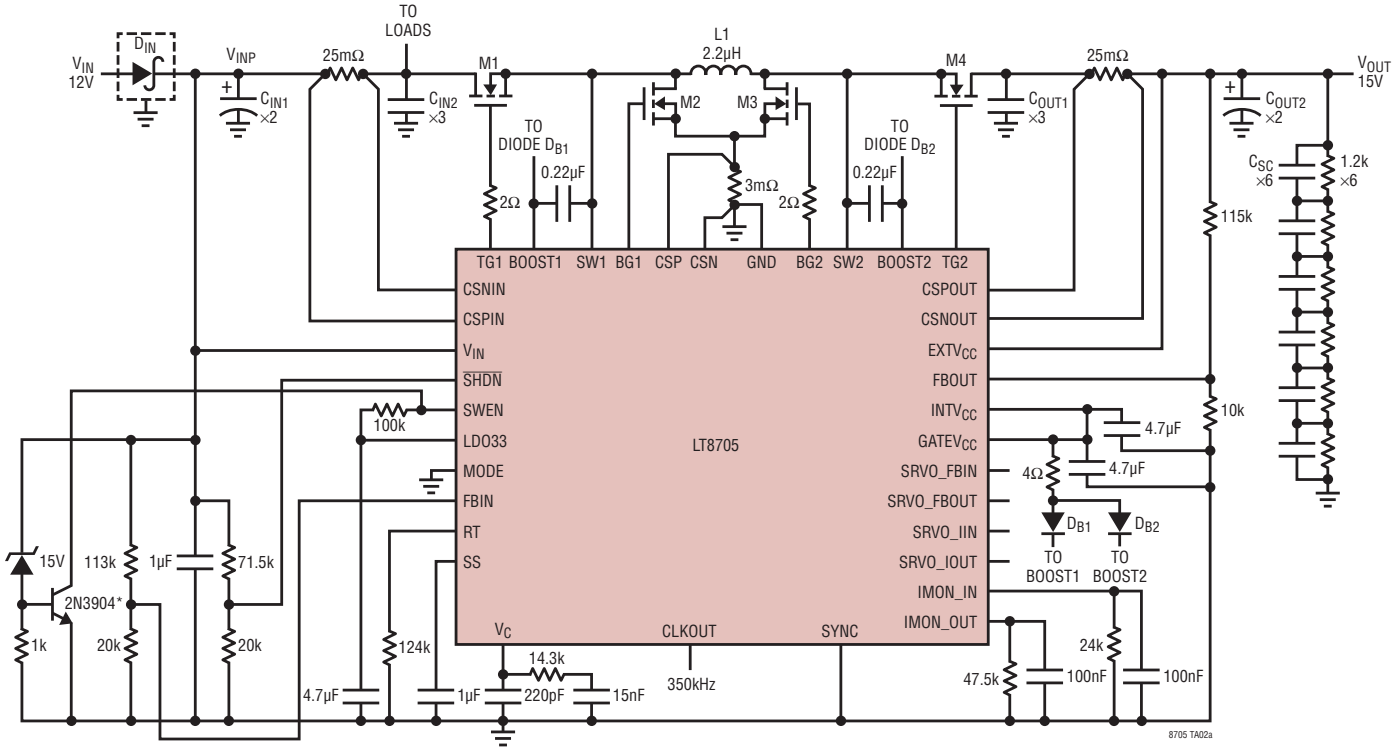


Note: See the front page and the Typical Performance Characteristics section for more curves from this application circuit using the Coilcraft inductor. The smaller Würth inductor is also suitable in place of the Coilcraft inductor with some loss in efficiency.

Figure 14. Telecom Voltage Stabilizer

APPLICATIONS INFORMATION

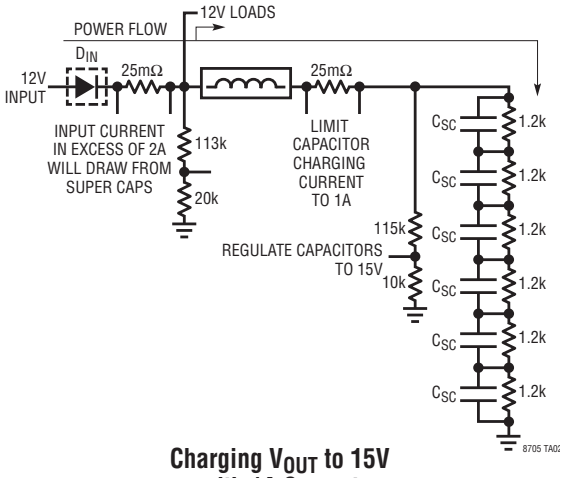
Supercapacitor Backup Supply

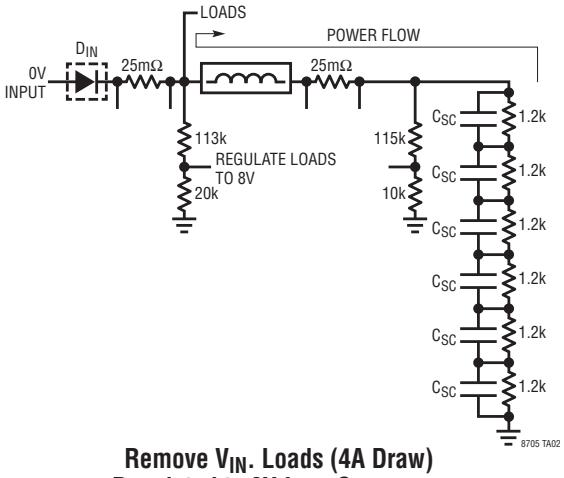


CIN1, COUT2: 100µF, 20V SANYO OS-CON 205A100M
CIN2, COUT1: 22µF, 25V, TDK C4532X741E226M
CSC: 60F, 2.5V COOPER BUSSMAN HB1840-2R5606-R

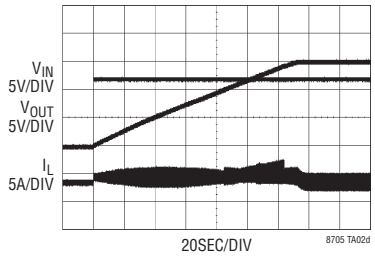
DIN: APPROPRIATE 2A SCHOTTKY DIODE OR IDEAL DIODE SUCH AS LTC4358, LTC4412, LTC4352, ETC.
DB1, DB2: CENTRAL SEMI CMMR1U-02-LTE
L1: 2.2µH, VISHAY IHLP-5050CE-01-2R2-M-01
M1-M4: FAIRCHILD FDMS7698

*INPUT SIDE OVERVOLTAGE PROTECTION WHEN CONVERTER IS DRAWING CURRENT FROM THE SUPER CAPACITORS

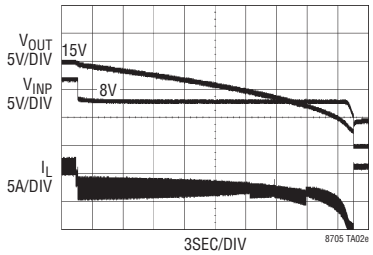




Charging V_{OUT} to 15V with 1A Current



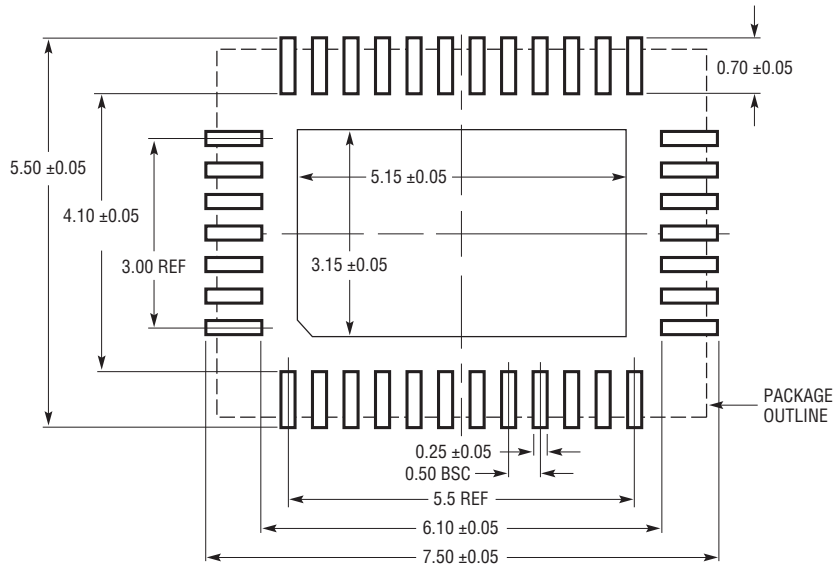
Remove V_{IN}. Loads (4A Draw) Regulated to 8V from Supercaps



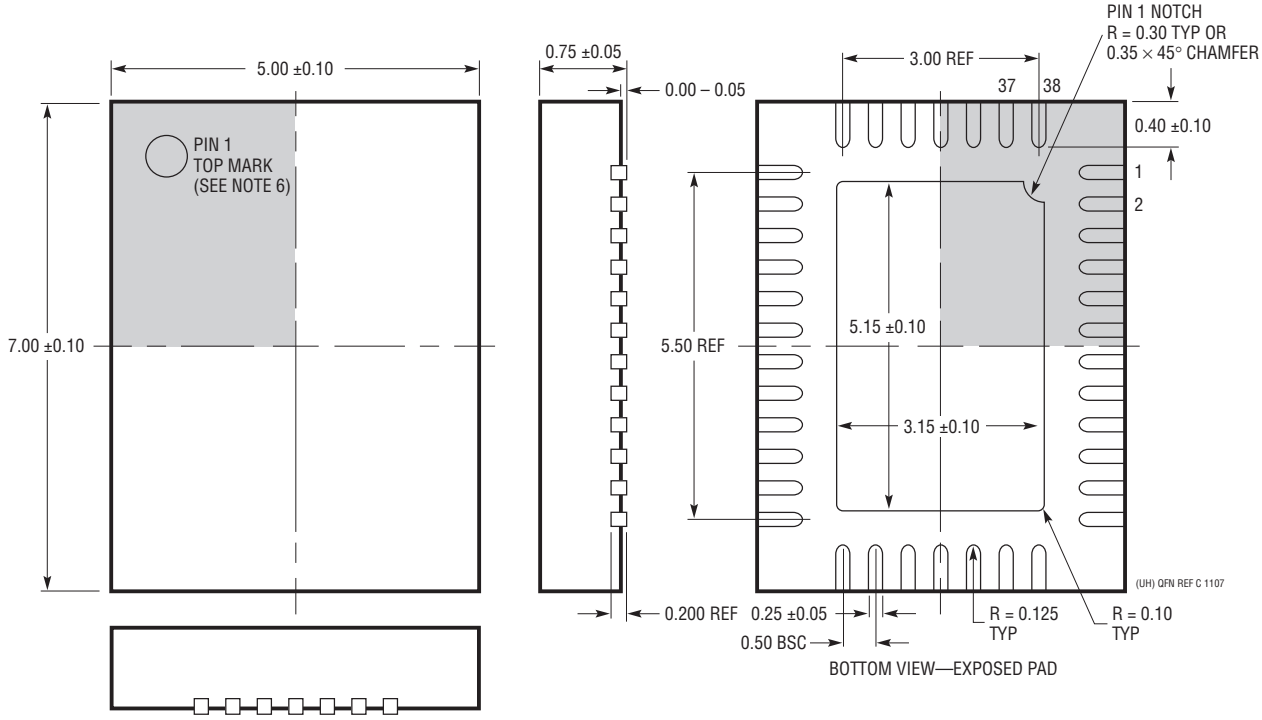
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

UHF Package
38-Lead Plastic QFN (5mm × 7mm)
(Reference LTC DWG # 05-08-1701 Rev C)



RECOMMENDED SOLDER PAD LAYOUT
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED

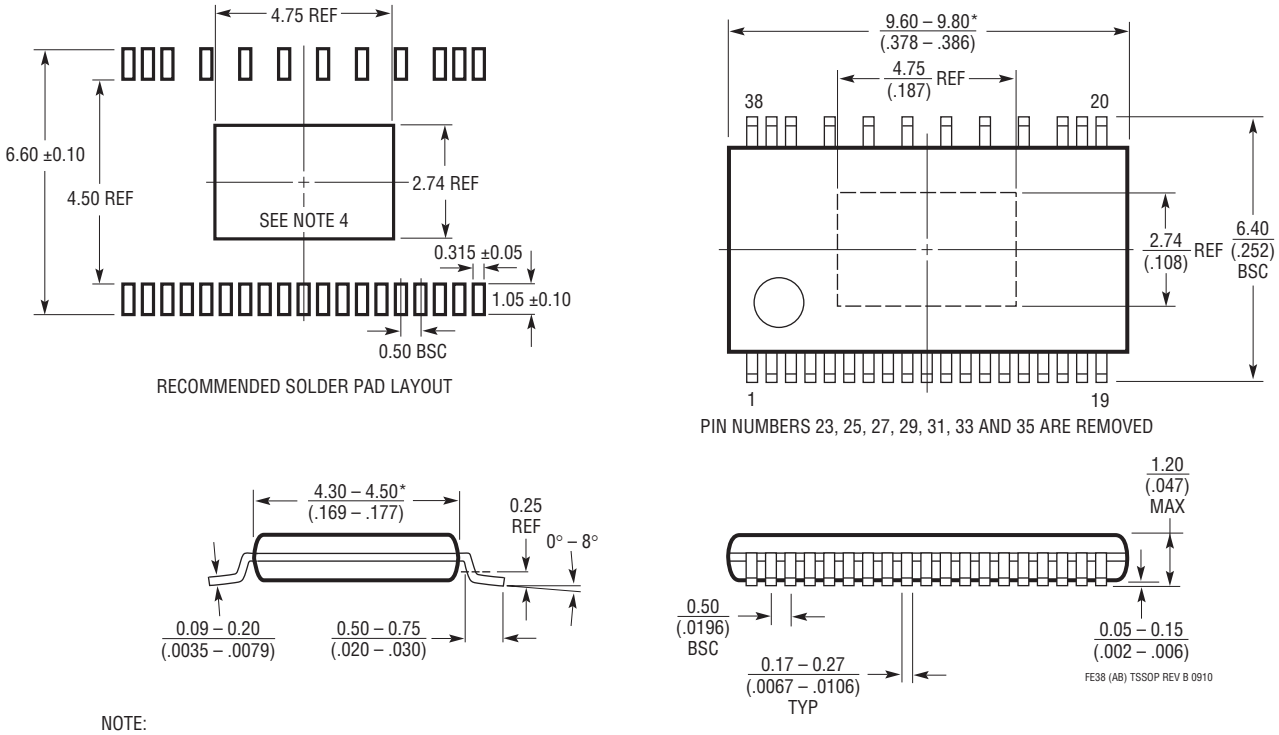


NOTE:
1. DRAWING CONFORMS TO JEDEC PACKAGE OUTLINE M0-220 VARIATION WHKD
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

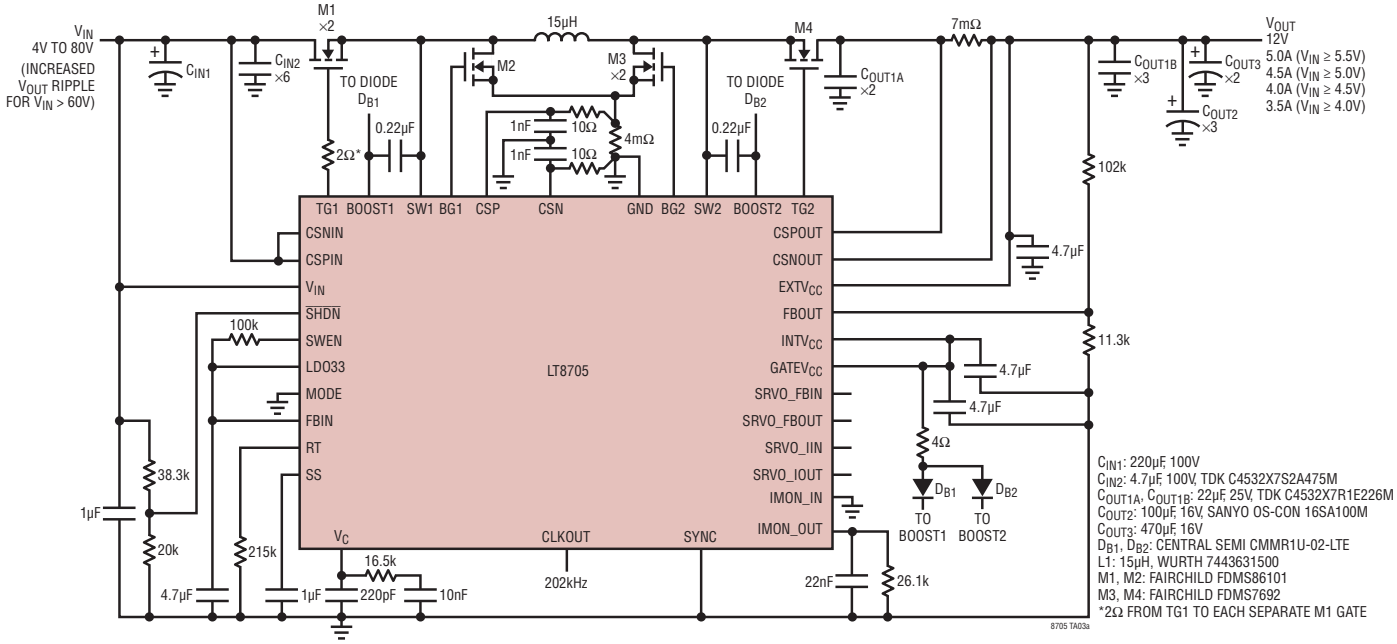
FE Package
Package Variation: FE38 (31)
38-Lead Plastic TSSOP (4.4mm)
(Reference LTC DWG # 05-08-1665 Rev B)
Exposed Pad Variation AB



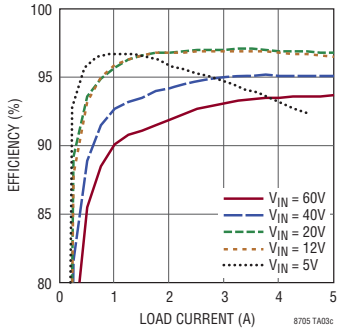
NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN MILLIMETERS (INCHES)
3. DRAWING NOT TO SCALE
4. RECOMMENDED MINIMUM PCB METAL SIZE FOR EXPOSED PAD ATTACHMENT
*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.150mm (.006") PER SIDE

TYPICAL APPLICATION

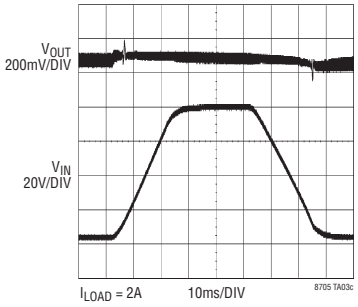
12V Output Converter Accepts 4V to 80V Input (5.5V Minimum to Start)



Efficiency vs Output Current



Input Transient (4V to 80V)



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT3791-1	60V High Efficiency (Up to 98%) Synchronous 4-Switch Buck-Boost DC/DC Controller	4.7V ≤ V_{IN} ≤ 60V, 1.2V ≤ 60V, Regulates V_{OUT}, I_{OUT} or I_{IN}, TSSOP-38
LTC3789	High Efficiency (Up to 98%) Synchronous 4-Switch Buck-Boost DC/DC Controller	4V ≤ V_{IN} ≤ 38V, 0.8V ≤ V_{OUT} ≤ 38V, SSOP-28, 4mm × 5mm QFN-28
LT3758	High Input Voltage, Boost, Flyback, SEPIC and Inverting Controller	5.5V ≤ V_{IN} ≤ 100V, Positive or Negative V_{OUT}, 3mm × 3mm DFN-10 or MSOP-10E
LTC3115-1	40V, 2A Synchronous Buck-Boost DC/DC Converter	2.7V ≤ V_{IN} ≤ 40V, 2.7V ≤ V_{OUT} ≤ 40V, 4mm × 5mm DFN-16, TSSOP-20
LTM4609	High Efficiency Buck-Boost DC/DC µModule Regulator	4.5V ≤ V_{IN} ≤ 36V, 0.8V ≤ V_{OUT} ≤ 34V, 15mm × 15mm × 2.8mm

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