

4-bit dual supply level translator without direction control pin

Datasheet –production data

Features

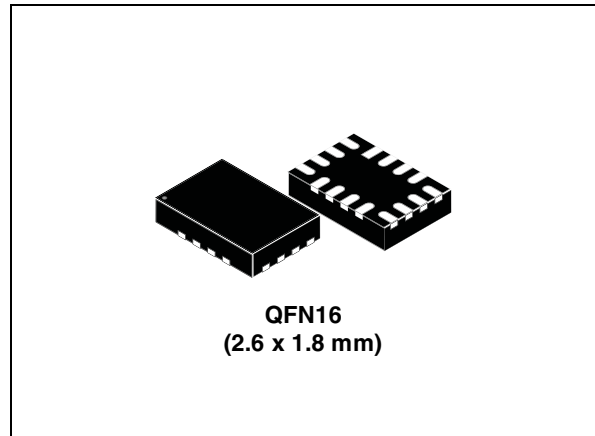
- 42 MHz: 84 Mbps (max.) data rate at $V_L = 1.8\text{ V}$, $V_{CC} = 3.3\text{ V}$
- Bi-directional level translation without direction control pin
- Wide voltage range ($V_{CC} \geq V_L$):
 - V_L ranges from 1.65 to 3.6 V
 - V_{CC} ranges from V_L to 5.5 V
- Power-down mode feature - when V_{CC} supply is off, all I/Os are in high impedance
- Totem pole driving
- 5.5 V tolerant enable pin
- ESD performance on all pins: $\pm 2\text{ kV HBM}$
- Small package and footprint QFN16 (2.6 x 1.8 mm) package

Applications

- Low-voltage system level translation
- Mobile phones and other mobile devices

Description

The ST2149 is a 4-bit dual supply level translator which provides the level shifting capability to allow data transfer in a multi-voltage system. Externally applied voltages, V_{CC} and V_L , set the logic levels on either side of the device. Its architecture allows bi-directional level translation without a control pin.



The ST2149 accepts V_L from 1.65 to 3.6 V and V_{CC} from 1.65 to 5.5 V, making it ideal for data transfer between low-voltage ASICs/PLD and higher voltage systems. This device has a tri-state output mode which can be used to disable all I/Os.

The ST2149 supports power-down mode when V_{CC} is grounded/floating or when the device is disabled via the OE pin.

Table 1. Device summary

Order code	Package	Packaging
Root part number 1QTR	QFN16 (2.6 x 1.8 mm)	Tape and reel (3000 parts per reel)

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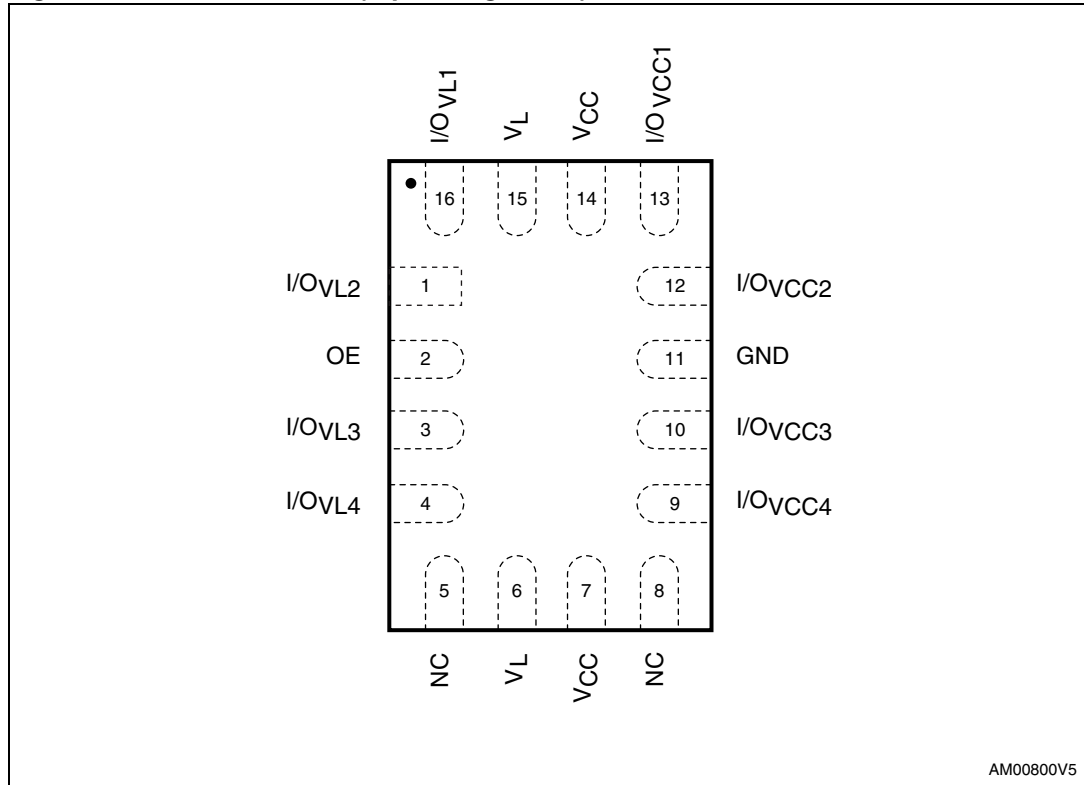
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1 Pin settings

1.1 Pin connection

Figure 1. Pin connection (top through view)



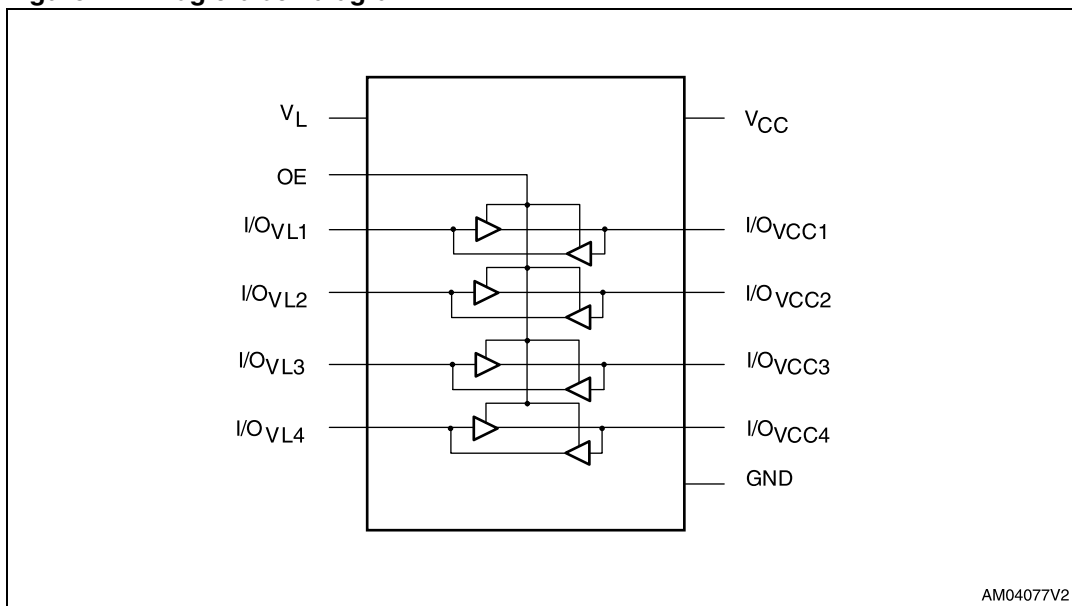
1.2 Pin description

Table 2. Pin description

Pin number	Symbol	Name and function
1	I/O _{VL2}	Data input/output
2	OE	Output enable
3	I/O _{VL3}	Data input/output
4	I/O _{VL4}	Data input/output
5	NC	No connection
6	V _L	Supply voltage
7	V _{CC}	Supply voltage
8	NC	No connection
9	I/O _{VCC4}	Data input/output
10	I/O _{VCC3}	Data input/output
11	GND	Ground
12	I/O _{VCC2}	Data input/output
13	I/O _{VCC1}	Data input/output
14	V _{CC}	Supply voltage
15	V _L	Supply voltage
16	I/O _{VL1}	Data input/output

2 Logic diagram

Figure 2. Logic block diagram



Device block diagrams

Figure 3. ST2149 block diagram

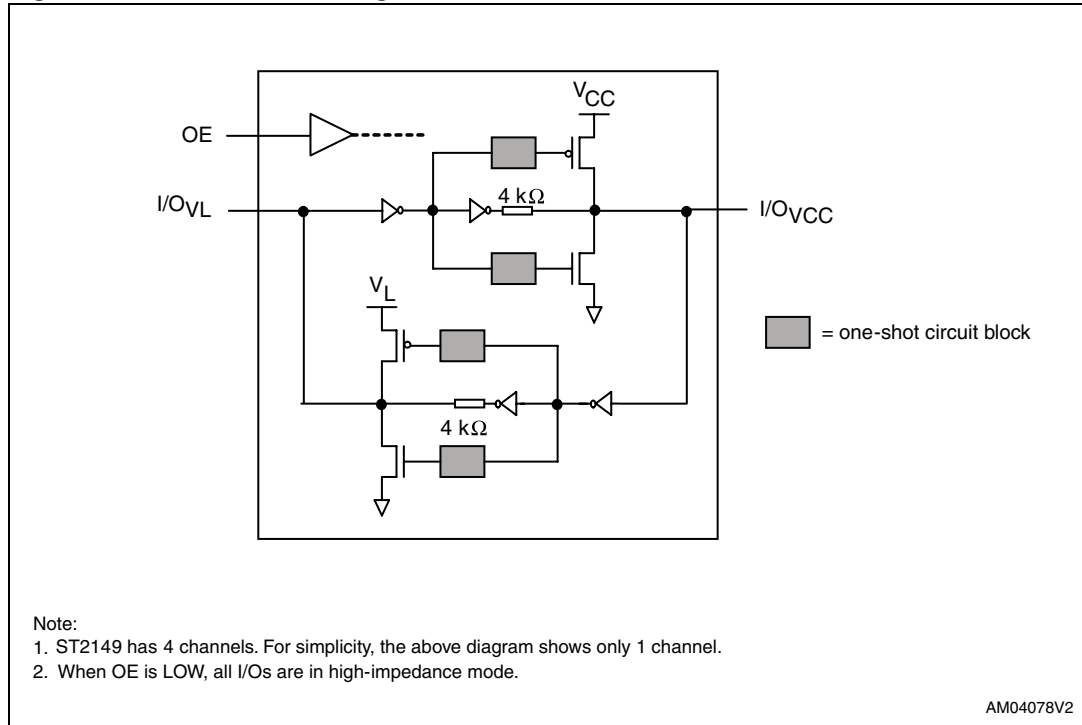
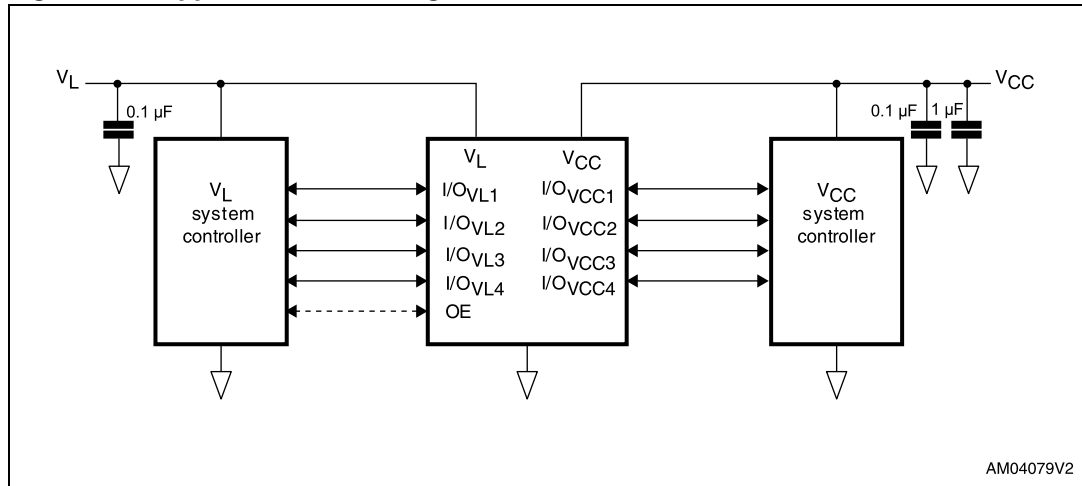


Figure 4. Application block diagram



3 Supplementary notes

3.1 Driver requirements

For proper operation, the driver from each side of the device must be able to source and sink a minimum of 1 mA current. The device architecture requires the driver to source/sink maximum current of ($V_{CC}/4$) mA to/from the weak 4 k Ω output buffer.

3.2 Load driving capability

To support the architecture that allows level translation without the direction pin, the one-shot transistor is turned ON only during state transition at the output side. After the one-shot transistor is turned OFF, only the 4 k Ω resistor maintains the state. So, a resistive load or pull-up resistor less than 50 k Ω is not recommended for proper operation.

3.3 Power-off feature

In some applications it may be required to turn off one of the power supplies powering up the level translator. The device is automatically disabled when V_{CC} supply is turned OFF, even if the OE pin is set to HIGH (enabled). In this mode, all I/Os are in high impedance state.

3.4 Truth table

Table 3. Truth table

Enable	Bi-directional Input/output	
OE	I/O $_{VCC}$	I/O $_{VL}$
H ⁽¹⁾	H ⁽²⁾	H ⁽¹⁾
H ⁽¹⁾	L	L
L	Z ⁽³⁾	Z ⁽³⁾

1. High-level V_L power supply referred.
2. High-level V_{CC} power supply referred.
3. Z = high impedance.

4 Maximum ratings

Stressing the device above the ratings listed in [Table 4](#) may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in [Recommended operating conditions](#) of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V _L	Supply voltage	-0.3 to 4.6	V
V _{CC}	Supply voltage	-0.3 to 6.5	V
V _{OE}	DC control input voltage	-0.3 to 6.5	V
V _{I/OVL}	DC I/O _{VL} input voltage (OE = GND or V _L)	-0.3 to V _L + 0.3	V
V _{I/OVCC}	DC I/O _{VCC} input voltage (OE = GND or V _L)	-0.3 to V _{CC} + 0.3	V
I _{IK}	DC input diode current	-20	mA
I _{I/OVL}	DC output current	±25	mA
I _{I/OVCC}	DC output current	±25	mA
I _{SC} TOUT	Short-circuit duration, continuous	40	mA
P _D	Power dissipation	500	mW
T _{STG}	Storage temperature	-65 to 150	°C
T _L	Lead temperature (10 seconds)	300	°C
ESD	Electrostatic discharge protection (HBM)	±2	kV

Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V _L	Supply voltage	1.65	–	3.6	V
V _{CC}	Supply voltage	V _L	–	5.5	V
V _{OE}	Input voltage (OE output enable pin, V _L power supply referred)	0	–	3.6	V
V _{I/OVL}	I/O _{VL} voltage	0	–	V _L	V
V _{I/OVCC}	I/O _{VCC} voltage	0	–	V _{CC}	V
T _{OP}	Operating temperature	-40	–	85	°C
dt/dV	Input rise and fall time	0	–	1	ns/V

5 Electrical characteristics

Over recommended operating conditions unless otherwise noted. All typical values are at $T_A = 25\text{ }^\circ\text{C}$.

Table 6. DC characteristics

Symbol	Parameter	V_L	V_{CC}	Test conditions	Value					Unit
					$T_A = 25\text{ }^\circ\text{C}$			$-40\text{ to }85\text{ }^\circ\text{C}$		
					Min.	Typ.	Max.	Min.	Max.	
V_{IHL}	High-level input voltage (I/O_{VL})	1.65	1.65 to 5.5		1.16	–	–	1.16	–	V
		1.8			1.26	–	–	1.26	–	
		2.5			1.75	–	–	1.75	–	
		3.0			2.10	–	–	2.10	–	
		3.6			2.52	–	–	2.52	–	
V_{ILL}	Low-level input voltage (I/O_{VL})	1.65	1.65 to 5.5		–	–	0.50	–	0.50	V
		1.8			–	–	0.54	–	0.54	
		2.5			–	–	0.75	–	0.75	
		3.0			–	–	0.90	–	0.90	
		3.6			–	–	1.08	–	1.08	
V_{IHC}	High-level input voltage (I/O_{VCC})	1.65 to 3.6	1.65		1.16	–	–	1.16	–	V
			1.8		1.26	–	–	1.26	–	
			2.5		1.75	–	–	1.75	–	
			3.0		2.10	–	–	2.10	–	
			3.6		2.52	–	–	2.52	–	
			4.3		3.01	–	–	3.01	–	
			5.5		3.85	–	–	3.85	–	
V_{ILC}	Low-level input voltage (I/O_{VCC})	1.65 to 3.6	1.65		–	–	0.50	–	0.50	V
			1.8		–	–	0.54	–	0.54	
			2.5		–	–	0.75	–	0.75	
			3.0		–	–	0.90	–	0.90	
			3.6		–	–	1.08	–	1.08	
			4.3		–	–	1.29	–	1.29	
			5.5		–	–	1.65	–	1.65	

Table 6. DC characteristics (continued)

Symbol	Parameter	V _L	V _{CC}	Test conditions	Value					Unit
					T _A = 25 °C			-40 to 85 °C		
					Min.	Typ.	Max.	Min.	Max.	
V _{IH-OE}	High-level input voltage (OE)	1.65	1.65 to 5.5		1.16	–	–	1.16	–	V
		1.8			1.26	–	–	1.26	–	
		2.5			1.75	–	–	1.75	–	
		3.0			2.10	–	–	2.10	–	
		3.6			2.52	–	–	2.52	–	
V _{IL-OE}	Low-level input voltage (OE)	1.65	1.65 to 5.5		–	–	0.50	–	0.50	V
		1.8			–	–	0.54	–	0.54	
		2.5			–	–	0.75	–	0.75	
		3.0			–	–	0.90	–	0.90	
		3.6			–	–	1.08	–	1.08	
V _{OHL}	High-level output voltage (I/O _{VL})	1.65 to 3.6	1.65 to 5.5	IO = -60 μA	V _L - 0.4	–	–	V _L - 0.4	–	V
V _{OLL}	Low-level output voltage (I/O _{VL})	1.65 to 3.6	1.65 to 5.5	IO = +60 μA	–	–	0.4	–	0.4	V
V _{OHC}	High-level output voltage (I/O _{VCC})	1.65 to 3.6	1.65 to 5.5	IO = -60 μA	V _{CC} - 0.4	–	–	V _{CC} - 0.4	–	V
V _{OLC}	Low-level output voltage (I/O _{VCC})	1.65 to 3.6	1.65 to 5.5	IO = +60 μA	–	–	0.4	–	0.4	V
I _{OE}	Control input leakage current (OE)	1.65 to 3.6	1.65 to 5.5	V _I = GND or V _L	–	–	0.1	–	1	μA
I _{IO_LKG}	High impedance leakage current (I/O _{VL} , I/O _{VCC})	1.65 to 3.6	1.65 to 5.5	OE = GND I/O _{VL} = high I/O _{VCC} = low	–	–	0.1	–	1	μA
				OE = GND I/O _{VL} = low I/O _{VCC} = high	–	–	0.1	–	1	μA

Table 6. DC characteristics (continued)

Symbol	Parameter	V_L	V_{CC}	Test conditions	Value					Unit
					$T_A = 25\text{ }^\circ\text{C}$			$-40\text{ to }85\text{ }^\circ\text{C}$		
					Min.	Typ.	Max.	Min.	Max.	
I_{OFF}	Partial power-down current	1.65 to 3.6	0	OE = V_L or GND $I/O_{VL} = \text{high}$ $I/O_{VCC} = \text{low}$	-	-	0.1	-	1	μA
				OE = V_L or GND $I/O_{VL} = \text{low}$ $I/O_{VCC} = \text{high}$	-	-	0.1	-	1	
I_{QVCC}	Quiescent supply current V_{CC}	1.65 to 3.6	1.65 to 5.5	OE = V_L	--	-	7	-	9	μA
I_{QVL}	Quiescent supply current V_L	1.65 to 3.6	1.65 to 5.5	OE = V_L	-	-	0.1	-	1	μA
		1.65 to 3.6	0		-	-	0.1	-	1	
I_{Z-VCC}	High impedance quiescent supply current V_{CC}	1.65 to 3.6	1.65 to 5.5	OE = GND $I/O = \text{Hi-Z}$	-	-	0.1	-	1	μA
I_{Z-VL}	High impedance quiescent supply current V_L	1.65 to 3.6	1.65 to 5.5	OE = GND $I/O = \text{Hi-Z}$	-	-	0.1	-	1	μA
		1.65 to 3.6	0		-	-	0.1	-	1	

AC characteristics

Load $C_L = 15\text{ pF}$; driver $t_r = t_f \leq 6\text{ ns}$ over temperature range $-40\text{ }^\circ\text{C}$ to $85\text{ }^\circ\text{C}$.

Table 7. AC characteristics - test conditions: $V_L = 1.65 - 1.95\text{ V}$

Symbol	Parameter	$V_{CC} = V_L - 1.95\text{ V}$		$V_{CC} = 2.3 - 2.7\text{ V}$		$V_{CC} = 3.0 - 3.6\text{ V}$		$V_{CC} = 4.5 - 5.5\text{ V}$		Unit	
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{RVCC}	Rise time I/O_{VCC}	-	5.0	-	3.2	-	2.4	-	1.4	ns	
t_{FVCC}	Fall time I/O_{VCC}	-	1.5	-	1.4	-	1.3	-	1.2	ns	
t_{RVL}	Rise time I/O_{VL}	-	2.8	-	2.7	-	2.6	-	2.6	ns	
t_{FVL}	Fall time I/O_{VL}	-	1.5	-	1.4	-	1.4	-	1.3	ns	
$t_{I/OVL-VCC}$	Propagation delay time I/O_{VL-LH} to I/O_{VCC-LH} I/O_{VL-HL} to I/O_{VCC-HL}	t_{PLH}	-	6.6	-	5.8	-	5.0	-	4.4	ns
		t_{PHL}	-	4.1	-	3.8	-	3.6	-	3.4	ns

Table 7. AC characteristics - test conditions: $V_L = 1.65 - 1.95 \text{ V}$ (continued)

$t_{I/OVCC-VL}$	Propagation delay time I/O _{VCC-LH} to I/O _{VL-LH}	t_{PLH}	–	4.9	–	4.4	–	4.1	–	4.4	ns
	I/O _{VCC-HL} to I/O _{VL-HL}	t_{PHL}	–	4.6	–	4.2	–	4.0	–	3.6	ns
$t_{PZL} \ t_{PZH}$	Output enable time		–	27	–	27	–	27	–	27	ns
$t_{PLZ} \ t_{PHZ}$	Output disable time		–	145	–	145	–	145	–	145	
D_R	Data rate ⁽¹⁾		41	–	66	–	84	–	86	–	Mbps

1. Data rate is guaranteed based on the condition that output I/O signal rise/fall time is less than 15% of period of input I/O signal; input I/O signal is at 50% duty cycle and output I/O signal duty cycle deviation is less than 50% ± 10%.

Table 8. AC characteristics - test conditions: $V_L = 2.3 - 2.7 \text{ V}$

Symbol	Parameter	$V_{CC} = V_L - 2.7 \text{ V}$		$V_{CC} = 3.0 - 3.6 \text{ V}$		$V_{CC} = 4.5 - 5.5 \text{ V}$		Unit	
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{RVCC}	Rise time I/O _{VCC}	–	3.3	–	2.2	–	1.6	ns	
t_{FVCC}	Fall time I/O _{VCC}	–	1.7	–	1.6	–	1.4	ns	
t_{RVL}	Rise time I/O _{VL}	–	2.2	–	2.0	–	1.9	ns	
t_{FVL}	Fall time I/O _{VL}	–	1.3	–	1.2	–	1.2	ns	
$t_{I/OVL-VCC}$	Propagation delay time I/O _{VL-LH} to I/O _{VCC-LH} I/O _{VL-HL} to I/O _{VCC-HL}	t_{PLH}	–	4.6	–	4.3	–	3.9	ns
		t_{PHL}	–	3.6	–	3.3	–	2.9	ns
$t_{I/OVCC-VL}$	Propagation delay time I/O _{VCC-LH} to I/O _{VL-LH} I/O _{VCC-HL} to I/O _{VL-HL}	t_{PLH}	–	3.9	–	3.5	–	3.5	ns
		t_{PHL}	–	3.6	–	3.0	–	2.5	ns
$t_{PZL} \ t_{PZH}$	Output enable time	–	20	–	20	–	20	ns	
$t_{PLZ} \ t_{PHZ}$	Output disable time	–	130	–	130	–	130		
D_R	Data rate ⁽¹⁾	84	–	85	–	88	–	Mbps	

1. Data rate is guaranteed based on the condition that output I/O signal rise/fall time is less than 15% of period of input I/O signal; input I/O signal is at 50% duty cycle and output I/O signal duty cycle deviation is less than 50% ± 10%.

Table 9. AC characteristics - test conditions: $V_L = 3.0 - 3.6 \text{ V}$

Symbol	Parameter	$V_{CC} = V_L - 3.6 \text{ V}$		$V_{CC} = 4.5 - 5.5 \text{ V}$		Unit	
		Min.	Max.	Min.	Max.		
t_{RVCC}	Rise time I/O _{VCC}	–	1.8	–	1.7	ns	
t_{FVCC}	Fall time I/O _{VCC}	–	1.3	–	1.2	ns	
t_{RVL}	Rise time I/O _{VL}	–	1.6	–	1.5	ns	
t_{FVL}	Fall time I/O _{VL}	–	1.1	–	1.1	ns	
$t_{I/OVL-VCC}$	Propagation delay time I/O _{VL-LH} to I/O _{VCC-LH} I/O _{VL-HL} to I/O _{VCC-HL}	t_{PLH}	–	4.1	–	4.1	ns
		t_{PHL}	–	2.6	–	2.3	ns

Table 9. AC characteristics - test conditions: $V_L = 3.0 - 3.6$ V (continued)

$t_{I/OVCC-VL}$	Propagation delay time I/O _{VCC-LH} to I/O _{VL-LH}	t_{PLH}	–	4.0	–	4.0	ns
	I/O _{VCC-HL} to I/O _{VL-HL}	t_{PHL}	–	2.6	–	2.4	ns
t_{PZL} t_{PZH}	Output enable time		–	15	–	15	ns
t_{PLZ} t_{PHZ}	Output disable time		–	110	–	110	
D_R	Data rate ⁽¹⁾		86	–	89	–	Mbps

1. Data rate is guaranteed based on the condition that output I/O signal rise/fall time is less than 15% of period of input I/O signal; input I/O signal is at 50% duty cycle and output I/O signal duty cycle deviation is less than $50\% \pm 10\%$.

6 Test circuit

Figure 5. Test circuit

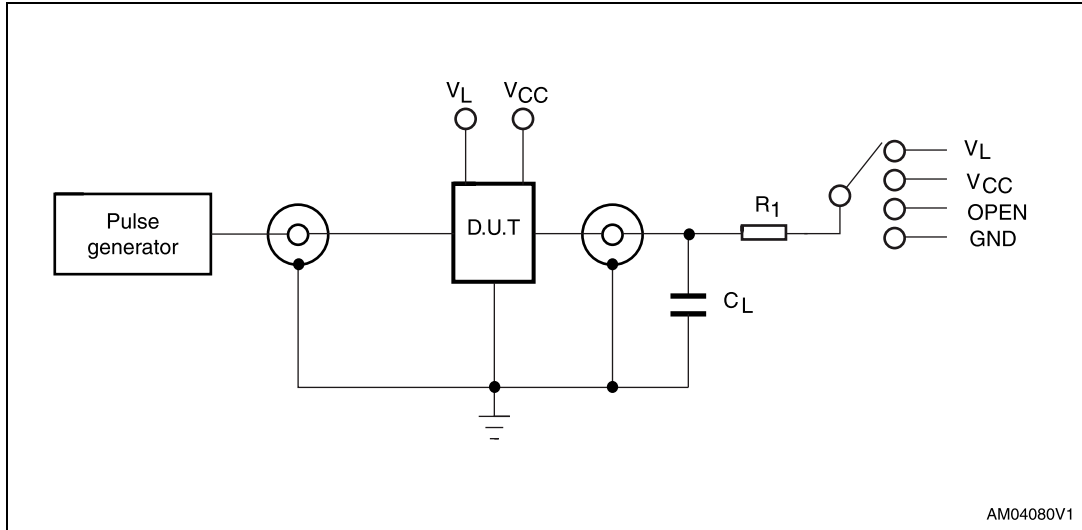


Table 10. Test circuit switches

Test	C_L	R_1	Switch
t_{PLH}, t_{PHL}	15 pF	20 k Ω	Open
t_r, t_f	15 pF	20 k Ω	Open
t_{PZL}, t_{PLZ}	15 pF	20 k Ω	V_L or V_{CC}
t_{PZH}, t_{PHZ}	15 pF	20 k Ω	GND

Table 11. Waveform symbol value

Symbol	Driving I/O V_L		Driving I/O V_{CC}	
	$1.65\text{ V} \leq V_L \leq V_{CC} \leq 2.5\text{ V}$	$3.3\text{ V} \leq V_L \leq V_{CC} \leq 5.5\text{ V}$	$1.65\text{ V} \leq V_L \leq V_{CC} \leq 2.5\text{ V}$	$3.3\text{ V} \leq V_L \leq V_{CC} \leq 5.5\text{ V}$
V_{IH}	V_L	V_L	V_{CC}	V_{CC}
V_{IM}	50% V_L	50% V_L	50% V_{CC}	50% V_{CC}
V_{OM}	50% V_{CC}	50% V_{CC}	50% V_L	50% V_L
V_X	$V_{OL} + 0.15\text{ V}$	$V_{OL} + 0.3\text{ V}$	$V_{OL} + 0.15\text{ V}$	$V_{OL} + 0.3\text{ V}$
V_Y	$V_{OH} - 0.15\text{ V}$	$V_{OH} - 0.3\text{ V}$	$V_{OH} - 0.15\text{ V}$	$V_{OH} - 0.3\text{ V}$

Figure 6. Waveform - propagation delay (f = 1 MHz, 50% duty cycle)

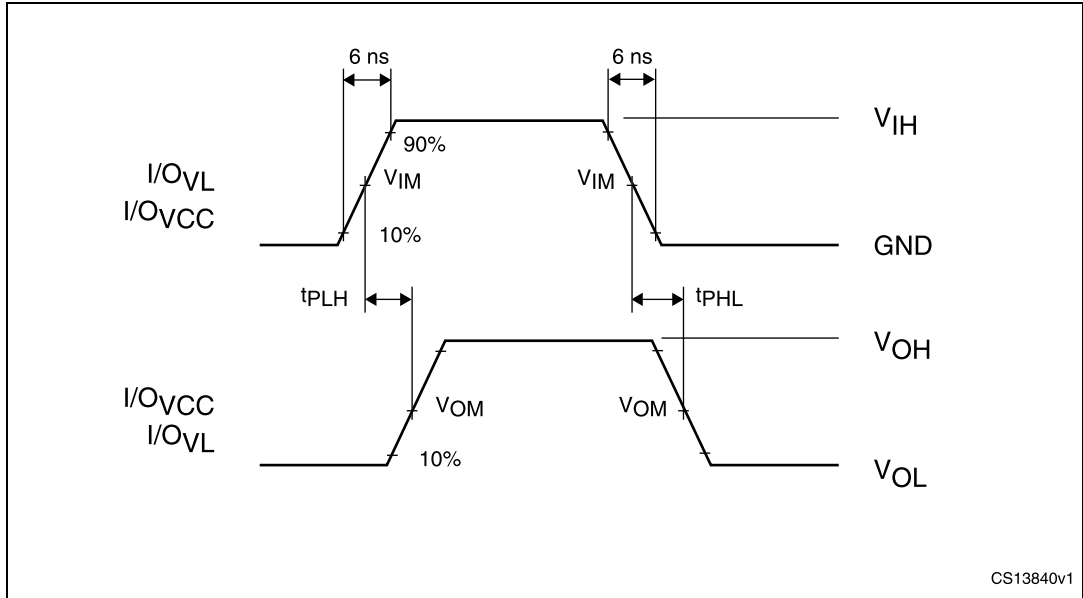
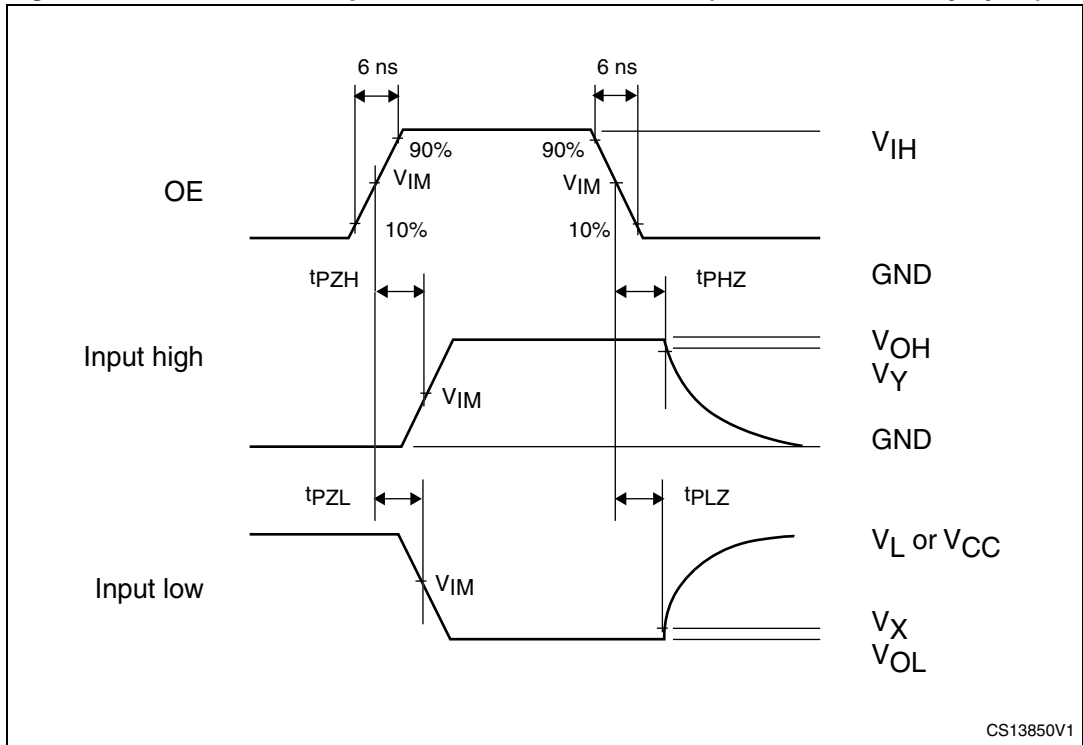


Figure 7. Waveform - output enable and disable time (f = 1 MHz, 50% duty cycle)



7 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Figure 8. Package outline for QFN16 (2.6 x 1.8 x 0.55 mm) - 0.40 mm pitch

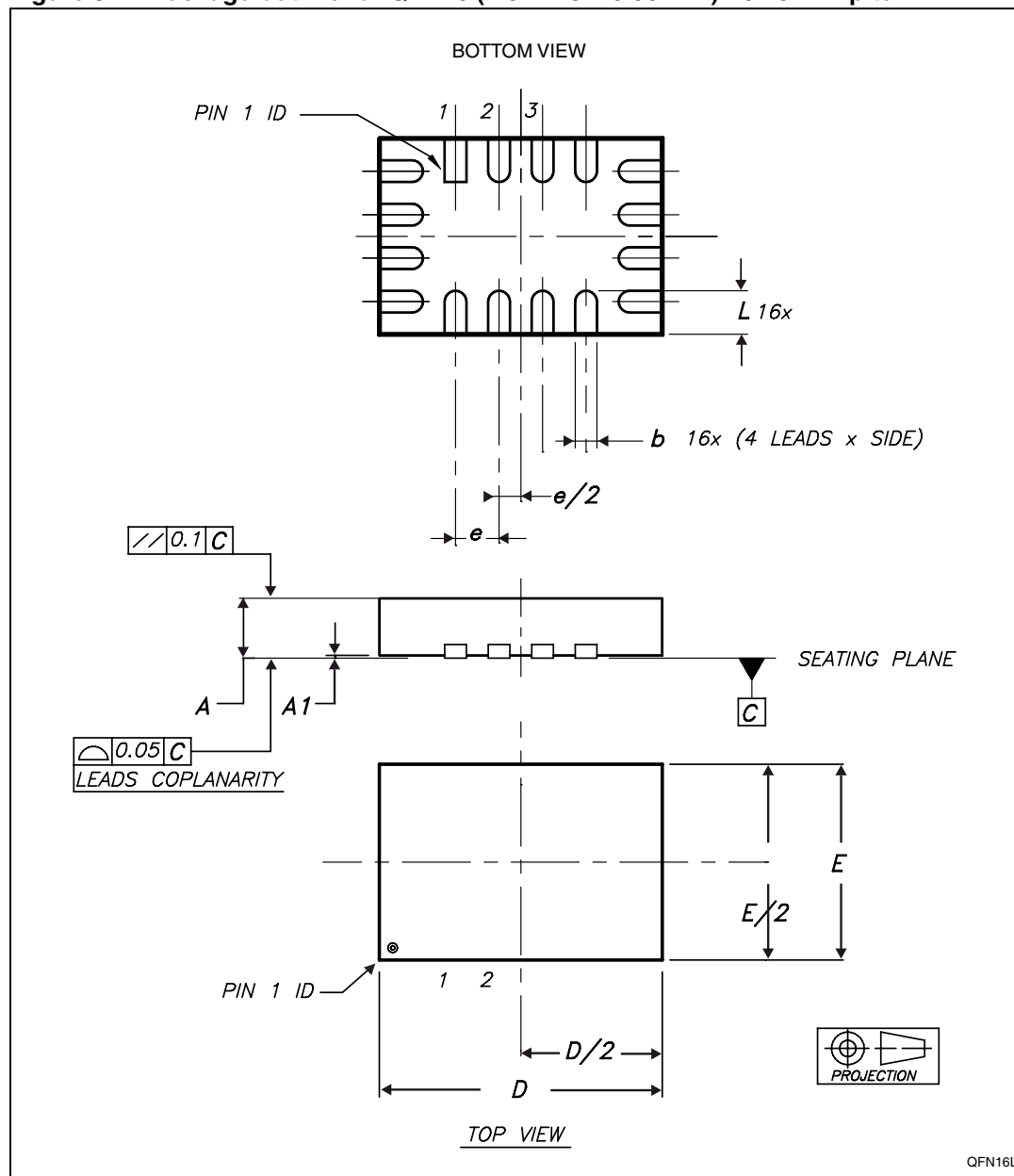
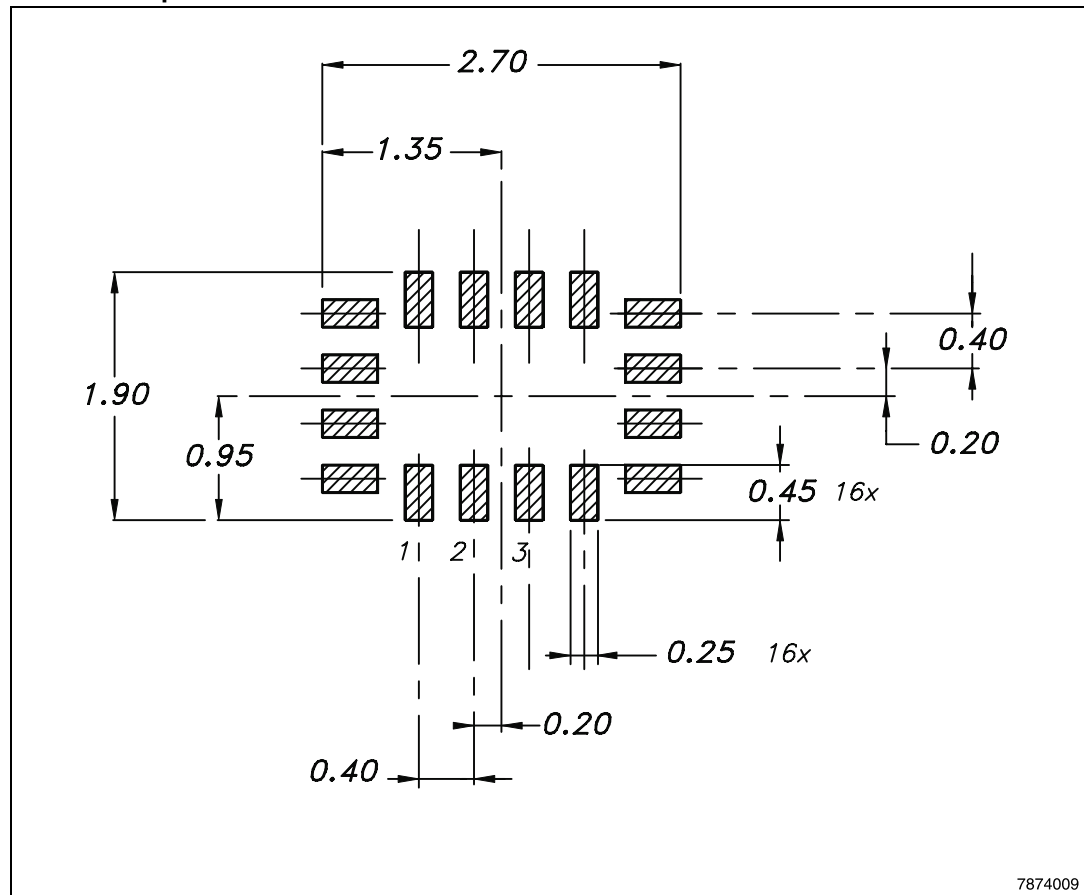


Table 12. Mechanical data for QFN16 (2.6 x 1.8 x 0.55 mm) - 0.40 mm pitch

Symbol	Dimensions		
	Millimeters		
	Typ.	Min.	Max.
A	0.55	0.45	0.60
A1	0.02	0	0.05
b	0.20	0.15	0.25
D	2.60	2.50	2.70
E	1.80	1.70	1.90
e	0.40	–	–
L	0.40	0.35	0.45

Figure 9. Footprint recommendation for QFN16 (2.6 x 1.8 x 0.55 mm) - 0.40 mm pitch



7874009

Figure 10. Carrier tape for QFN16 (2.6 x 1.8 x 0.55 mm) - 0.40 mm pitch

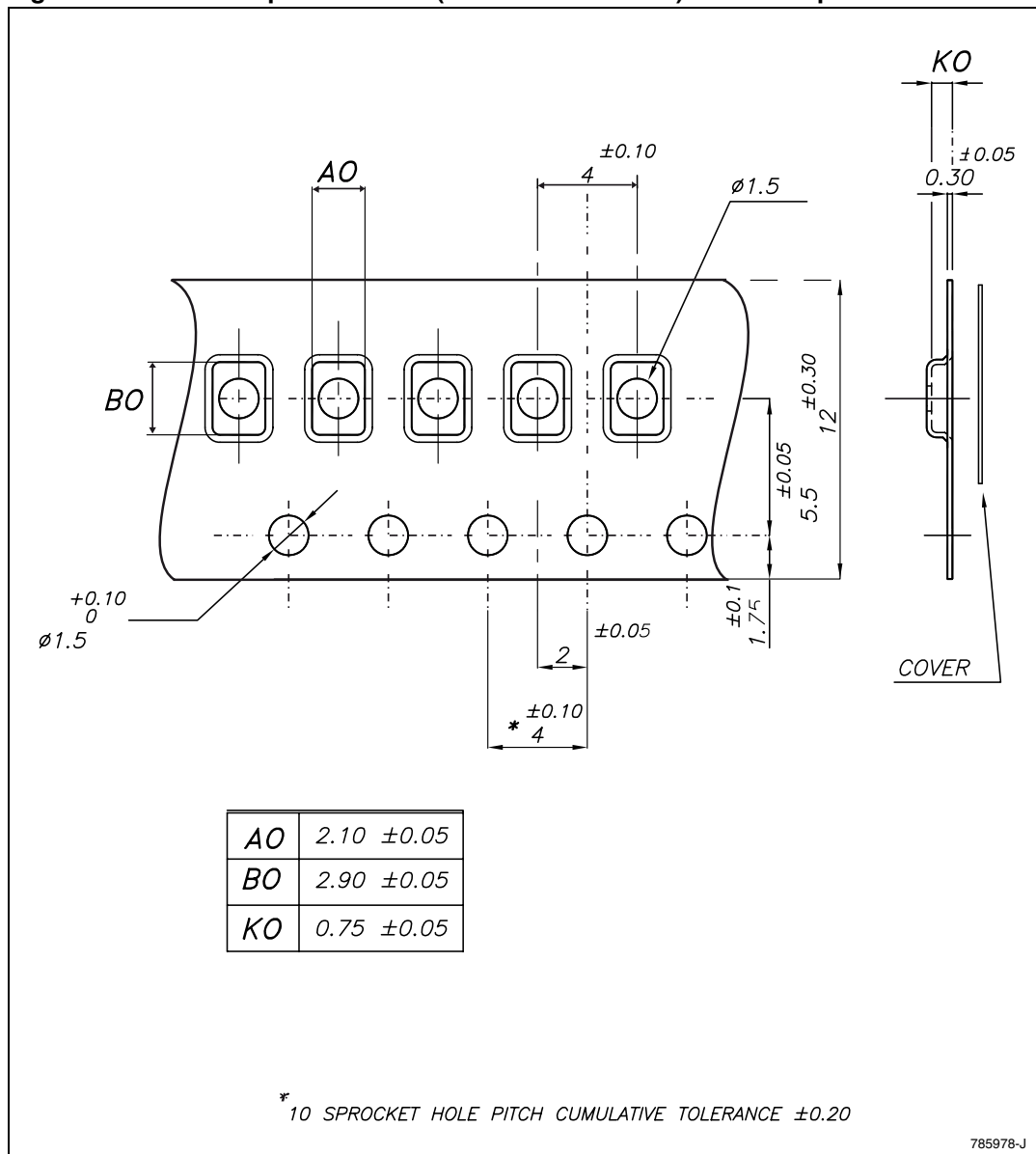
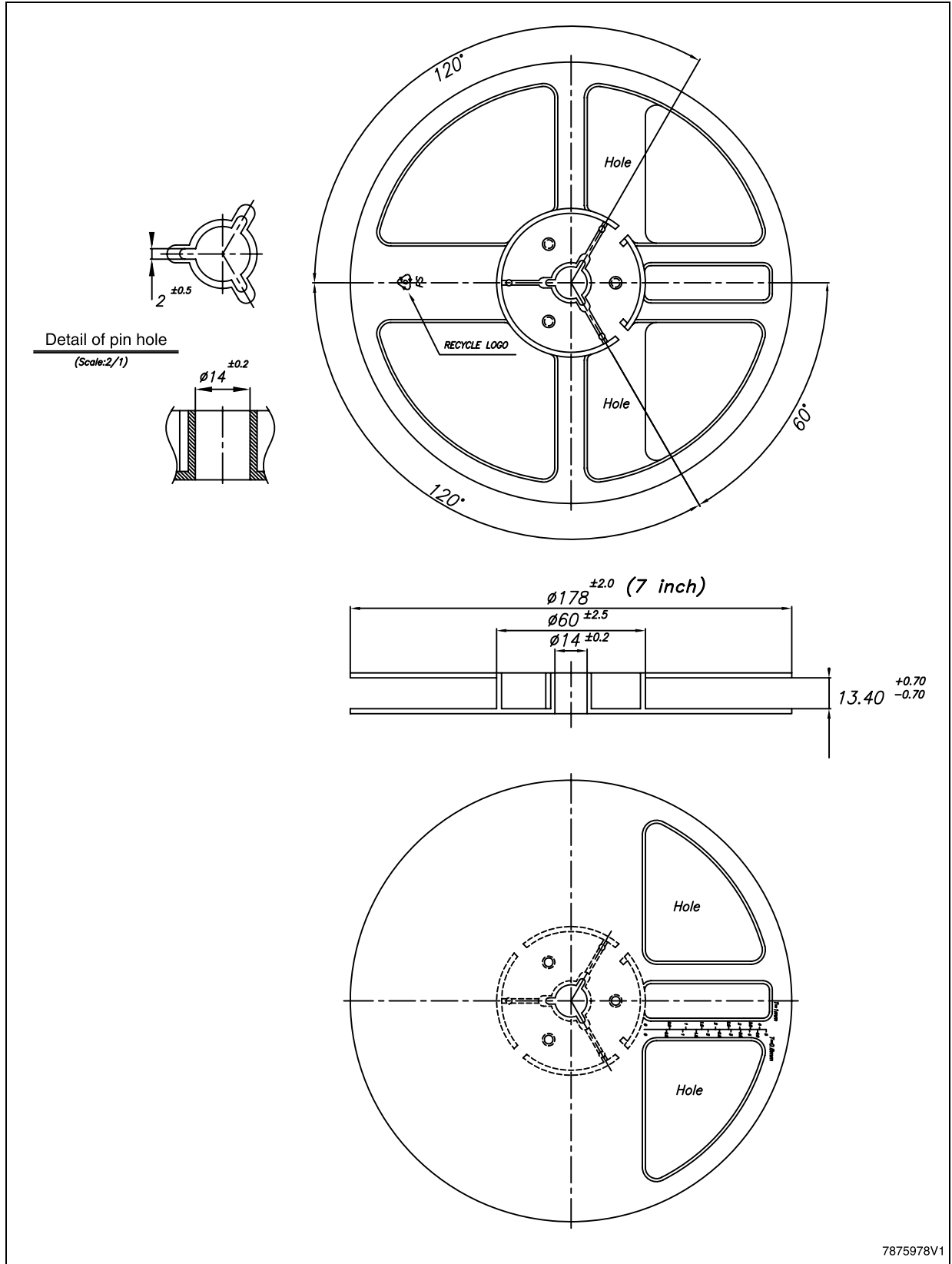


Figure 11. Reel information for QFN16 (2.6 x 1.8 x 0.55 mm) - 0.40 mm pitch



8 Revision history

Table 13. Document revision history

Date	Revision	Changes
07-Sep-2009	1	Initial release.
14-Jun-2012	2	Updated Features , Figure 1 , Figure 3 , Section 3.2 , Section 3.3 , Table 4 , Table 5 , Table 6 , Section : AC characteristics , Table 7 , Table 8 , Table 9 , minor text corrections throughout document.

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