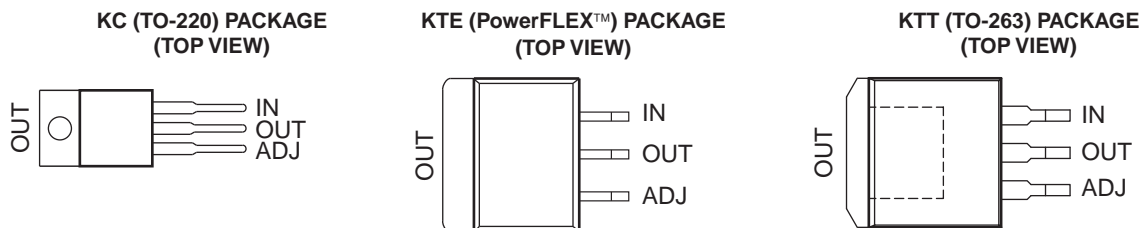


HIGH-VOLTAGE ADJUSTABLE REGULATOR

FEATURES

- Output Adjustable From 1.25 V to 125 V When Used With an External Resistor Divider
- 700-mA Output Current
- Full Short-Circuit, Safe-Operating-Area, and Thermal-Shutdown Protection
- 0.001%/V Typical Input Voltage Regulation
- 0.15% Typical Output Voltage Regulation
- 76-dB Typical Ripple Rejection



DESCRIPTION/ORDERING INFORMATION

The TL783 is an adjustable three-terminal high-voltage regulator with an output range of 1.25 V to 125 V and a DMOS output transistor capable of sourcing more than 700 mA. It is designed for use in high-voltage applications where standard bipolar regulators cannot be used. Excellent performance specifications, superior to those of most bipolar regulators, are achieved through circuit design and advanced layout techniques.

As a state-of-the-art regulator, the TL783 combines standard bipolar circuitry with high-voltage double-diffused MOS transistors on one chip, to yield a device capable of withstanding voltages far higher than standard bipolar integrated circuits. Because of its lack of secondary-breakdown and thermal-runaway characteristics usually associated with bipolar outputs, the TL783 maintains full overload protection while operating at up to 125 V from input to output. Other features of the device include current limiting, safe-operating-area (SOA) protection, and thermal shutdown. Even if ADJ is disconnected inadvertently, the protection circuitry remains functional.

Only two external resistors are required to program the output voltage. An input bypass capacitor is necessary only when the regulator is situated far from the input filter. An output capacitor, although not required, improves transient response and protection from instantaneous output short circuits. Excellent ripple rejection can be achieved without a bypass capacitor at the adjustment terminal.

ORDERING INFORMATION⁽¹⁾

| T _J | PACKAGE ⁽²⁾ | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|----------------|------------------------|--------------|-----------------------|------------------|
| 0°C to 125°C | PowerFLEX™ – KTE | Reel of 2000 | TL783CKTER | TL783 |
| | TO-263 – KTT | Reel of 500 | TL783CKTTR | TL783C |
| | TO-220 – KC | Tube of 50 | TL783CKC | TL783C |

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

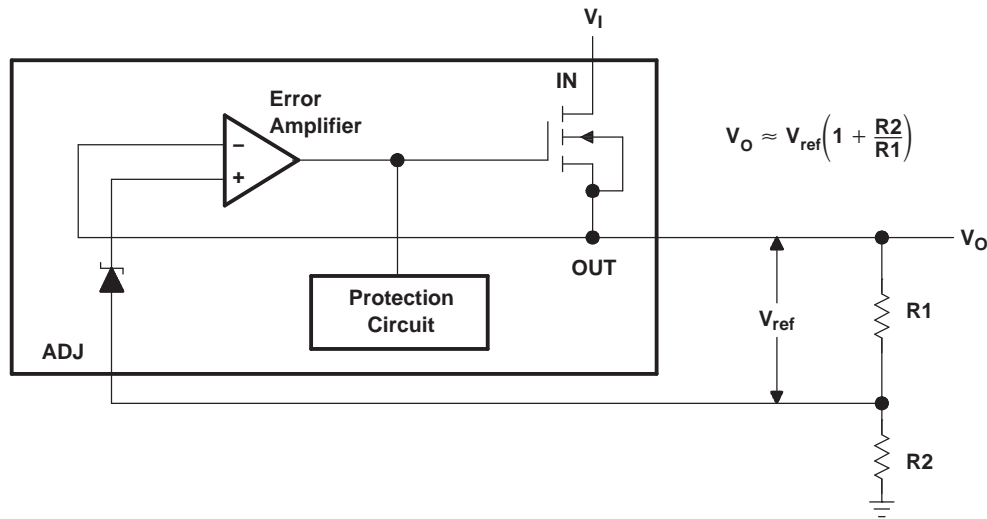
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PowerFLEX, PowerPAD are trademarks of Texas Instruments.

FUNCTIONAL BLOCK DIAGRAM



Absolute Maximum Ratings⁽¹⁾

over operating temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|-------------|--|-----|-----|------|
| $V_I - V_O$ | Input-to-output differential voltage | | 125 | V |
| T_J | Operating virtual junction temperature | | 150 | °C |
| T_{stg} | Storage temperature range | -65 | 150 | °C |

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Package Thermal Data⁽¹⁾

| PACKAGE | BOARD | θ_{JC} | $\theta_{JP}^{(2)}$ | θ_{JA} |
|-----------------|-------------------|---------------|---------------------|---------------|
| PowerFLEX (KTE) | High K, JESD 51-5 | | 2.7°C/W | 23°C/W |
| TO-263 (KTT) | High K, JESD 51-5 | 18°C/W | 1.94°C/W | 25.3°C/W |
| TO-220 (KC) | High K, JESD 51-5 | 17°C/W | 3°C/W | 19°C/W |

- (1) Maximum power dissipation is a function of $T_{J(max)}$, θ_{JA} , and T_A . The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_{J(max)} - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability. Due to variations in individual device electrical characteristics and thermal resistance, the built-in thermal overload protection may be activated at power levels slightly above or below the rated dissipation.
- (2) For packages with exposed thermal pads, such as QFN, PowerPAD™, or PowerFLEX, θ_{JP} is defined as the thermal resistance between the die junction and the bottom of the exposed pad.

Recommended Operating Conditions

| | | MIN | MAX | UNIT |
|-------------|--|-----|-----|------|
| $V_I - V_O$ | Input-to-output differential voltage | | 125 | V |
| I_O | Output current | 15 | 700 | mA |
| T_J | Operating virtual junction temperature | 0 | 125 | °C |

Electrical Characteristics

 $V_I - V_O = 25\text{ V}$, $I_O = 0.5\text{ A}$, $T_J = 0^\circ\text{C}$ to 125°C (unless otherwise noted)

| PARAMETER | TEST CONDITIONS ⁽¹⁾ | MIN | TYP | MAX | UNIT |
|---|---|--|-------|------|---------------|
| Input voltage regulation ⁽²⁾ | $V_I - V_O = 20\text{ V}$ to 125 V , $P \leq$ rated dissipation | $T_J = 25^\circ\text{C}$ | 0.001 | 0.01 | %V |
| | | $T_J = 0^\circ\text{C}$ to 125°C | 0.004 | 0.02 | |
| Ripple rejection | $\Delta V_{I(PP)} = 10\text{ V}$, $V_O = 10\text{ V}$, $f = 120\text{ Hz}$ | 66 | 76 | | dB |
| Output voltage regulation | $I_O = 15\text{ mA}$ to 700 mA , $T_J = 25^\circ\text{C}$ | $V_O \leq 5\text{ V}$ | 7.5 | 25 | mV |
| | | $V_O \geq 5\text{ V}$ | 0.15 | 0.5 | % |
| | $I_O = 15\text{ mA}$ to 700 mA , $P \leq$ rated dissipation | $V_O \leq 5\text{ V}$ | 20 | 70 | mV |
| | | $V_O \geq 5\text{ V}$ | 0.3 | 1.5 | % |
| Output voltage change with temperature | | | 0.4 | | % |
| Output voltage long-term drift | 1000 hours at $T_J = 125^\circ\text{C}$, $V_I - V_O = 125\text{ V}$ | | 0.2 | | % |
| Output noise voltage | $f = 10\text{ Hz}$ to 10 kHz , $T_J = 25^\circ\text{C}$ | | 0.003 | | % |
| Minimum output current to maintain regulation | $V_I - V_O = 125\text{ V}$ | | | 15 | mA |
| Peak output current | $V_I - V_O = 25\text{ V}$, $t = 1\text{ ms}$ | | 1100 | | mA |
| | $V_I - V_O = 15\text{ V}$, $t = 30\text{ ms}$ | | 715 | | |
| | $V_I - V_O = 25\text{ V}$, $t = 30\text{ ms}$ | 700 | 900 | | |
| | $V_I - V_O = 125\text{ V}$, $t = 30\text{ ms}$ | 100 | 250 | | |
| ADJ input current | | | 83 | 110 | μA |
| Change in ADJ input current | $V_I - V_O = 15\text{ V}$ to 125 V , $I_O = 15\text{ mA}$ to 700 mA , $P \leq$ rated dissipation | | 0.5 | 5 | μA |
| Reference voltage (OUT to ADJ) ⁽³⁾ | $V_I - V_O = 10\text{ V}$ to 125 V , $I_O = 15\text{ mA}$ to 700 mA , $P \leq$ rated dissipation | 1.2 | 1.27 | 1.3 | V |

- (1) Pulse-testing techniques maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately.
- (2) Input voltage regulation is expressed here as the percentage change in output voltage per 1-V change at the input
- (3) Due to the dropout voltage and output current-limiting characteristics of this device, output current is limited to less than 700 mA at input-to-output voltage differentials of less than 25 V.

TYPICAL CHARACTERISTICS

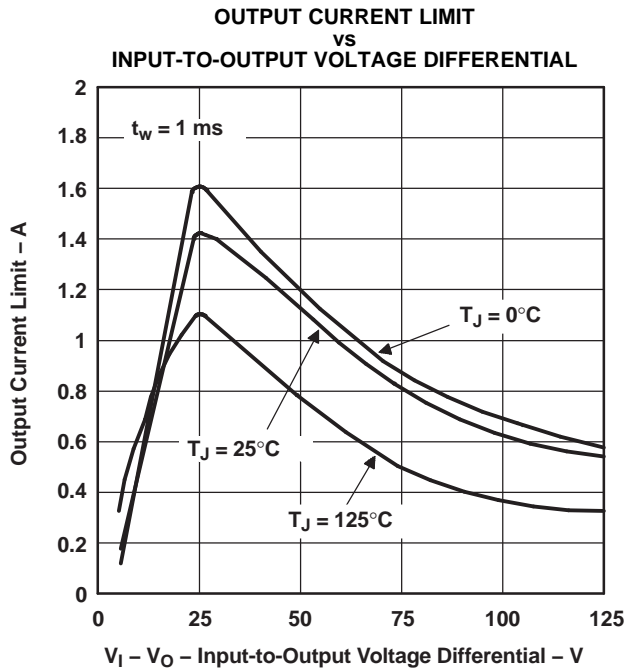


Figure 1.

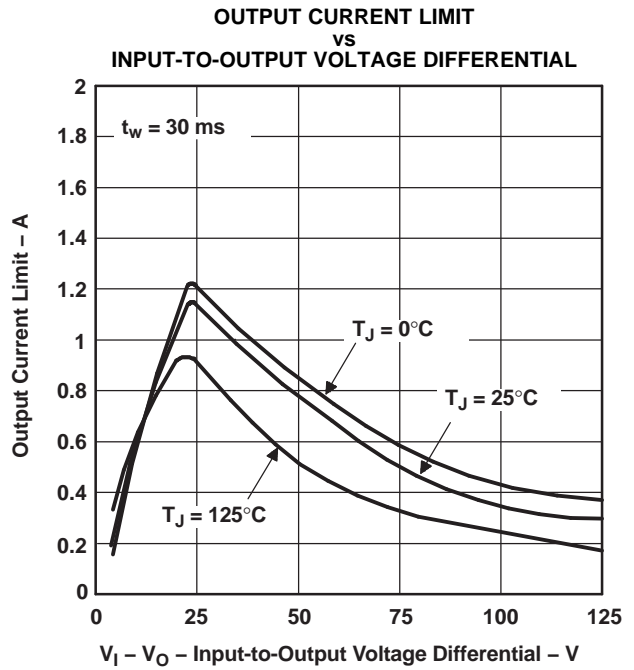


Figure 2.

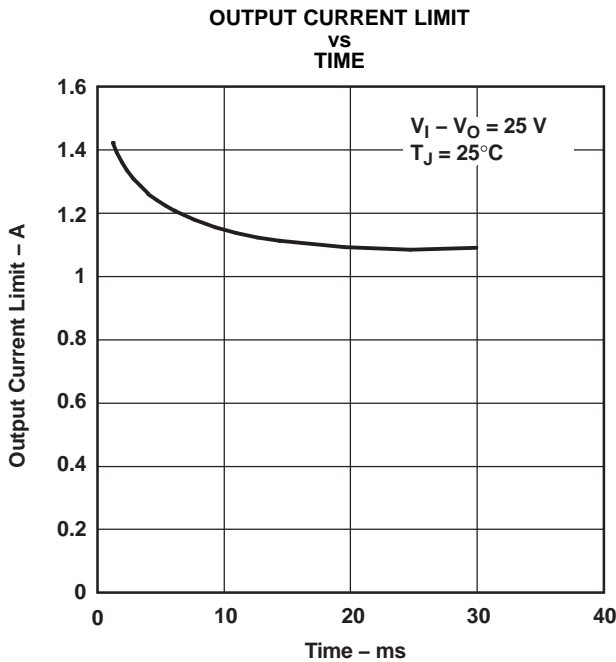


Figure 3.

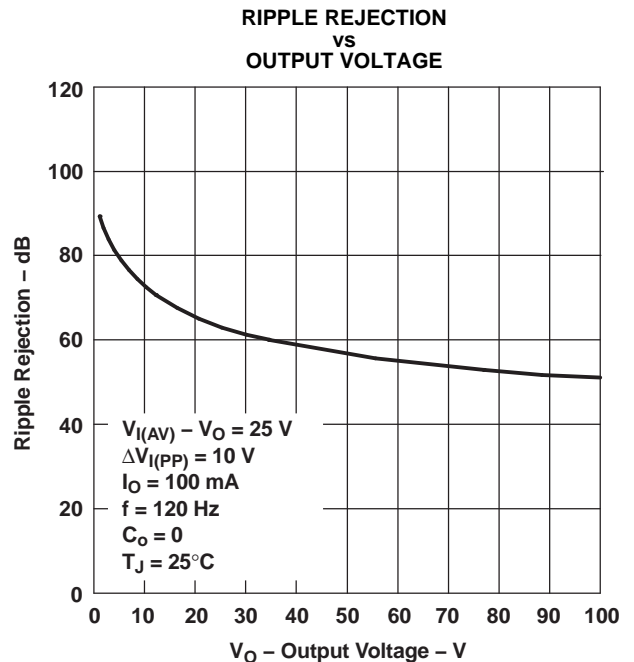


Figure 4.

TYPICAL CHARACTERISTICS (continued)

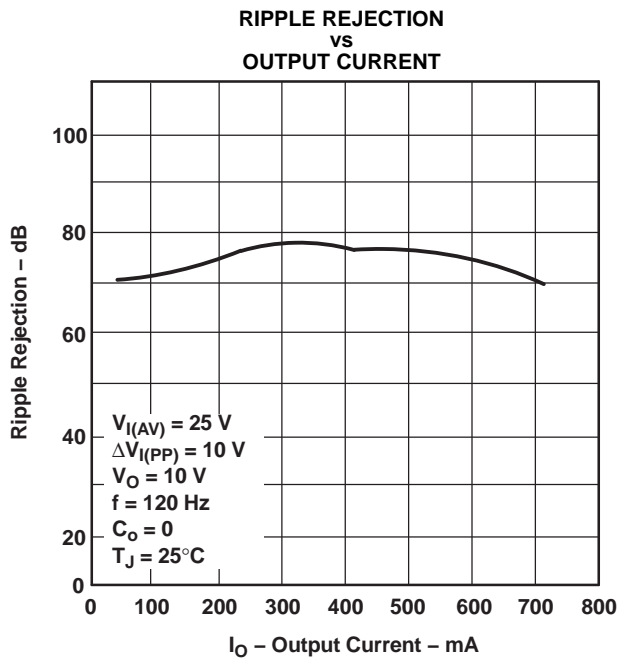


Figure 5.

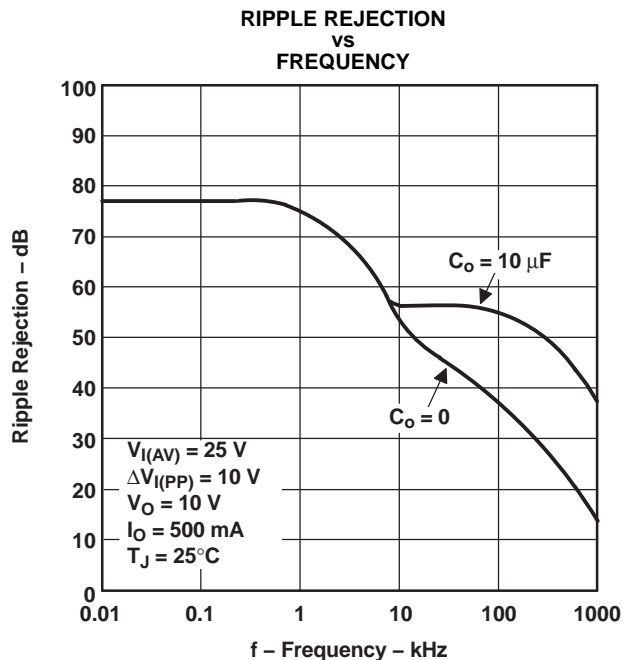


Figure 6.

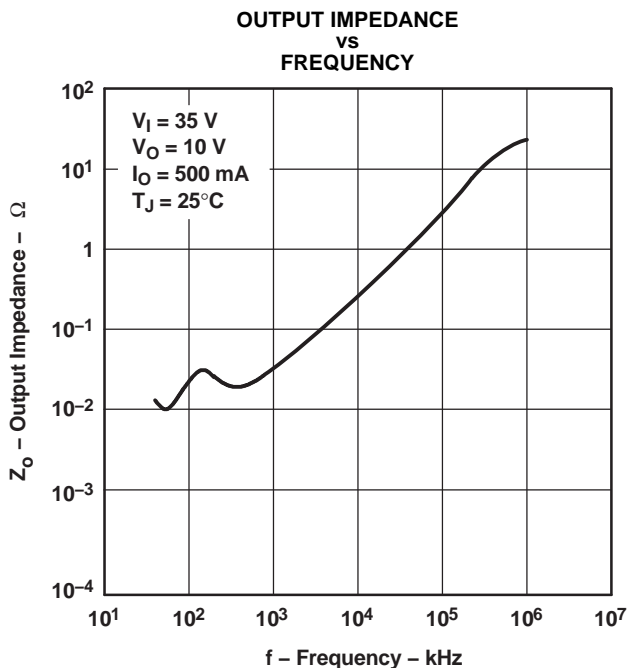


Figure 7.

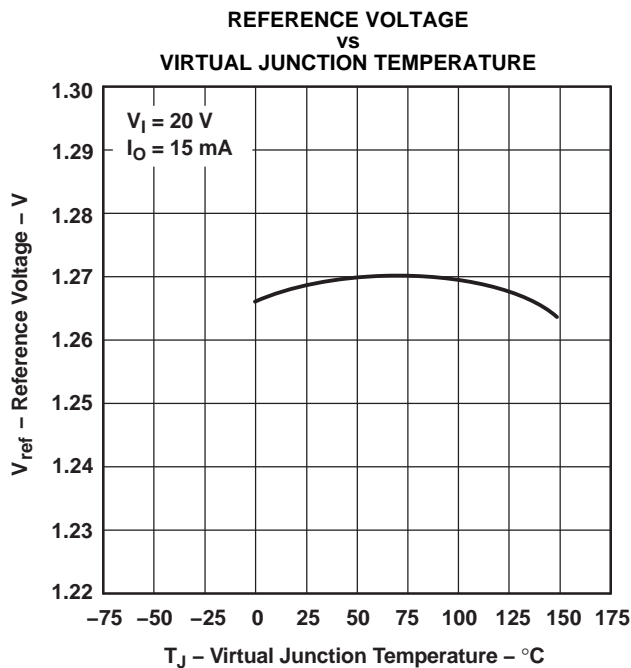
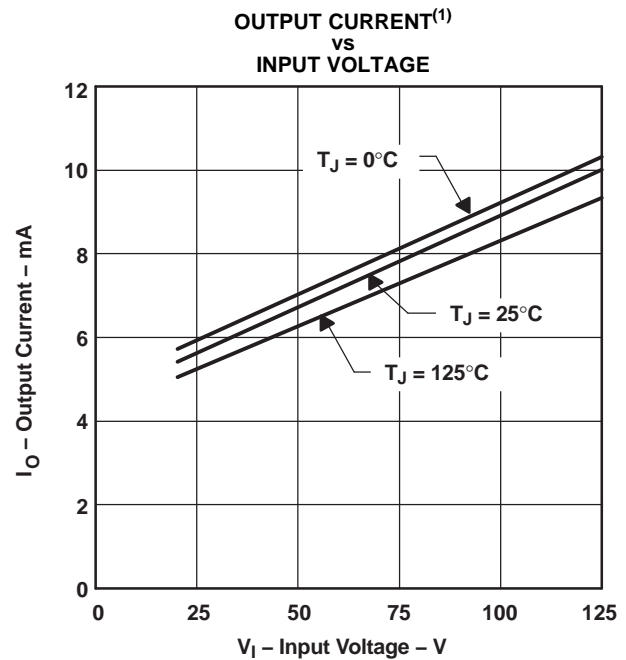
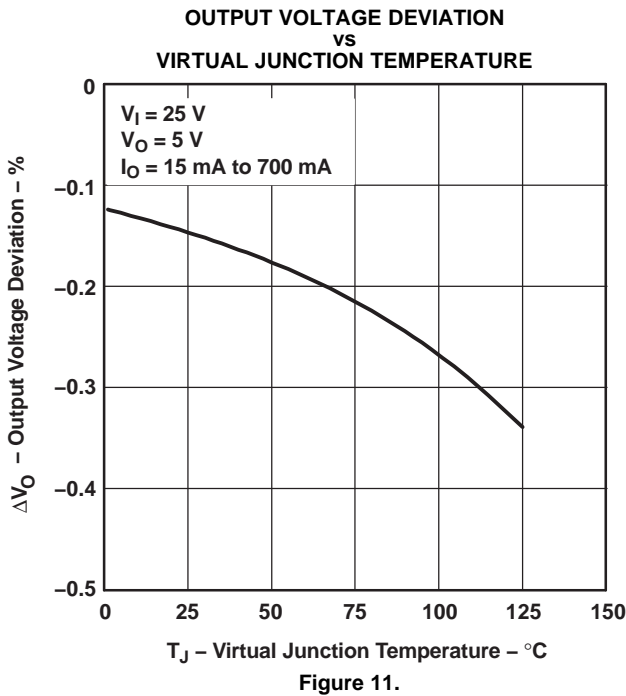
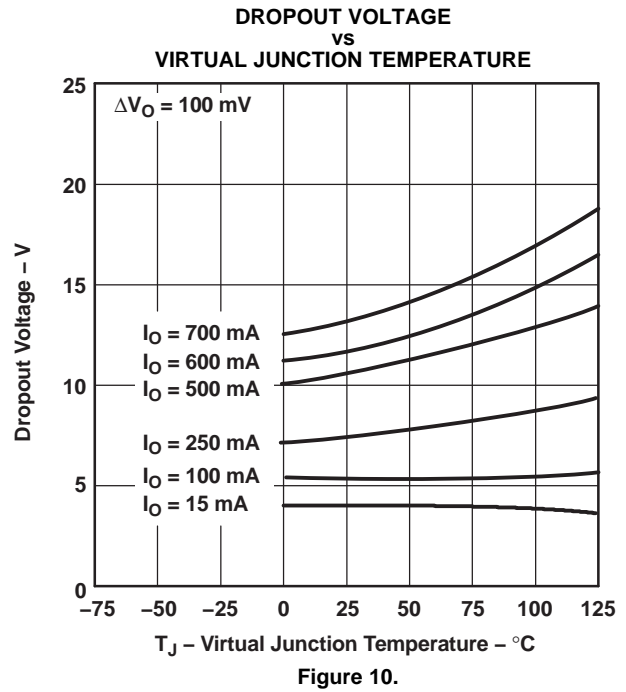
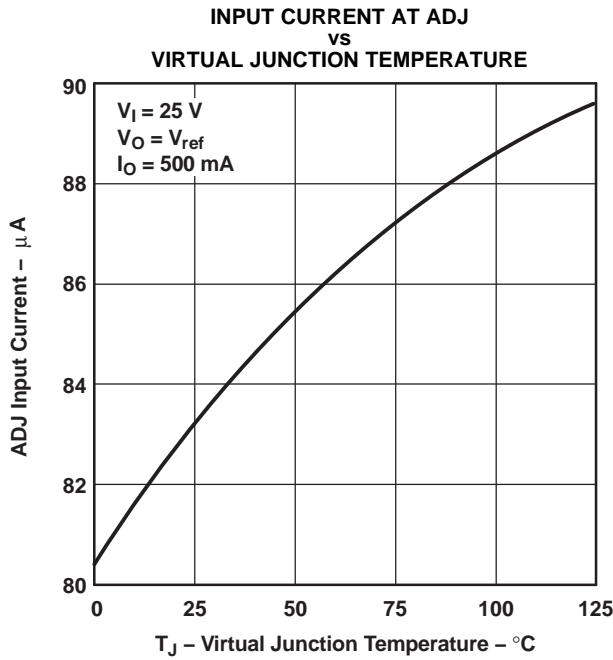


Figure 8.

TYPICAL CHARACTERISTICS (continued)



(1) This is the minimum current required to maintain voltage regulation.

TYPICAL CHARACTERISTICS (continued)

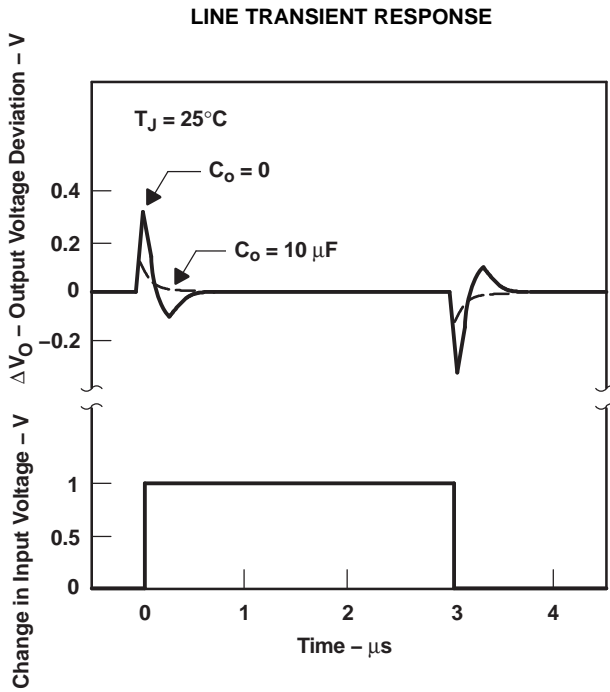


Figure 13.

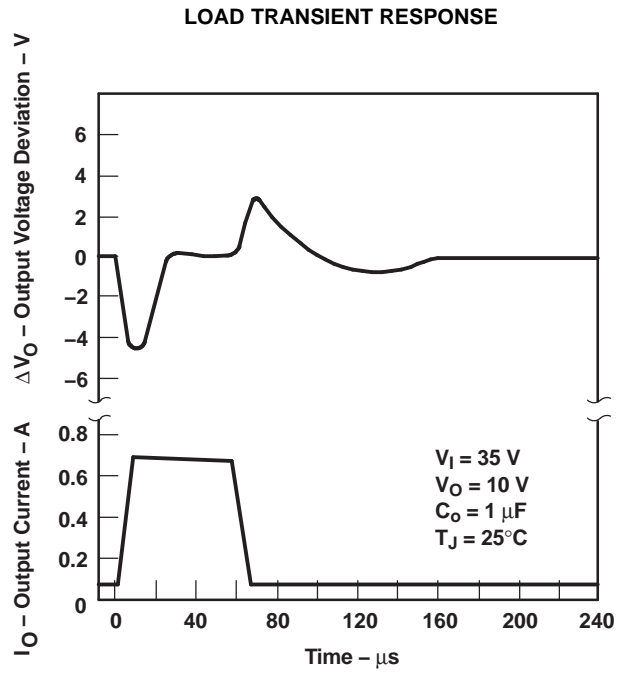


Figure 14.

DESIGN CONSIDERATIONS

The internal reference (see [functional block diagram](#)) generates 1.25 V nominal (V_{ref}) between OUT and ADJ. This voltage is developed across R1 and causes a constant current to flow through R1 and the programming resistor R2, giving an output voltage of:

$$V_O = V_{ref} (1 + R2/R1) + I_{I(ADJ)} (R2)$$

or

$$V_O \approx V_{ref} (1 + R2/R1)$$

The TL783 was designed to minimize the input current at ADJ and maintain consistency over line and load variations, thereby minimizing the associated ($R2$) error term.

To maintain $I_{I(ADJ)}$ at a low level, all quiescent operating current is returned to the output terminal. This quiescent current must be sunk by the external load and is the minimum load current necessary to prevent the output from rising. The recommended R1 value of 82 Ω provides a minimum load current of 15 mA. Larger values can be used when the input-to-output differential voltage is less than 125 V (see the output-current curve in [Figure 12](#)) or when the load sinks some portion of the minimum current.

Bypass Capacitors

The TL783 regulator is stable without bypass capacitors; however, any regulator becomes unstable with certain values of output capacitance if an input capacitor is not used. Therefore, the use of input bypassing is recommended whenever the regulator is located more than four inches from the power-supply filter capacitor. A 1- μ F tantalum or aluminum electrolytic capacitor usually is sufficient.

Adjustment-terminal capacitors are not recommended for use on the TL783 because they can seriously degrade load transient response, as well as create a need for extra protection circuitry. Excellent ripple rejection presently is achieved without this added capacitor.

Due to the relatively low gain of the MOS output stage, output voltage dropout may occur under large-load transient conditions. The addition of an output bypass capacitor greatly enhances load transient response and prevents dropout. For most applications, it is recommended that an output bypass capacitor be used, with a minimum value of:

$$C_o (\mu F) = 15/V_O$$

Larger values provide proportionally better transient-response characteristics.

Protection Circuitry

The TL783 regulator includes built-in protection circuits capable of guarding the device against most overload conditions encountered in normal operation. These protective features are current limiting, safe-operating-area protection, and thermal shutdown. These circuits protect the device under occasional fault conditions only. Continuous operation in the current limit or thermal shutdown mode is not recommended.

The internal protection circuits of the TL783 protect the device up to maximum-rated V_I as long as certain precautions are taken. If V_I is switched on instantaneously, transients exceeding maximum input ratings may occur, which can destroy the regulator. Usually, these are caused by lead inductance and bypass capacitors causing a ringing voltage on the input. In addition, when rise times in excess of 10 V/ns are applied to the input, a parasitic npn transistor in parallel with the DMOS output can be turned on, causing the device to fail. If the device is operated over 50 V and the input is switched on, rather than ramped on, a low-Q capacitor, such as tantalum or aluminum electrolytic, should be used, rather than ceramic, paper, or plastic bypass capacitors. A Q factor of 0.015, or greater, usually provides adequate damping to suppress ringing. Normally, no problems occur if the input voltage is allowed to ramp upward through the action of an ac line rectifier and filter network.

Similarly, when an instantaneous short circuit is applied to the output, both ringing and excessive fall times can result. A tantalum or aluminum electrolytic bypass capacitor is recommended to eliminate this problem. However, if a large output capacitor is used, and the input is shorted, addition of a protection diode may be necessary to prevent capacitor discharge through the regulator. The amount of discharge current delivered is dependent on output voltage, size of capacitor, and fall time of V_I . A protective diode (see [Figure 15](#)) is required only for capacitance values greater than:

$$C_o (\mu F) = 3 \times 10^4 / (V_O)^2$$

Care always should be taken to prevent insertion of regulators into a socket with power on. Power should be turned off before removing or inserting regulators.

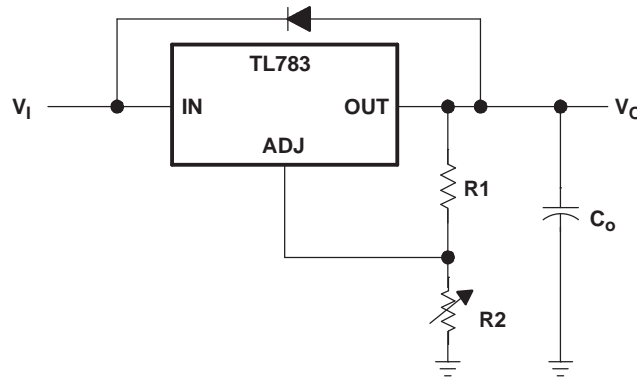


Figure 15. Regulator With Protective Diode

Load Regulation

The current-set resistor (R1) should be located close to the regulator output terminal, rather than near the load. This eliminates long line drops from being amplified, through the action of R1 and R2, to degrade load regulation. To provide remote ground sensing, R2 should be near the load ground.

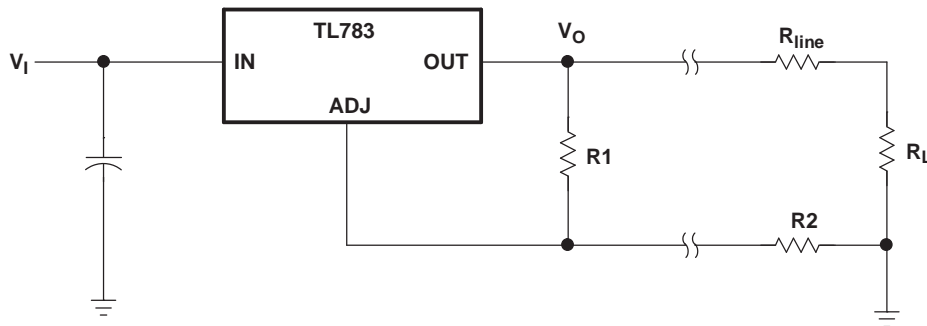
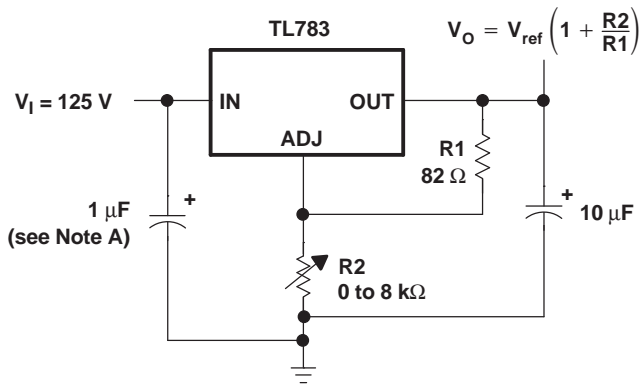


Figure 16. Regulator With Current-Set Resistor

APPLICATION INFORMATION



A. Needed if device is more than 4 inches from filter capacitor
Figure 17. 1.25-V to 115-V Adjustable Regulator

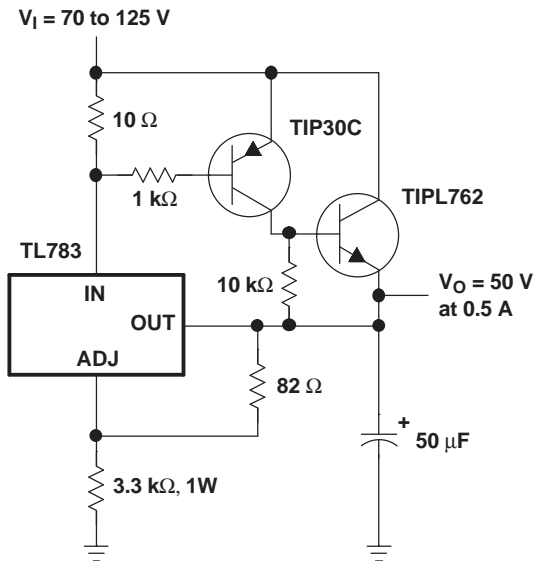


Figure 19. 50-V Regulator With Current Boost

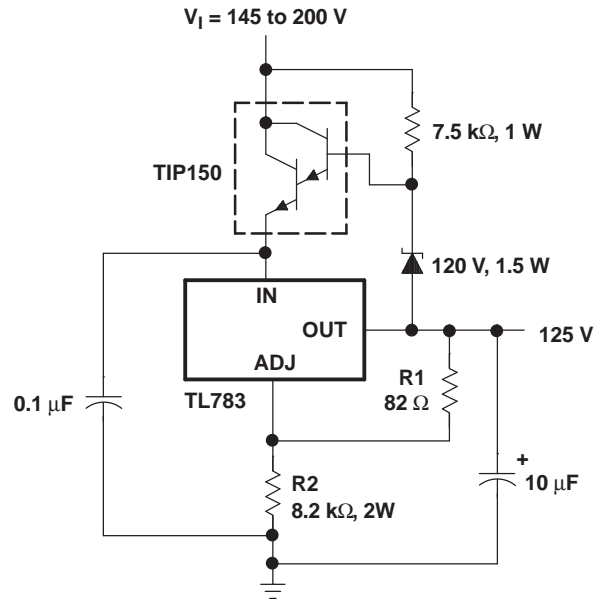


Figure 18. 125-V Short-Circuit-Protected Off-Line Regulator

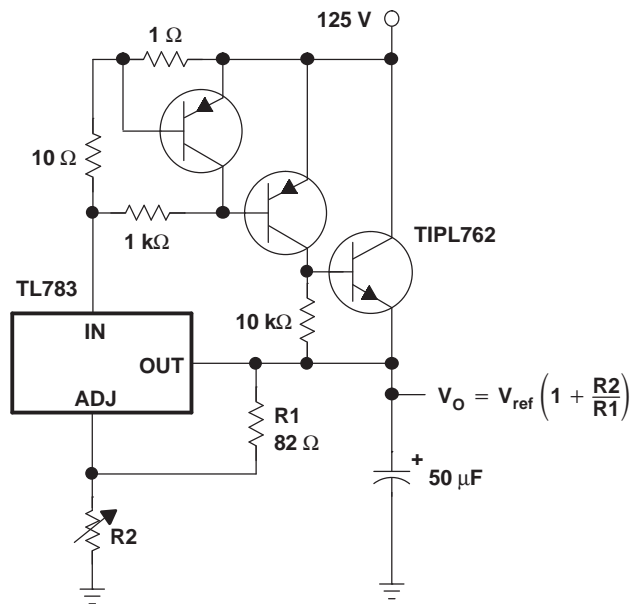


Figure 20. Adjustable Regulator With Current Boost and Current Limit

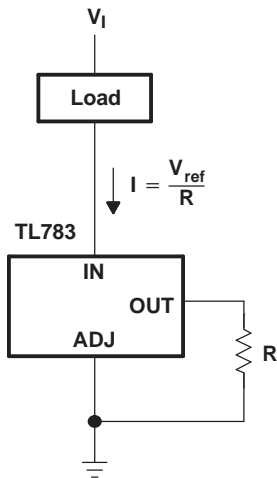


Figure 21. Current-Sinking Regulator

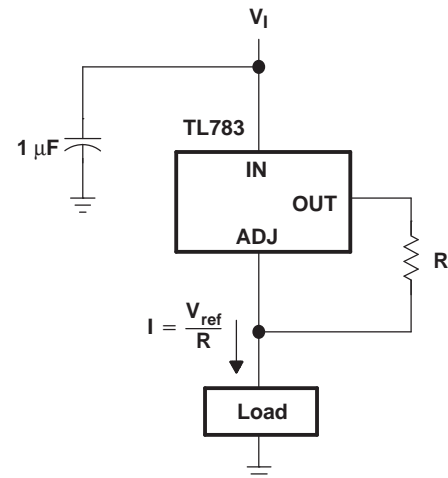


Figure 22. Current-Sourcing Regulator

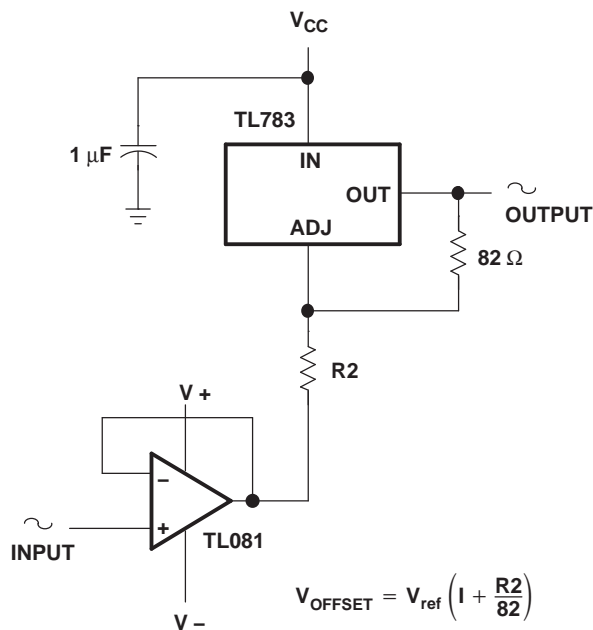


Figure 23. High-Voltage Unity-Gain Offset Amplifier

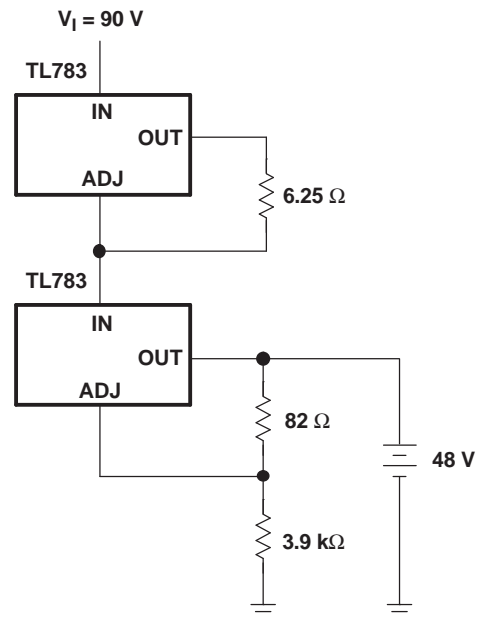


Figure 24. 48-V 200-mA Float Charger

PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/ Ball Finish | MSL Peak Temp ⁽³⁾ | Samples (Requires Login) |
|------------------|-----------------------|------------------|-----------------|------|-------------|----------------------------|----------------------|------------------------------|--------------------------------------|
| TL783CKC | OBSOLETE | TO-220 | KC | 3 | | TBD | Call TI | Call TI | Samples Not Available |
| TL783CKCE3 | OBSOLETE | TO-220 | KC | 3 | | TBD | Call TI | Call TI | Samples Not Available |
| TL783CKCSE3 | ACTIVE | TO-220 | KCS | 3 | 50 | Pb-Free (RoHS) | CU SN | N / A for Pkg Type | Request Free Samples |
| TL783CKTER | OBSOLETE | PFM | KTE | 3 | | TBD | Call TI | Call TI | Samples Not Available |
| TL783CKTTR | ACTIVE | DDPAK/ TO-263 | KTT | 3 | 500 | Green (RoHS & no Sb/Br) | CU SN | Level-3-245C-168 HR | Request Free Samples |
| TL783CKTTRG3 | ACTIVE | DDPAK/ TO-263 | KTT | 3 | 500 | Green (RoHS & no Sb/Br) | CU SN | Level-3-245C-168 HR | Request Free Samples |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------|--------------|-----------------|------|-----|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TL783CKTTR | DDPAK/TO-263 | KTT | 3 | 500 | 330.0 | 24.4 | 10.6 | 15.8 | 4.9 | 16.0 | 24.0 | Q2 |

TAPE AND REEL BOX DIMENSIONS

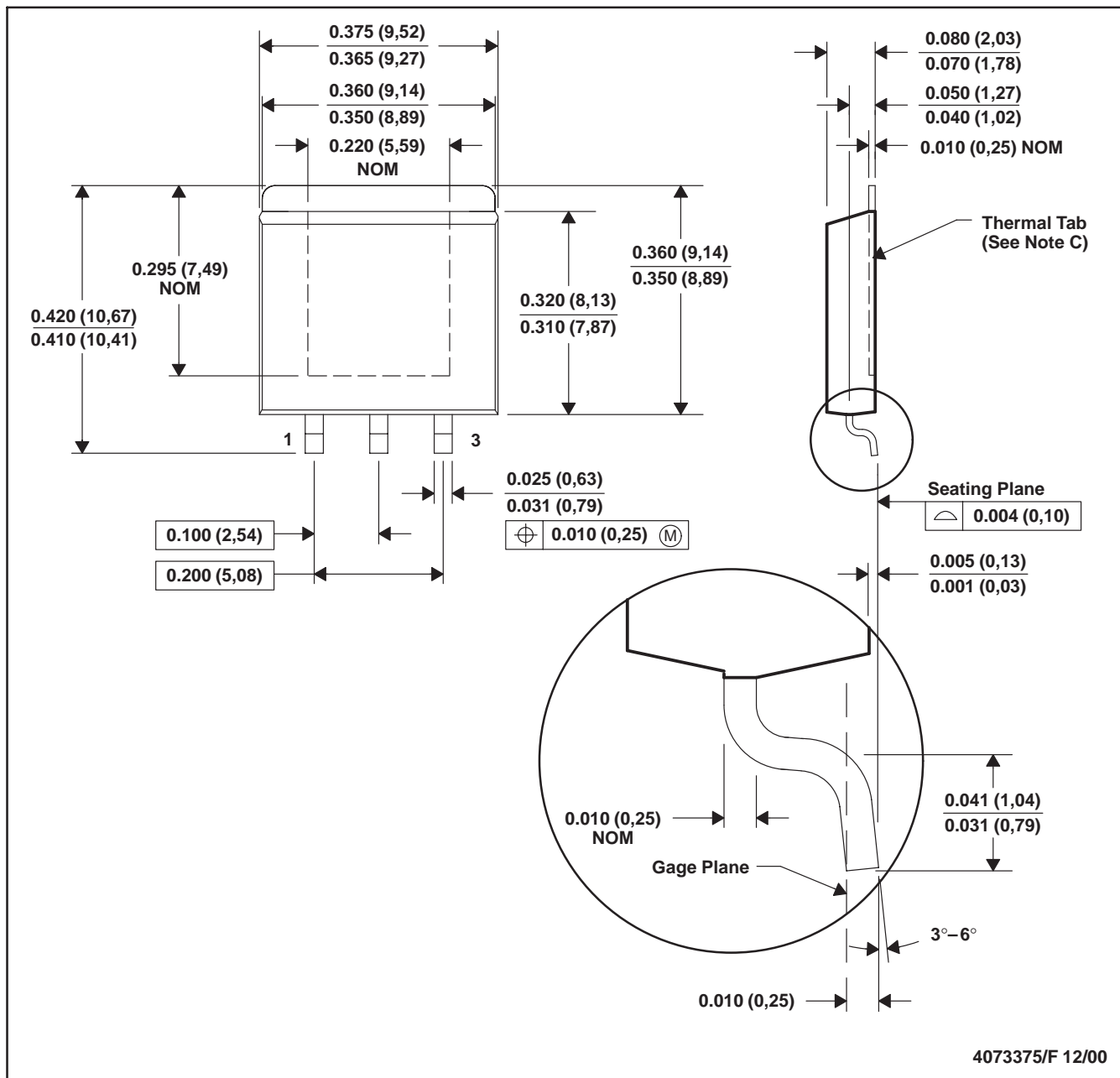


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|------------|--------------|-----------------|------|-----|-------------|------------|-------------|
| TL783CKTTR | DDPAK/TO-263 | KTT | 3 | 500 | 340.0 | 340.0 | 38.0 |

KTE (R-PSFM-G3)

PowerFLEX™ PLASTIC FLANGE-MOUNT



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. The center lead is in electrical contact with the thermal tab.
 D. Dimensions do not include mold protrusions, not to exceed 0.006 (0,15).
 E. Falls within JEDEC MO-169

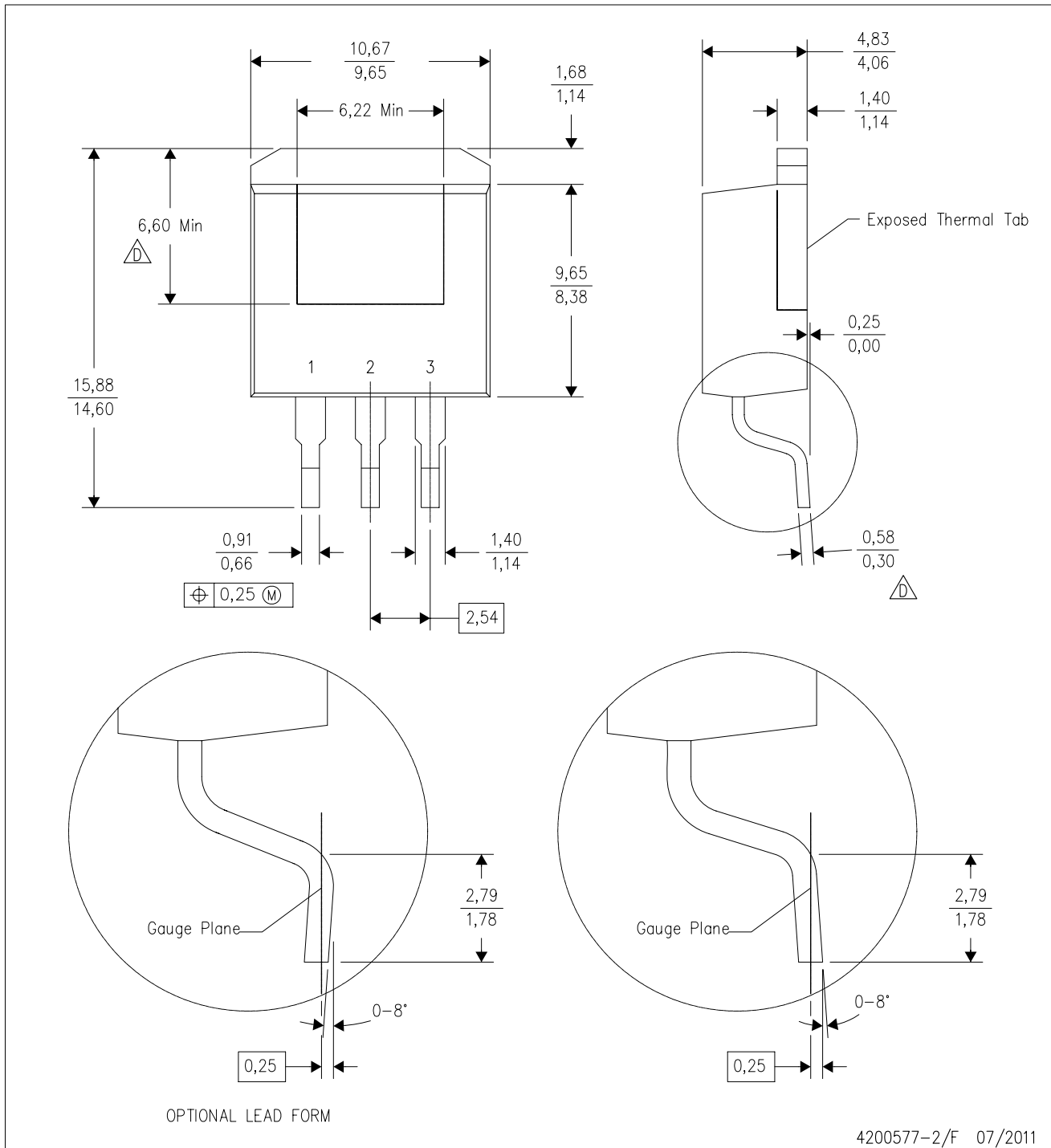
PowerFLEX is a trademark of Texas Instruments.



MECHANICAL DATA

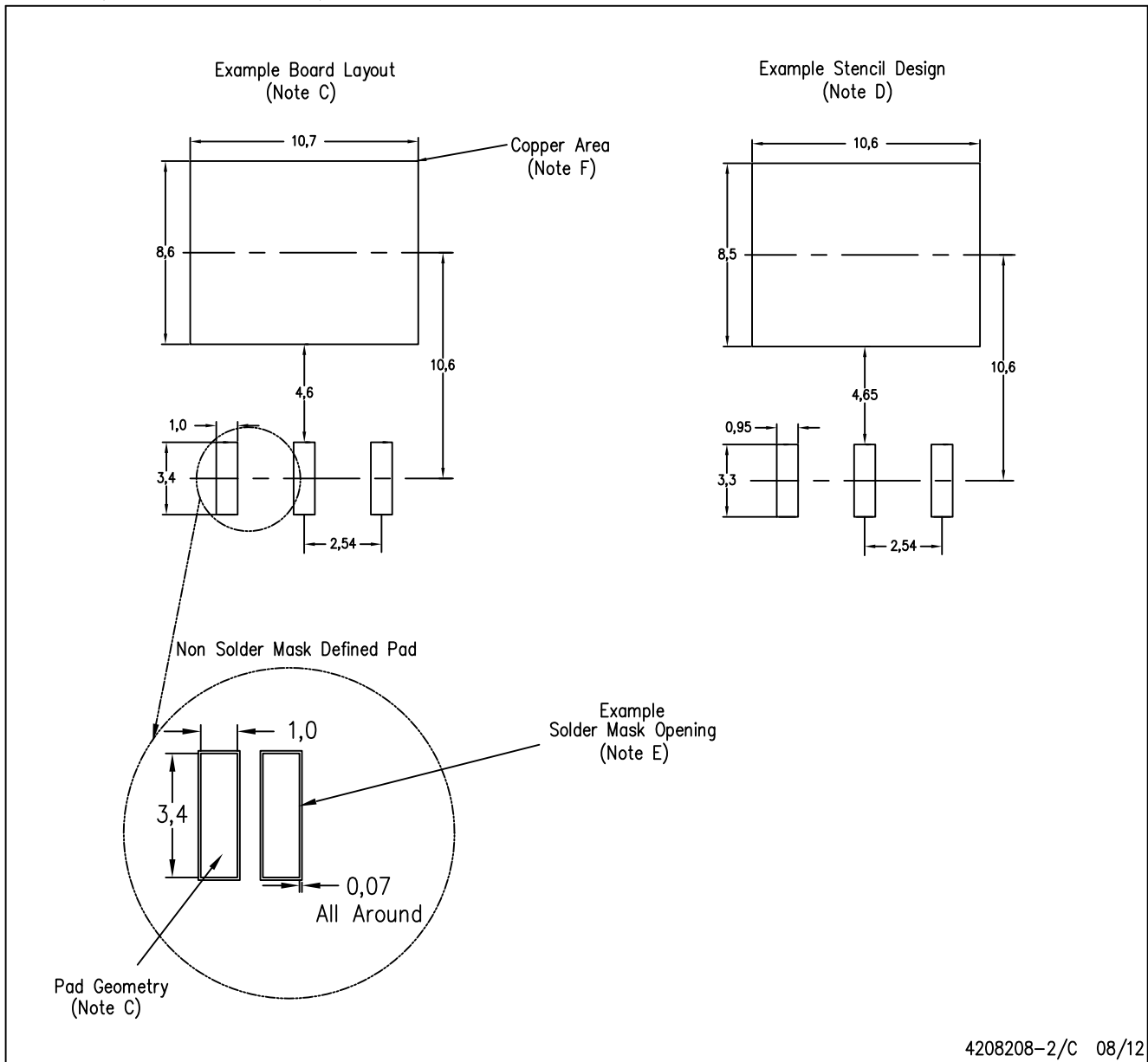
KTT (R-PSFM-G3)

PLASTIC FLANGE-MOUNT PACKAGE



KTT (R-PSFM-G3)

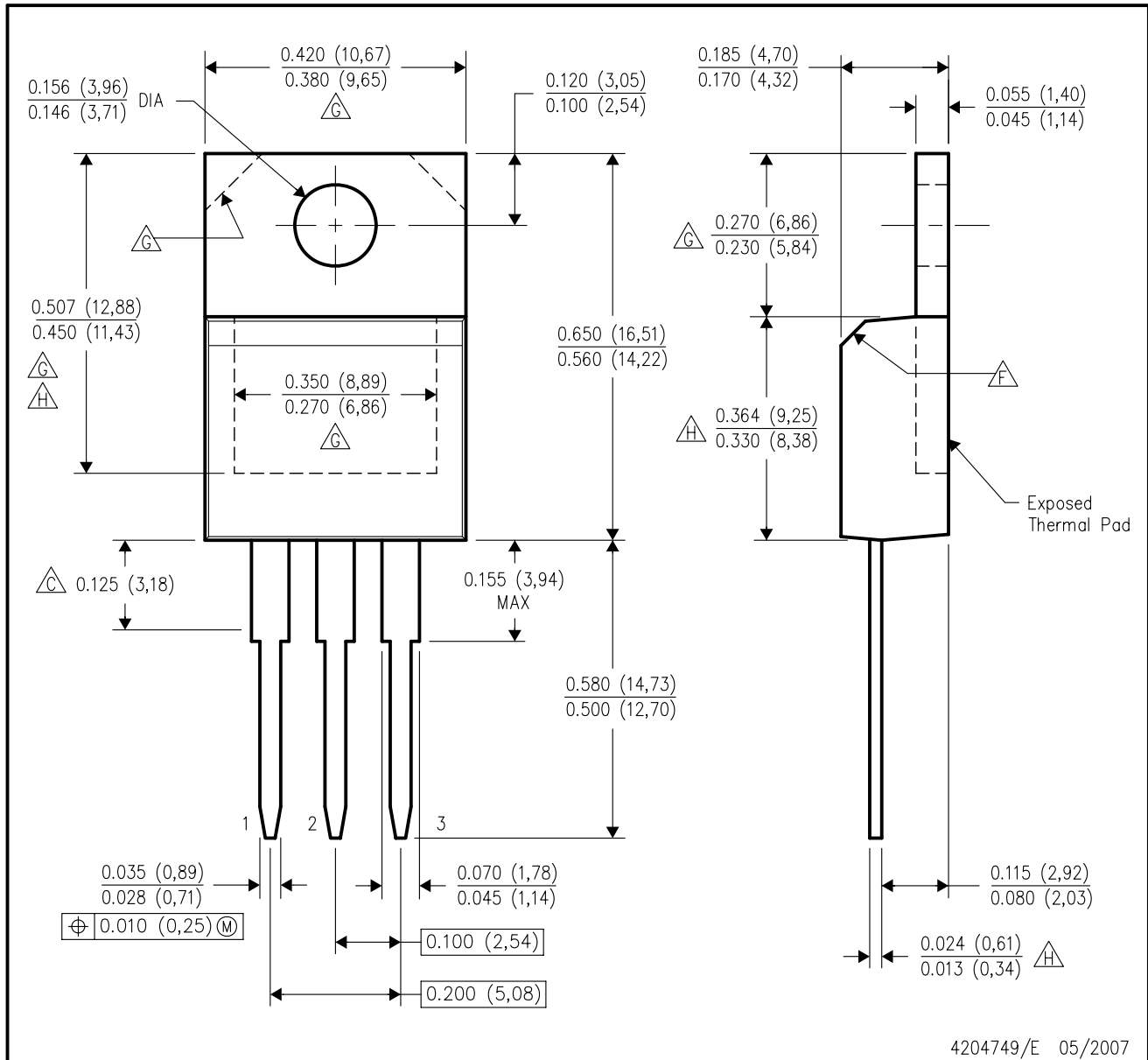
PLASTIC FLANGE-MOUNT PACKAGE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-SM-782 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
 - This package is designed to be soldered to a thermal pad on the board. Refer to the Product Datasheet for specific thermal information, via requirements, and recommended thermal pad size. For thermal pad sizes larger than shown a solder mask defined pad is recommended in order to maintain the solderable pad geometry while increasing copper area.

KCS (R-PSFM-T3)

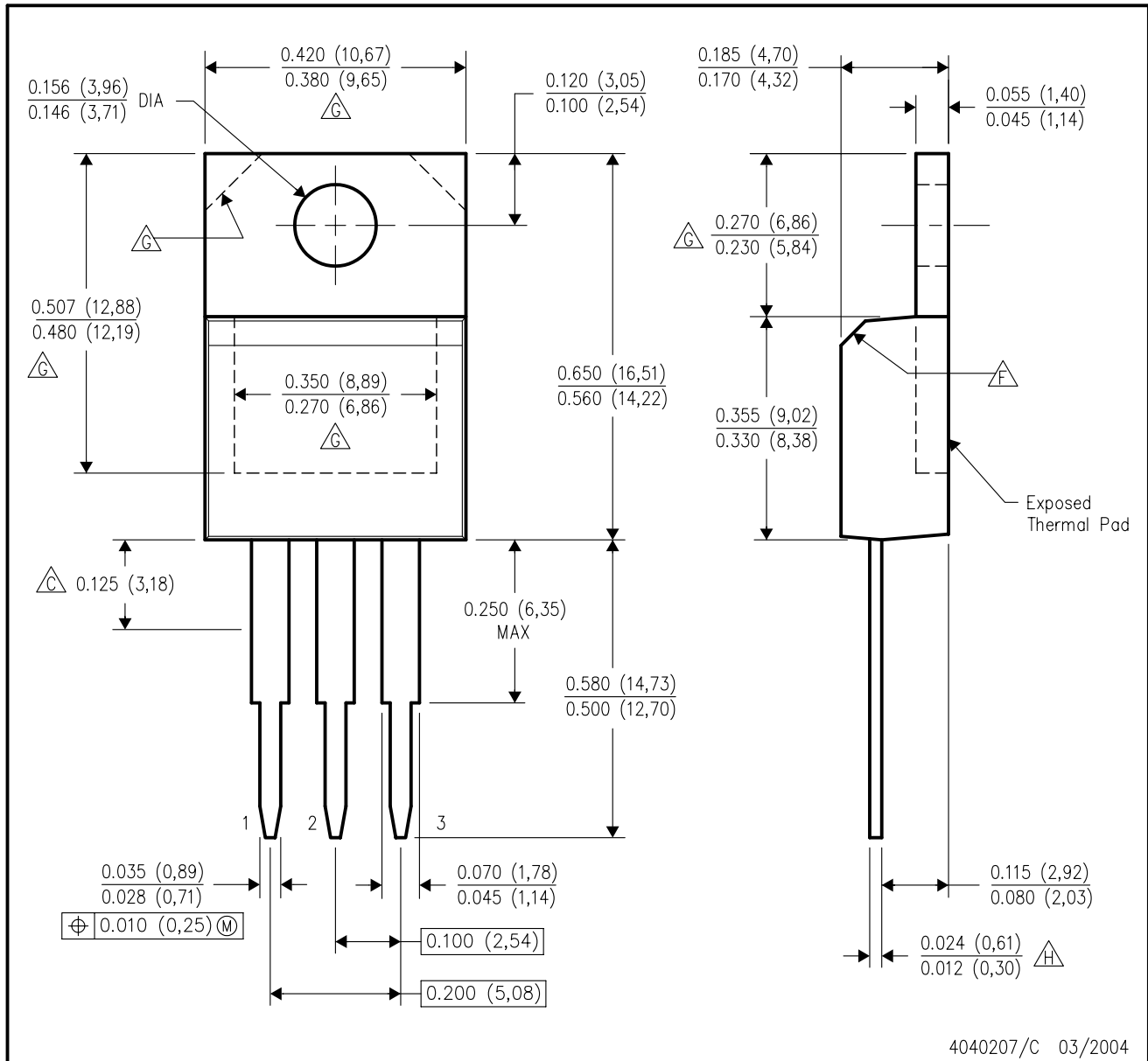
PLASTIC FLANGE-MOUNT PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Lead dimensions are not controlled within this area.
 - D. All lead dimensions apply before solder dip.
 - E. The center lead is in electrical contact with the mounting tab.
 - F. The chamfer is optional.
 - G. Thermal pad contour optional within these dimensions.
 - H. Falls within JEDEC TO-220 variation AB, except minimum lead thickness, minimum exposed pad length, and maximum body length.

KC (R-PSFM-T3)

PLASTIC FLANGE-MOUNT PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Lead dimensions are not controlled within this area.
 - D. All lead dimensions apply before solder dip.
 - E. The center lead is in electrical contact with the mounting tab.
 - F. The chamfer is optional.
 - G. Thermal pad contour optional within these dimensions.
 - H. Falls within JEDEC TO-220 variation AB, except minimum lead thickness.

IMPORTANT NOTICE

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