1. Introduction

25-06327

MII51001-1.9

EPM2210F256C5N

Introduction

The MAX® II family of instant-on, non-volatile CPLDs is based on a 0.18-µm, 6-layer-metal-flash process, with densities from 240 to 2,210 logic elements (LEs) (128 to 2,210 equivalent macrocells) and non-volatile storage of 8 Kbits. MAX II devices offer high I/O counts, fast performance, and reliable fitting versus other CPLD architectures. Featuring MultiVolt core, a user flash memory (UFM) block, and enhanced in-system programmability (ISP), MAX II devices are designed to reduce cost and power while providing programmable solutions for applications such as bus bridging, I/O expansion, power-on reset (POR) and sequencing control, and device configuration control.

Features

The MAX II CPLD has the following features:

- Low-cost, low-power CPLD
- Instant-on, non-volatile architecture
- Standby current as low as 25 µA
- Provides fast propagation delay and clock-to-output times
- Provides four global clocks with two clocks available per logic array block (LAB)
- UFM block up to 8 Kbits for non-volatile storage
- MultiVolt core enabling external supply voltages to the device of either 3.3 V/2.5 V or 1.8 V
- MultiVolt I/O interface supporting 3.3-V, 2.5-V, 1.8-V, and 1.5-V logic levels
- Bus-friendly architecture including programmable slew rate, drive strength, bus-hold, and programmable pull-up resistors
- Schmitt triggers enabling noise tolerant inputs (programmable per pin)
- I/Os are fully compliant with the Peripheral Component Interconnect Special Interest Group (PCI SIG) PCI Local Bus Specification, Revision 2.2 for 3.3-V operation at 66 MHz
- Supports hot-socketing
- Built-in Joint Test Action Group (JTAG) boundary-scan test (BST) circuitry compliant with IEEE Std. 1149.1-1990
- ISP circuitry compliant with IEEE Std. 1532

Table 1–1 shows the MAX II family features.

Table 1–1. MAX II Family Features

Feature	EPM240 EPM240G	EPM570 EPM570G	EPM1270 EPM1270G	EPM2210 EPM2210G	EPM240Z	EPM570Z
LEs	240	570	1,270	2,210	240	570
Typical Equivalent Macrocells	192	440	980	1,700	192	440
Equivalent Macrocell Range	128 to 240	240 to 570	570 to 1,270	1,270 to 2,210	128 to 240	240 to 570
UFM Size (bits)	8,192	8,192	8,192	8,192	8,192	8,192
Maximum User I/O pins	80	160	212	272	80	160
t_{PD1} (ns) *(1)*	4.7	5.4	6.2	7.0	7.5	9.0
f_{CNT} (MHz) *(2)*	304	304	304	304	152	152
t_{SU} (ns)	1.7	1.2	1.2	1.2	2.3	2.2
t_{CO} (ns)	4.3	4.5	4.6	4.6	6.5	6.7

Notes to Table 1–1:

(1) t_{PD1} represents a pin-to-pin delay for the worst case I/O placement with a full diagonal path across the device and combinational logic implemented in a single LUT and LAB that is adjacent to the output pin.

(2) The maximum frequency is limited by the I/O standard on the clock input pin. The 16-bit counter critical delay will run faster than this number.

For more information about equivalent macrocells, refer to the *MAX II Logic Element to Macrocell Conversion Methodology* white paper.

MAX II and MAX IIG devices are available in three speed grades: –3, –4, and –5, with –3 being the fastest. Similarly, MAX IIZ devices are available in three speed grades: –6, –7, and –8, with –6 being the fastest. These speed grades represent the overall relative performance, not any specific timing parameter. For propagation delay timing numbers within each speed grade and density, refer to the *DC and Switching Characteristics* chapter in the *MAX II Device Handbook*.

Table 1–2 shows MAX II device speed-grade offerings.

Table 1–2. MAX II Speed Grades

Device	Speed Grade					
	–3	–4	–5	–6	–7	–8
EPM240 EPM240G	✓	✓	✓	—	—	—
EPM570 EPM570G	✓	✓	✓	—	—	—
EPM1270 EPM1270G	✓	✓	✓	—	—	—
EPM2210	✓	✓	✓	—	—	—
EPM2210G						
EPM240Z	—	—	—	✓	✓	✓
EPM570Z	—	—	—	✓	✓	✓

MAX II devices are available in space-saving FineLine BGA, Micro FineLine BGA, and thin quad flat pack (TQFP) packages (refer to Table 1–3 and Table 1–4). MAX II devices support vertical migration within the same package (for example, you can migrate between the EPM570, EPM1270, and EPM2210 devices in the 256-pin FineLine BGA package). Vertical migration means that you can migrate to devices whose dedicated pins and JTAG pins are the same and power pins are subsets or supersets for a given package across device densities. The largest density in any package has the highest number of power pins; you must lay out for the largest planned density in a package to provide the necessary power pins for migration. For I/O pin migration across densities, cross reference the available I/O pins using the device pin-outs for all planned densities of a given package type to identify which I/O pins can be migrated. The Quartus® II software can automatically cross-reference and place all pins for you when given a device migration list.

Table 1–3. MAX II Packages and User I/O Pins

Device	68-Pin Micro FineLine BGA *(1)*	100-Pin Micro FineLine BGA *(1)*	100-Pin FineLine BGA	100-Pin TQFP	144-Pin TQFP	144-Pin Micro FineLine BGA *(1)*	256-Pin Micro FineLine BGA *(1)*	256-Pin FineLine BGA	324-Pin FineLine BGA
EPM240 EPM240G	—	80	80	80	—	—	—	—	—
EPM570 EPM570G	—	76	76	76	116	—	160	160	—
EPM1270 EPM1270G	—	—	—	—	116	—	212	212	—
EPM2210 EPM2210G	—	—	—	—	—	—	—	204	272
EPM240Z	54	80	—	—	—	—	—	—	—
EPM570Z	—	76	—	—	—	116	160	—	—

Note to Table 1–3:

(1) Packages available in lead-free versions only.

Table 1–4. MAX II TQFP, FineLine BGA, and Micro FineLine BGA Package Sizes

Package	68-Pin Micro FineLine BGA	100-Pin Micro FineLine BGA	100-Pin FineLine BGA	100-Pin TQFP	144-Pin TQFP	144-Pin Micro FineLine BGA	256-Pin Micro FineLine BGA	256-Pin FineLine BGA	324-Pin FineLine BGA
Pitch (mm)	0.5	0.5	1	0.5	0.5	0.5	0.5	1	1
Area (mm2)	25	36	121	256	484	49	121	289	361
Length × width (mm × mm)	5 × 5	6 × 6	11 × 11	16 × 16	22 × 22	7 × 7	11 × 11	17 × 17	19 × 19

MAX II devices have an internal linear voltage regulator which supports external supply voltages of 3.3 V or 2.5 V, regulating the supply down to the internal operating voltage of 1.8 V. MAX IIG and MAX IIZ devices only accept 1.8 V as the external supply voltage. MAX IIZ devices are pin-compatible with MAX IIG devices in the 100-pin Micro FineLine BGA and 256-pin Micro FineLine BGA packages. Except for external supply voltage requirements, MAX II and MAX II G devices have identical pin-outs and timing specifications. Table 1–5 shows the external supply voltages supported by the MAX II family.

Table 1–5. MAX II External Supply Voltages

Devices	EPM240 EPM570 EPM1270 EPM2210	EPM240G EPM570G EPM1270G EPM2210G EPM240Z EPM570Z *(1)*
MultiVolt core external supply voltage (V_{CCINT}) *(2)*	3.3 V, 2.5 V	1.8 V
MultiVolt I/O interface voltage levels (V_{CCIO})	1.5 V, 1.8 V, 2.5 V, 3.3 V	1.5 V, 1.8 V, 2.5 V, 3.3 V

Notes to Table 1–5:

(1) MAX IIG and MAX IIZ devices only accept 1.8 V on their VCCINT pins. The 1.8-V V_{CCINT} external supply powers the device core directly.

(2) MAX II devices operate internally at 1.8 V.

Referenced Documents

This chapter references the following documents:

- *DC and Switching Characteristics* chapter in the *MAX II Device Handbook*
- *MAX II Logic Element to Macrocell Conversion Methodology* white paper

Document Revision History

Table 1–6 shows the revision history for this chapter.

Table 1–6. Document Revision History

Date and Revision	Changes Made	Summary of Changes
August 2009, version 1.9	■ Updated Table 1–2.	Added information for speed grade –8
October 2008, version 1.8	■ Updated "Introduction" section. ■ Updated new Document Format.	—
December 2007, version1.7	■ Updated Table 1–1 through Table 1–5. ■ Added "Referenced Documents" section.	Updated document with MAX IIZ information.
December 2006, version 1.6	■ Added document revision history.	—
August 2006, version 1.5	■ Minor update to features list.	—
July 2006, version 1.4	■ Minor updates to tables.	—

Table 1–6. Document Revision History

Date and Revision	Changes Made	Summary of Changes
June 2005, version 1.3	■ Updated timing numbers in Table 1-1.	—
December 2004, version 1.2	■ Updated timing numbers in Table 1-1.	—
June 2004, version 1.1	■ Updated timing numbers in Table 1-1.	—

Altera Device Package Information

04R-00227-1.0

256 Pin Fineline Ball-Grid Array (FBGA) - Wire Bond - A:1.90

- All dimensions and tolerances conform to ASME Y14.5M – 1994.
- Controlling dimension is in millimeters.
- Pin A1 may be indicated by an ID dot, or a special feature, in its proximity on package surface.

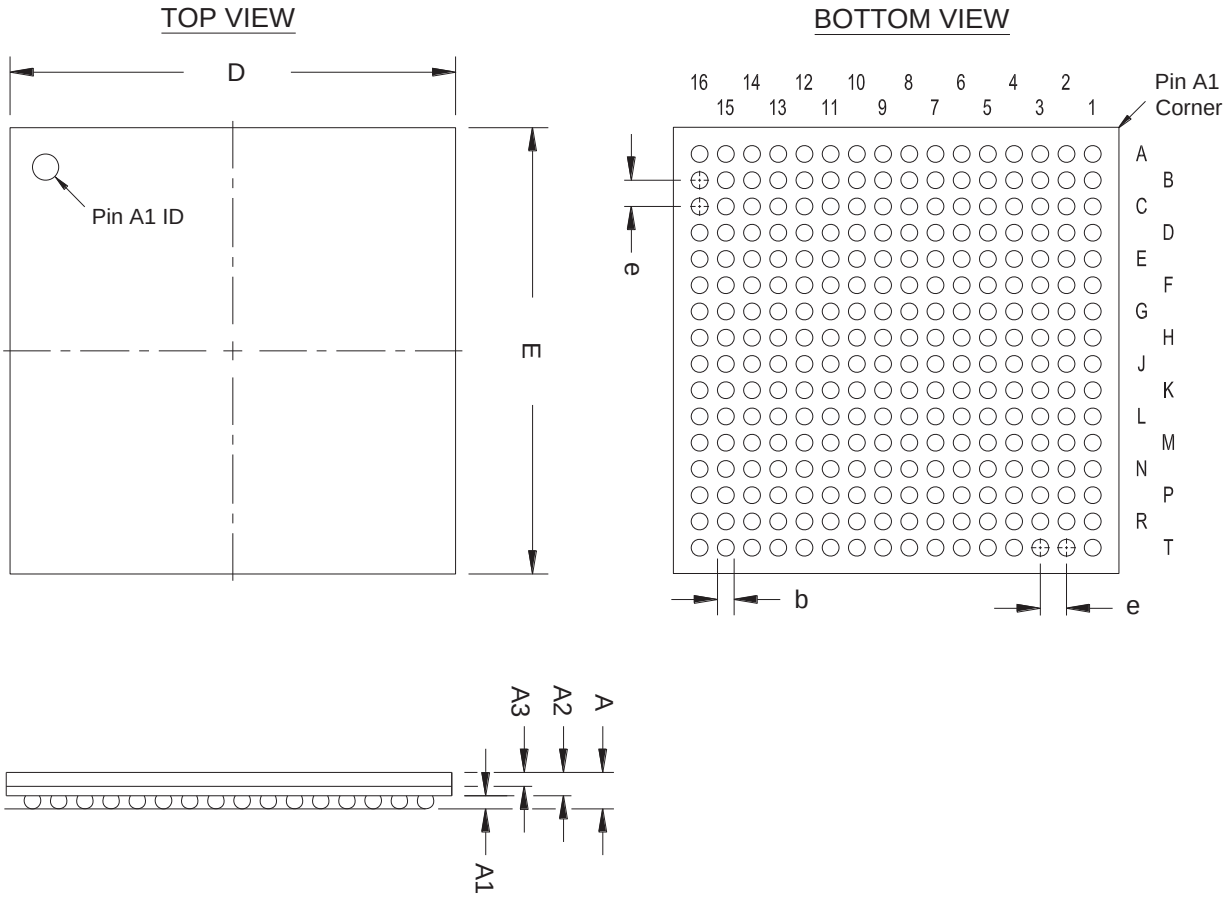
Package Information

Description	Specification
Ordering Code Reference	F
Package Acronym	FBGA
Substrate Material	BT
Solder ball composition	Regular: 63Sn:37Pb (Typ.) Pb-free: Sn:3Ag:0.5Cu (Typ.)
JEDEC Outline Reference	MS-034 Variation: AAF-1
Lead Coplanarity	0.008 inch (0.20 mm)
Weight	1.1 g (Typ.)
Moisture Sensitivity Level	Printed on moisture barrier bag

Package Outline Dimension Table

Symbol	Millimeters		
	Min.	Nom.	Max.
A	1.60	1.75	1.90
A1	0.40	0.50	0.60
A2	1.00	1.25	1.50
A3	0.65	0.70	0.75
D	17.00 BSC		
E	17.00 BSC		
b	0.50	0.60	0.70
e	1.00 BSC		

Package Outline



Document Revision History

Table 1 shows the revision history for this document.

Table 1. Document Revision History

Date	Version	Changes
July 2011	1.0	Initial release

101 Innovation Drive
San Jose, CA 95134
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Designing With High-Density BGA Packages for Altera Devices

December 2007, ver. 5.1 Application Note 114

Introduction

As programmable logic devices (PLDs) increase in density and I/O pins, the demand for small packages and diverse packaging options continues to grow. Ball-grid array (BGA) packages are an ideal solution because the I/O connections are on the interior of the device, improving the ratio between pin count and board area. Typical BGA packages contain up to twice as many connections as quad flat pack (QFP) packages for the same area. Further, BGA solder balls are considerably stronger than QFP leads, resulting in robust packages that can tolerate rough handling.

Altera has developed high-density BGA solutions for users of high-density PLDs. These new formats require less than half the board space of standard BGA packages.

This application note provides guidelines for designing your printed circuit board (PCB) for Altera's high-density BGA packages and discusses:

- Overview of BGA Packages
- PCB Layout Terminology
- PCB Layout for High-Density BGA Packages

Overview of BGA Packages

In BGA packages, the I/O connections are located on the interior of the device. Leads normally placed along the periphery of the package are replaced with solder balls arranged in a matrix across the bottom of the substrate. The final device is soldered directly to the PCB using assembly processes that are virtually identical to the standard surface mount technology preferred by system designers.

Additionally, BGA packages provide the following advantages:

- *Fewer damaged leads*—BGA leads consist of solid solder balls, which are less likely to suffer damage during handling.
- *More leads per unit area*—Lead counts are increased by moving the solder balls closer to the edges of package and by decreasing pitch to 1.0 mm for flip-chip BGAs and 0.8 mm for micro-BGAs.

- *Less expensive surface mount equipment*—BGA packages can tolerate slightly imperfect placement during mounting, requiring less expensive surface mount equipment. The placement can be imperfect because the BGA packages self-align during solder reflow.
- *Smaller footprints*—BGA packages are usually 20% to 50% smaller than QFP packages, making BGA packages more attractive for applications that require high performance and a smaller footprint.
- *Integrated circuit speed advantages*—BGA packages operate well into the microwave frequency spectrum and achieve high electrical performance by using ground planes, ground rings, and power rings in the package construction.
- *Improved heat dissipation*—Because the die is located at the center of the BGA package and most GND and VCC pins are located at the center of the package, the GND and VCC pins are located under the die. As a result, the heat generated in the device can be transferred out through the GND and VCC pins (i.e., the GND and VCC pins act as a heat sink).

PCB Layout Terminology

This section defines common terms used in PCB layout that you need to know to design with Altera's high-density BGAs.

Escape Routing

Escape routing is the method used to route each signal from a package to another element on the PCB.

Multi-Layer PCBs

The increased I/O count associated with BGA packages has made multi-layer PCBs the industry-standard method for performing escape routing. Signals can be routed to other elements on the PCB through various numbers of PCB layers.

Vias

Vias, or plated through holes, are used in multi-layer PCBs to transfer signals from one layer to another. Vias are actual holes drilled through a multi-layer PCB and provide electrical connections between various PCB layers. All vias provide layer-to-layer connections only. Device leads or other reinforcing materials are not inserted into vias.

Table 1 describes the terms used to define via dimensions.

Table 1. Via Dimension Terms

Term	Definition
Aspect ratio	The ratio of a via's length or depth to its pre-plated diameter
Drilled hole diameter	The final diameter of the actual via hole drilled in the board
Finished via diameter	The final diameter of a via hole after it has been plated

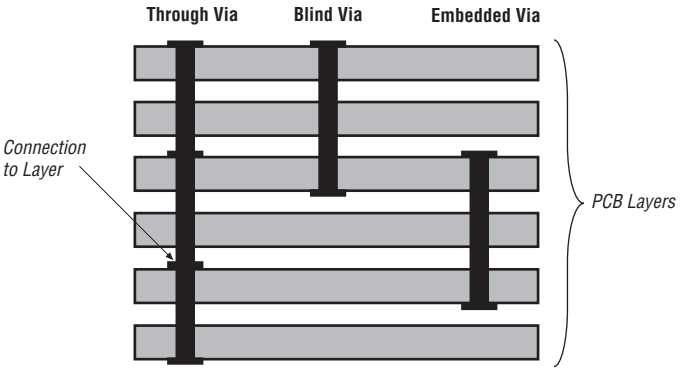
Table 2 shows the three via types typically used on PCBs.

Table 2. Via Types

Type	Description
Through via	An interconnection between the top and the bottom layer of a PCB. Vias also provide interconnections to inner PCB layers.
Blind via	An interconnection from the top or bottom layer to an inner PCB layer.
Embedded via	An interconnection between any numbers of inner PCB layers.

Figure 1 shows all three via types.

Figure 1. Types of Vias



Blind vias and through vias are used more frequently than embedded vias. Blind vias can be more expensive than through vias, but overall costs are reduced when signal traces are routed under a blind via, requiring fewer PCB layers. Through vias, on the other hand, do not permit signals to be routed through lower layers, which can increase the required number of PCB layers and overall costs.

Via Capture Pad

Vias are connected electrically to PCB layers through via capture pads that surround each via.

Surface Land Pad

Surface land pads are the areas on the PCB to which the BGA solder balls adhere. The size of these pads affects the space available for vias and for the escape routing. In general, surface land pads are available in the following two basic designs:

- Non solder mask defined (NSMD), also known as copper defined
- Solder mask defined (SMD)

The main differences between the two surface land pad types are the size of the trace and space, the type of vias you can use, and the shapes of the solder balls after solder reflow.

Non Solder Mask Defined Pad

In the NSMD pad, the solder mask opening is larger than the copper pad. Thus, the surface land pad's copper surface is completely exposed, providing greater area to which the BGA solder ball can adhere (see Figure 2).

Altera recommends that you use a NSMD pad for most applications because it provides more flexibility, fewer stress points, and more line-routing space between pads.

Solder Mask Defined Pad

In SMD pad, the solder mask overlaps the surface land pad's copper surface (see Figure 2 on page 5). This overlapping provides greater adhesion strength between the copper pad and the PCB's epoxy/glass laminate, which can be important under extreme bending and during accelerated thermal cycling tests. However, the solder mask overlap reduces the amount of copper surface available for the BGA solder ball.

Figure 2. Side View of NSMD & SMD Land Pads

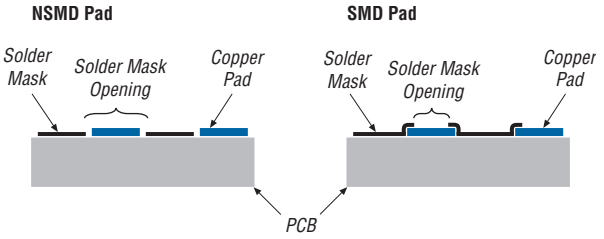
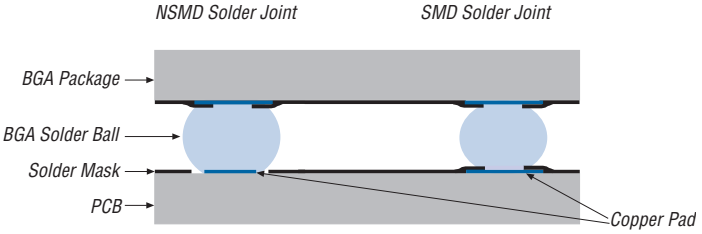


Figure 3 shows the side view for an NSMD and SMD solder joint.

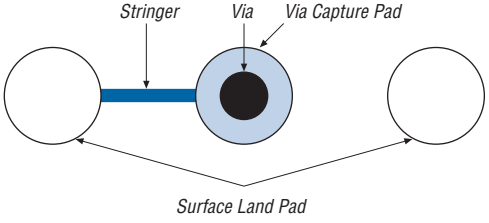
Figure 3. Side View of NSMD & SMD Solder Joints



Stringer

Stringers are rectangular or square interconnect segments that electrically connect via capture pads and surface land pads. Figure 4 shows the connection between vias, via capture pads, surface land pads, and stringers.

Figure 4. Via, Land Pad, Stringer & Via Capture Pad



PCB Layout for High-Density BGA Packages

When designing a PCB for high-density BGA packages, consider the following factors:

- Surface land pad dimension
- Via capture pad layout and dimension
- Signal-line space and trace width
- Number of PCB layers

Controlling dimension is calculated in millimeters for all high-density BGA figures

Surface Land Pad Dimension

Altera has done extensive modeling simulation and experimental studies to determine the optimum land pad design on the PCB to provide the longest solder joint fatigue life. The results of these studies show that a pad design that provides a balanced stress on the solder joint provides the best solder joint reliability. Since the BGA pads are solder mask defined, if SMD pads are used on the PCB, the surface land pads should be the same size as the BGA pad to provide a balanced stress on solder joints. If non-solder mask defined pads are used on the PCB, the land pads should be approximately 15% smaller than the BGA pad size to achieve a balanced stress on solder joints.

Table 3 on page 7 lists the recommended pad sizes for SMD and NSMD land patterns. You should use NSMD pads for high-density board layouts because the smaller pad sizes allow for more space between vias and trace routing. As an example, Figure 6 on page 8 shows the space available for vias and escape routing when you use NSMD surface land pads for a 1.00-mm flip-chip BGA.

Figure 5. BGA Pad Dimensions

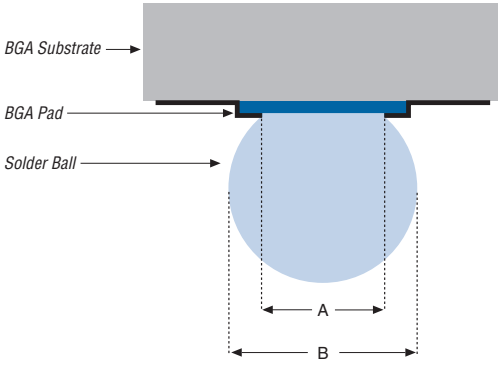


Table 3 shows the recommended pad sizes for SMD and NSMD land patterns.

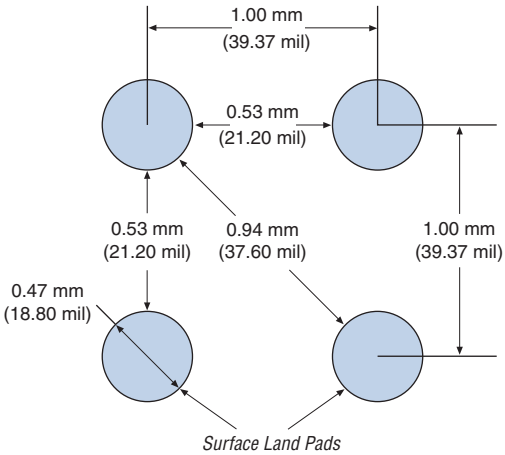
Table 3. Recommended Pad Sizes for SMD & NSMD Pads

BGA Pad Pitch	BGA Pad Opening (A) (mm)	Solder Ball Diameter (B) (mm)	Recommended SMD Pad Size (mm)	Recommended NSMD Pad Size (mm)
1.27 mm (Plastic Ball Grid Array (PBGA))	0.60	0.75	0.60	0.51
1.27 mm (Super Ball Grid Array (SBGA))	0.60	0.75	0.60	0.51
1.27 mm (Tape Ball Grid Array (TBGA))	0.60	0.75	0.60	0.51
1.27 mm (flip-chip) *(1)*	0.65	0.75	0.65	0.55
1.00 mm (wirebond) *(1)*	0.45	0.63	0.45	0.38
1.00 mm (flip-chip) *(1)*	0.55	0.63	0.55	0.47
1.00 mm (flip-chip) *(1)* APEX 20KE	0.60	0.65	0.60	0.51
0.80 mm UBGA (BT Substrate)	0.4	0.55	0.4	0.34
0.80 mm UBGA (EPC16U88)	0.4	0.45	0.4	0.34
0.50 mm MBGA	0.3	0.3	0.27	0.26

Note to Table 3:

(1) FineLine BGA® packages that use flip-chip technology are marked "Thermally Enhanced FineLine BGA" and wirebond packages are marked "Non-Thermally Enhanced FineLine BGA" in the *Altera Device Package Information Data Sheet*.

Figure 6. Via & Routing Space Available for 1.00-mm Flip-Chip BGA NSMD Land Pads



Via Capture Pad Layout & Dimension

The size and layout of via capture pads affect the amount of space available for escape routing. In general, you can lay out via capture pads in the following two ways:

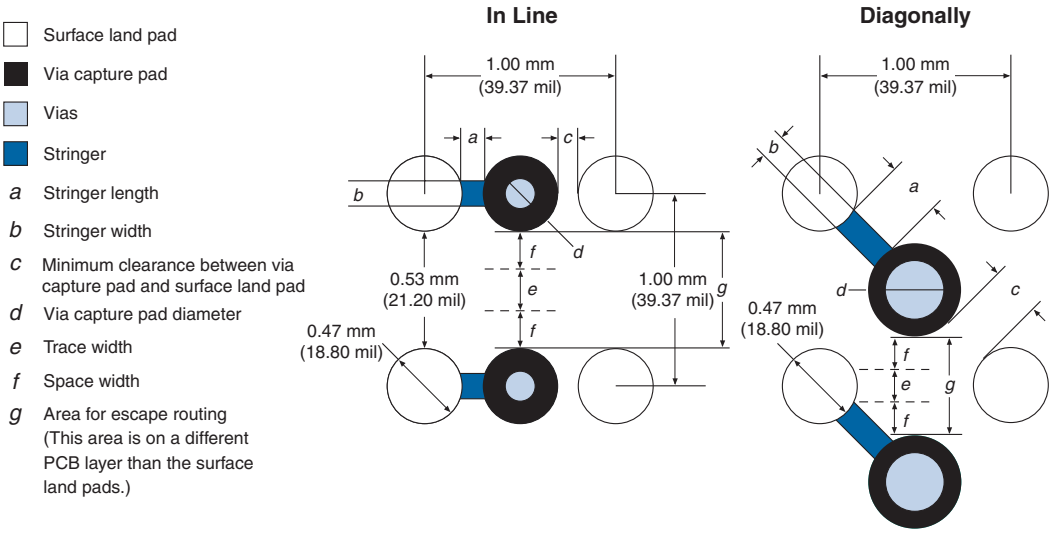
- In-line with the surface land pads

  or

- Diagonal of the surface land pads.

Figure 7 shows both layouts for 1.00-mm flip-chip BGA NSMD land pads.

Figure 7. Placement of Via Capture Pad for 1.00-mm Flip-Chip BGA NSMD Land Pads



The decision to place the via capture pads diagonally or in-line with the surface lands pads is based on the following factors:

- Diameter of the via capture pad
- Stringer length
- Clearance between via capture pad and surface land pad

To decide how to lay out your PCB, use the information shown in Figure 7 and Table 4. If your PCB design guidelines do not conform to either equation in Table 4, contact Altera® Applications for further assistance.

Table 4. Formula for Via Layouts for 1.00-mm Flip-Chip BGA NSMD Land Pads

Layout	Formula
In-line	$a + c + d \leq$ 0.53 mm
Diagonally	$a + c + d \leq$ 0.94 mm

Table 4 shows that you can place a larger via capture pad diagonally than in-line with the surface land pads.

Via capture pad size also affects how many traces can be routed on a PCB. Figure 8 shows sample layouts of typical and premium via capture pads. The typical layout shows a via capture pad size of 0.66 mm, a via size of 0.254 mm, and an inner space and trace of 0.102 mm. With this layout, only one trace can be routed between the vias. If more traces are required, you must reduce the via capture pad size or the space and trace size.

The premium layout shows a via capture pad size of 0.508 mm, a via size of 0.203 mm, and an inner space and trace of 0.076 mm. This layout provides enough space to route two traces between the vias.

Figure 8. Typical & Premium Via Capture Pad Sizes for a 1.00-mm Flip-Chip BGA

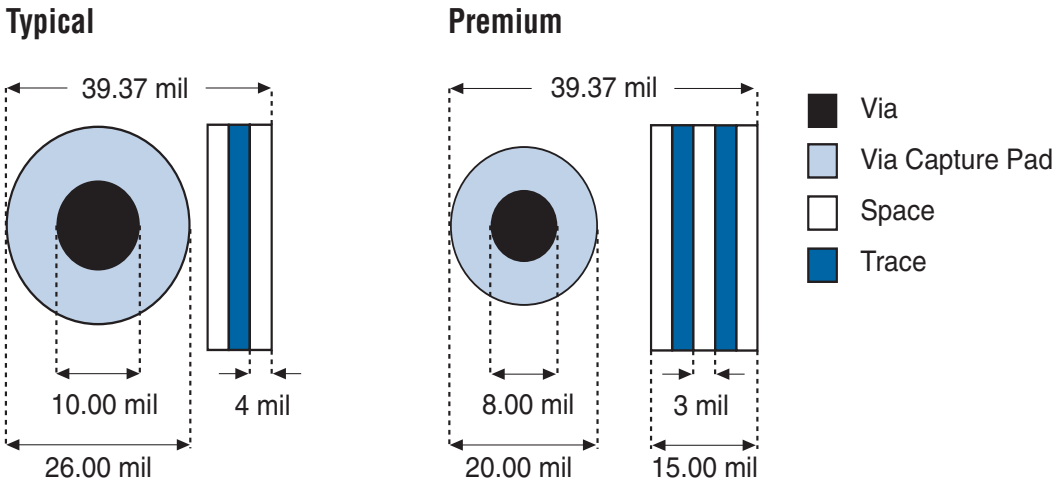


Table 5 shows the typical and premium layout specifications used by most PCB vendors.

Table 5. PCB Vendor Specifications

Specification	Typical (mm)	Premium (mm) PCB Thickness > 1.5 mm	Premium (mm) PCB Thickness <= 1.5 mm
Trace & space width	0.1/0.1	0.076/0.076	0.076/0.076
Drilled hole diameter	0.305	0.254	0.15
Finished via diameter	0.254	0.203	0.1
Via capture pad	0.66	0.508	0.275
Aspect ratio	7:1	10:1	10:1

For detailed information on drill sizes, via sizes, space and trace sizes, or via capture pad sizes, contact your PCB vendor directly.

Signal Line Space & Trace Width

The ability to perform escape routing is defined by the width of the trace and the minimum space required between traces. The minimum area for signal routing is the smallest area that the signal must be routed through (i.e., the distance between two vias, or *g* in Figure 9). This area is calculated by the following formula:

g = (BGA pitch) – d

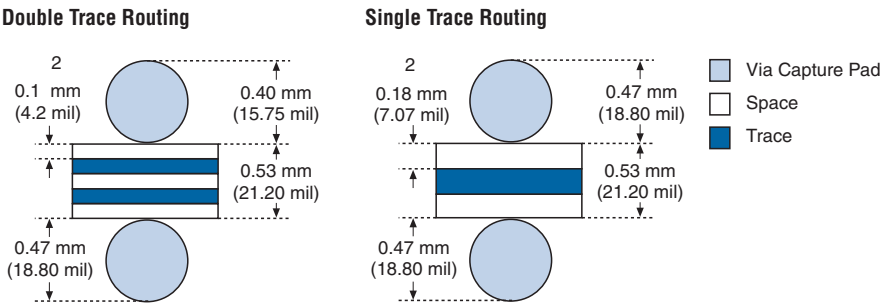
The number of traces that can be routed through this area is based on the permitted line trace and space widths. You can use Table 6 to determine the total number of traces that can be routed through *g*.

Table 6. Number of Traces

Number of Traces	Formula
1	$g \geq [2 \times (\text{space width})] + \text{trace width}$
2	$g \geq [3 \times (\text{space width})] + [2 \times (\text{trace width})]$
3	$g \geq [5 \times (\text{space width})] + [3 \times (\text{trace width})]$

Figure 9 shows that by reducing the trace and space size, you can route more traces through *g*. Increasing the number of traces reduces the required number of PCB layers and decreases the overall cost.

Figure 9. Escape Routing for Double & Single Traces for 1.00-mm Flip-Chip BGA



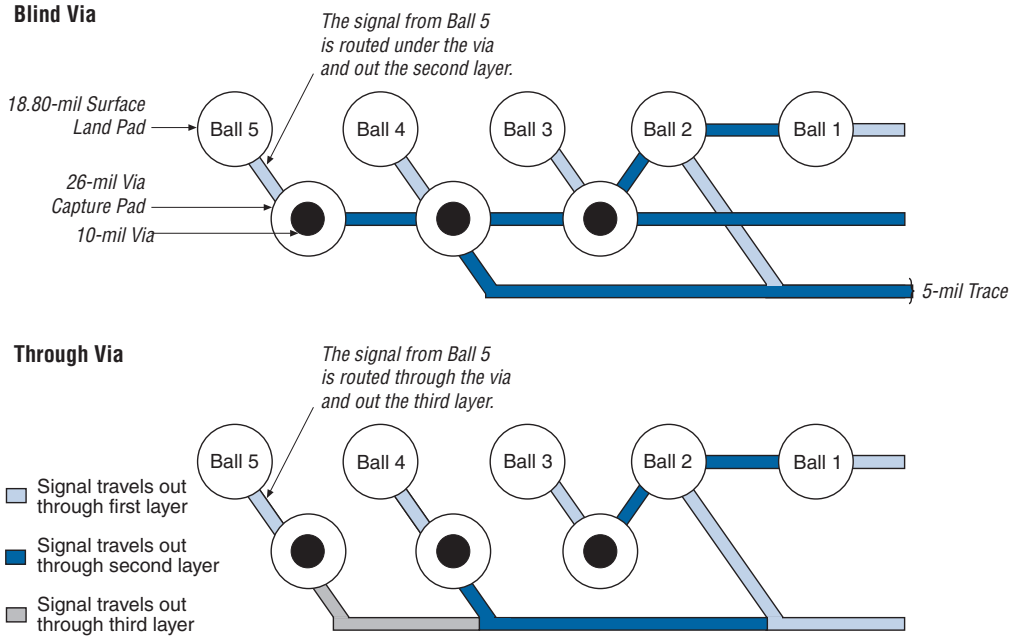
Number of PCB Layers

In general, the number of PCB layers required to route signals is inversely proportional to the number of traces between vias (i.e., the more traces used, the fewer PCB layers required). You can estimate the number of layers your PCB requires by first determining:

- Trace and space size
- Number of traces routed between the via capture pads
- Type of vias used

Using fewer I/O pins than the maximum can reduce the required number of layers. The via type selected can also reduce the number of layers required. To see how the via type can affect the required number of PCB layers, consider the sample layouts shown in Figure 10.

Figure 10. Sample PCB Layout for 1.00-mm Flip-Chip BGA



The blind via layout in Figure 10 requires only two PCB layers. The signals from the first two balls can be routed directly through the first layer. The signals from the third and fourth balls can be routed through a

via and out the second layer, and the signal from the fifth ball can be routed under the vias for third and fourth balls and out the second layer. Together, only two PCB layers are required.

In contrast, the through via layout in Figure 10 requires three PCB layers, because signals cannot be routed under through vias. The signals from the third and fourth balls can still be routed through a via and out the second layer, but the signal from the fifth ball must be routed through a via and out the third layer. Using blind vias rather than through vias in this example saves one PCB layer.

In 2006, Altera introduced 0.5 mm pitch Micro FineLine BGA® (MBGA) packages on the MAX II device family. The size and weight of these packages make them suitable for portable applications or any application that has board space and/or power constraints. The pin layout and the pin assignments have been designed so that the signals from solder pads can be routed in 2 layers using through-hole vias. Examples of layout schemes for routing on 2 layers is demonstrated in Figures 11 and 12 for the 100-pin and 256-pin MBGAs, respectively. This layout type is suitable for PCB thickness smaller than or equal to 1.5 mm. For PCB thickness greater than 1.5 mm, application of blind vias may be more suitable for escape routing.

In this section, sample PCB routing schemes use VCCN and VSS. In the pin table, VCCN and VSS corresponds to VCCIO and GND, respectively.

Figure 11. A Sample PCB Routing Scheme on 2 Layers for 0.5 mm 100-pin MBGA

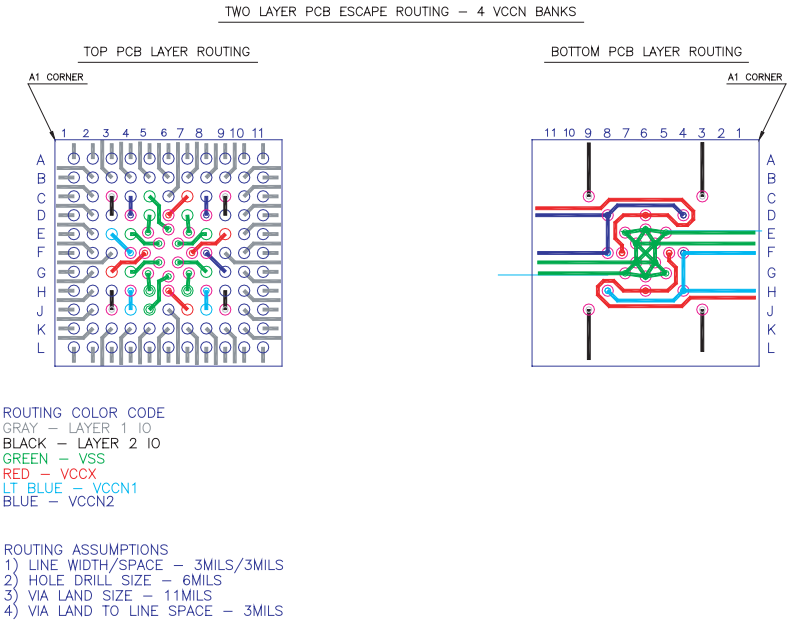
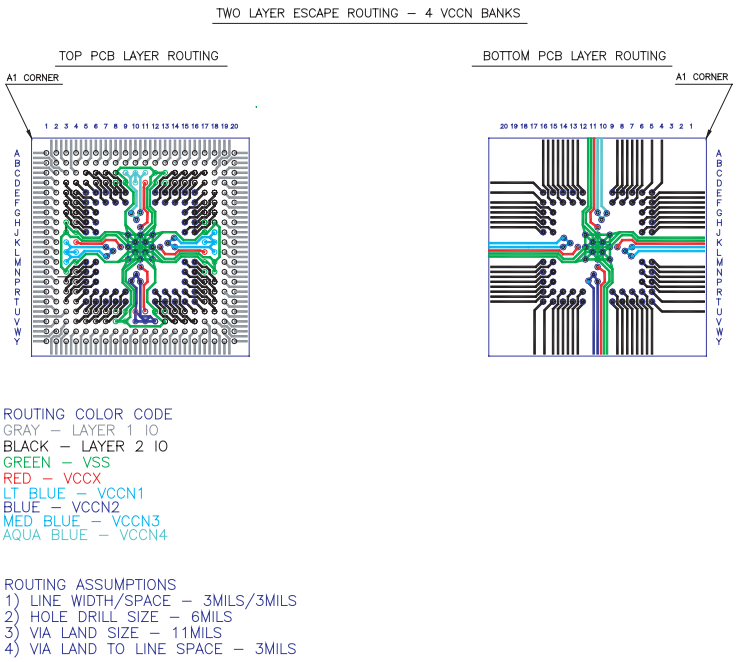


Figure 12. A Sample PCB Routing Scheme on 2 Layers for 0.5 mm 256-pin MBGA



In 2007, Altera introduced 68-pin and 144-pin MBGA packages for the MAX IIZ device family. Examples of layout schemes for routing are demonstrated for 68-pin, and 144-pin MBGA packages in Figures 13, 14, and 15, respectively. The 68-pin package is routed in 2 layers and the 144-pin package uses 4-layers.

Figure 13. A Sample PCB Routing Scheme on 2 Layers for 0.5 mm 68-pin MBGA (Separate VCCN Banks)

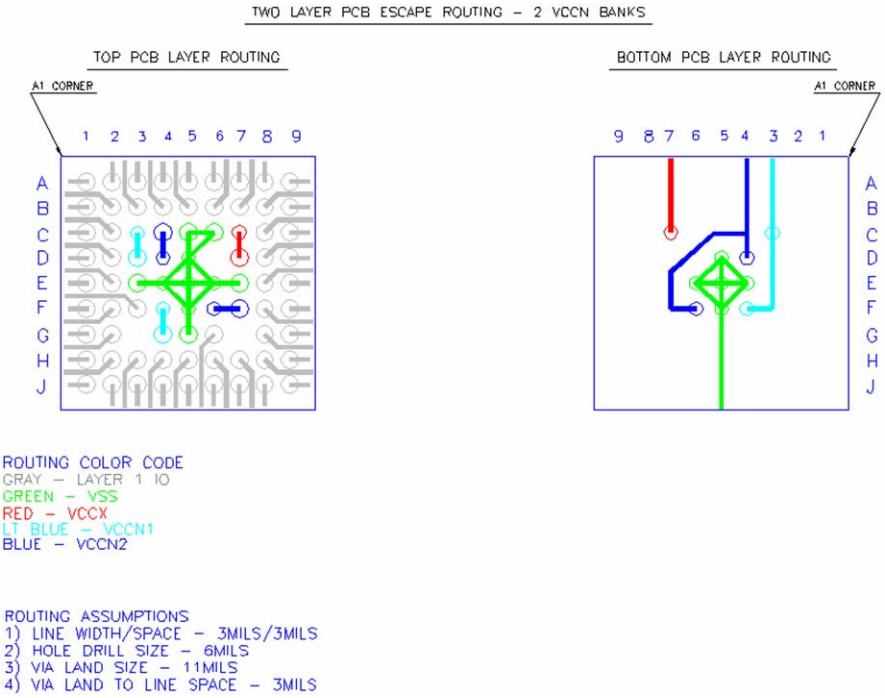


Figure 14. A Sample PCB Routing Scheme on 2 Layers for 0.5 mm 68-pin MBGA (Common VCCN Bank)

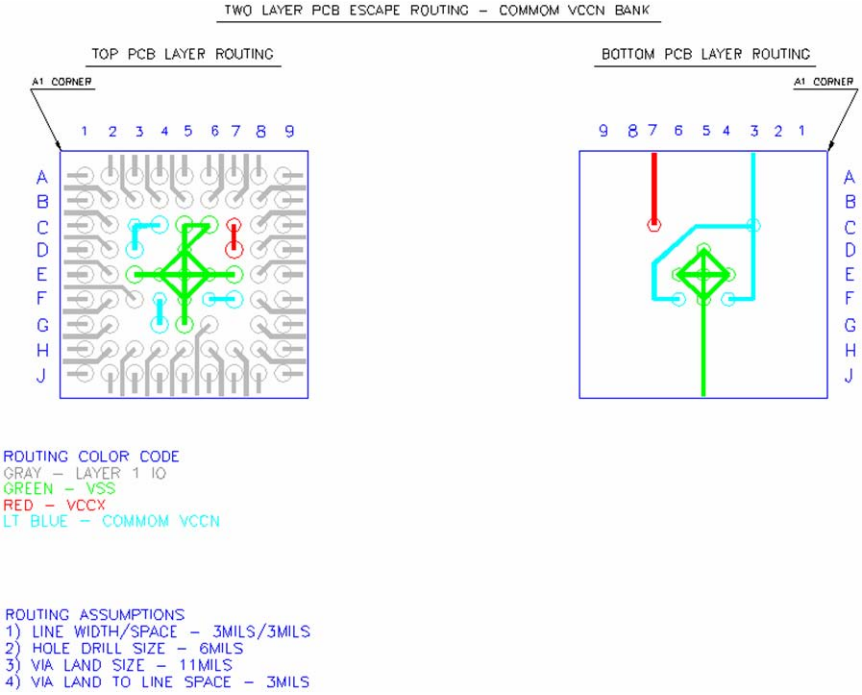
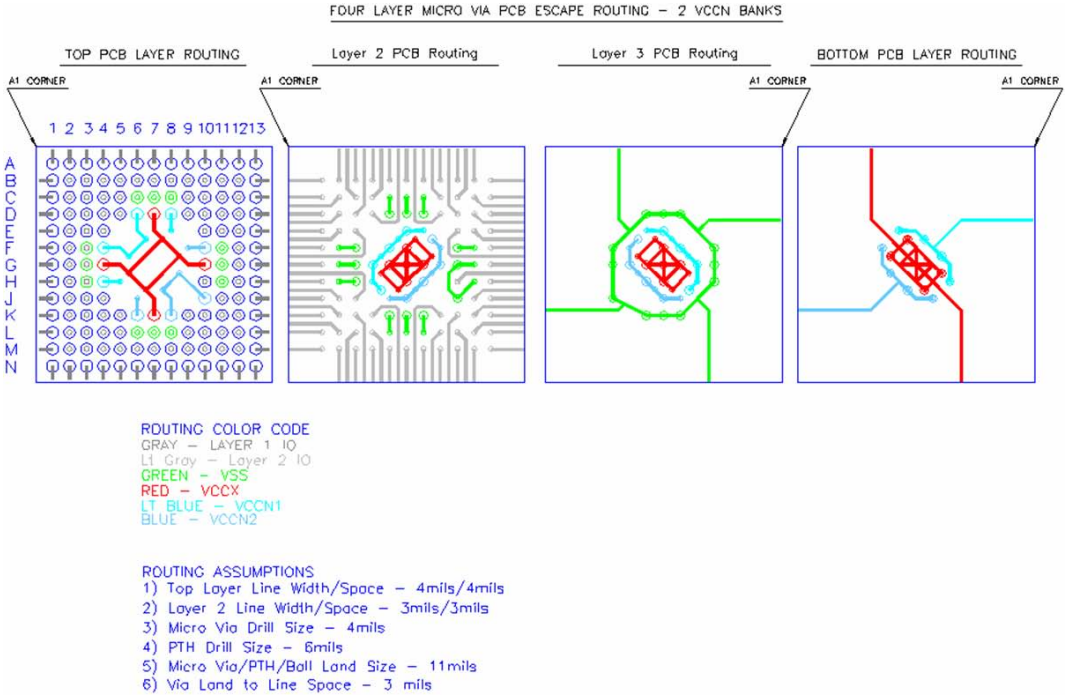


Figure 15. A Sample PCB Routing Scheme on 4 Layers for 0.5 mm 144-pin MBGA



Conclusion

Altera has taken a leadership position in PLD packaging with the introduction of high-density BGA packages. These packages use a reduced PCB area while maintaining a very high pin count. By using the information in this application note, you can easily design PCBs to use high-density BGA packages, and take advantage of the package's reduced size.

References

Yuan Li. Anil Pannikkat, Larry Anderson, Tarun Verma, Bruce Euzent, *Building Reliability Into Full-Array BGA's*, 26th IEMT Symposium, PackCon 2000.

Revision History

Version 5.1

Information contained in *AN 114: Designing With High-Density BGA Packages for Altera Devices* version 5.1 supersedes information published in previous versions.

- Additional samples were added in "Number of PCB Layers" on page 12.

Version 5.0

Information contained in *AN 114: Designing With High-Density BGA Packages for Altera Devices* version 5.0 supersedes information published in previous versions.

- Updated Table 3 to include pad recommendations for 0.5 mm MBGA
- Updated Table 5 to reflect the current PCB vendor capability.
- Added the MBGA update to "Number of PCB Layers" on page 12 section.
- Added Figures 11 and 12.

Version 4.0

Information contained in *AN 114: Designing With High-Density BGA Packages for Altera Devices* version 4.0 supersedes information published in previous versions.

- Changed name of document to *Designing With High-Density BGA Packages for Altera Devices* from *Designing With FineLine BGA Packages for APEX, FLEX, ACEX, MAX 7000 & MAX 3000 Devices*.

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