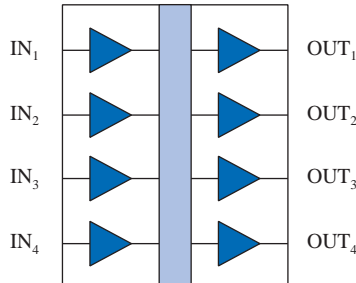
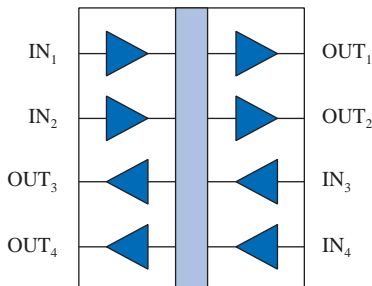


High Speed/High Temperature Four-Channel Digital Isolators

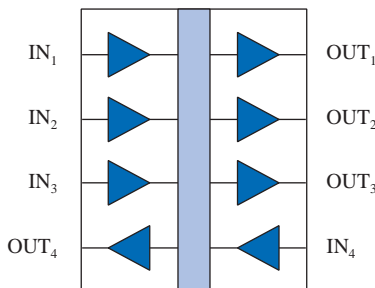
Functional Diagrams



IL715



IL716



IL717

Features

- +5 V/+3.3 V CMOS/TTL Compatible
- High Speed: 110 Mbps
- High Temperature: -40°C to $+125^{\circ}\text{C}$ (IL715T/IL716T/IL717T)
- 1.5 mA/Channel Typical Quiescent Current
- 100 ps Typical Pulse Jitter
- 2 ns Channel-to-Channel Skew
- 10 ns Typical Propagation Delay
- Low EMC Footprint
- 30 kV/ μs Typical Common Mode Transient Immunity
- 2500 V_{RMS} Isolation (1 min.)
- UL1577 and IEC 61010-2001 Approved
- 0.3" and 0.15" 16-pin SOIC Packages

Applications

- ADCs and DACs
- Digital Fieldbus
- RS-485 and RS-422
- Multiplexed Data Transmission
- Data Interfaces
- Board-to-Board Communication
- Digital Noise Reduction
- Operator Interface
- Ground Loop Elimination
- Peripheral Interfaces
- Parallel Bus
- Logic Level Shifting

Description

NVE's IL715, IL716, and IL717 four-channel high-speed digital isolators are CMOS devices manufactured with NVE's patented* IsoLoop[®] spintronic Giant Magnetoresistive (GMR) technology.

All transmit and receive channels operate at 110 Mbps over the full temperature and supply voltage range. The symmetric magnetic coupling barrier provides a typical propagation delay of only 10 ns and a pulse width distortion of 2 ns, achieving the best specifications of any isolator. Typical transient immunity of 30 kV/ μs is unsurpassed. Available in 0.15" SOIC packages, the four-channel devices provide the highest channel density available.

Typical transient immunity of 30 kV/ μs is unsurpassed. High channel density makes these devices ideal for isolating ADCs and DACs, parallel buses and peripheral interfaces.

The IL715, IL716, and IL717 are available in 0.3" and 0.15" 16-pin SOIC packages and performance is specified over the temperature range of -40°C to $+100^{\circ}\text{C}$ without derating. The IL715T, IL716T, and IL717T are specified over -40°C to $+125^{\circ}\text{C}$; the widest temperature range digital couplers available.

Absolute Maximum Ratings

Parameters	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Storage Temperature	T_s	-55		150	°C	
Ambient Operating Temperature ⁽¹⁾ IL715T, IL716T, and IL717T	T_A	-55		125 135	°C	
Supply Voltage	V_{DD1}, V_{DD2}	-0.5		7	V	
Input Voltage	V_i	-0.5		$V_{DD}+0.5$	V	
Output Voltage	V_o	-0.5		$V_{DD}+0.5$	V	
Output Current Drive	I_o			10	mA	
Lead Solder Temperature				260	°C	10 sec.
ESD			2		kV	HBM

Recommended Operating Conditions

Parameters	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Ambient Operating Temperature IL715, IL716, and IL717	T_A	-40		100	°C	
IL715T, IL716T, and IL717T	T_A	-40		125	°C	
Supply Voltage	V_{DD1}, V_{DD2}	3.0		5.5	V	
Logic High Input Voltage	V_{IH}	2.4		V_{DD}	V	
Logic Low Input Voltage	V_{IL}	0		0.8	V	
Input Signal Rise and Fall Times	t_{IR}, t_{IF}			1	µs	

Insulation Specifications

Parameters	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Creepage Distance						
0.15" SOIC		4.03			mm	
0.3" SOIC		8.08			mm	
Leakage Current ⁽⁵⁾			0.2		µA	240 V_{RMS} , 60 Hz
Barrier Impedance ⁽⁵⁾			$>10^{14} 3$		ΩpF	

Package Characteristics

Parameters	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Capacitance (Input–Output) ⁽⁵⁾	C_{I-O}		4		pF	f = 1 MHz
Thermal Resistance						
0.15" SOIC	θ_{JC}		41		°C/W	Thermocouple at center underside of package
0.3" SOIC	θ_{JC}		28		°C/W	
Package Power Dissipation	P_{PD}			150	mW	f = 1 MHz, $V_{DD} = 5 V$

Safety and Approvals

IEC61010-1

TUV Certificate Numbers: **N1502812, N1502812-101**

Classification as Reinforced Insulation

Model	Package	Pollution Degree	Material Group	Max. Working Voltage
IL715, IL716, and IL717	0.3" SOIC	II	III	300 V_{RMS}
IL715-3, IL716-3, and IL717-3	0.15" SOIC	II	III	150 V_{RMS}

UL 1577

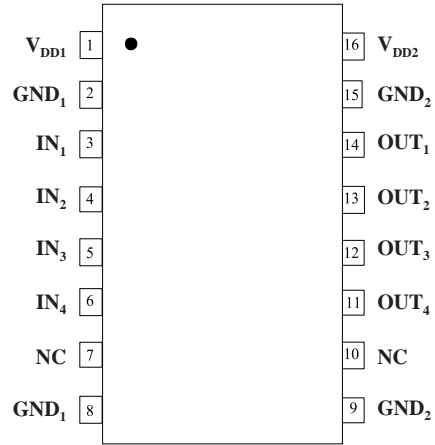
Component Recognition Program File Number: E207481
Rated 2500 V_{RMS} for 1 minute

Soldering Profile

Per JEDEC J-STD-020C, MSL=2

IL715 Pin Connections

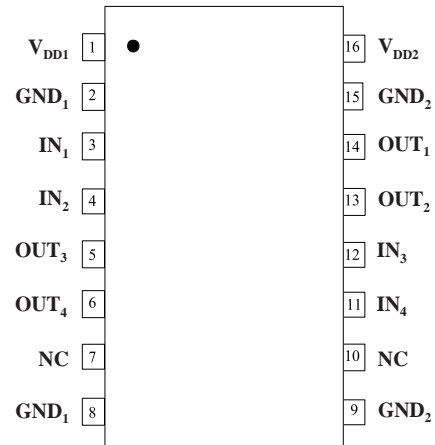
1	V _{DD1}	Supply voltage
2	GND ₁	Ground return for V _{DD1} *
3	IN ₁	Data in, channel 1
4	IN ₂	Data in, channel 2
5	IN ₃	Data in, channel 3
6	IN ₄	Data in, channel 4
7	NC	No connection
8	GND ₁	Ground return for V _{DD1} *
9	GND ₂	Ground return for V _{DD2} *
10	NC	No connection
11	OUT ₄	Data out, channel 4
12	OUT ₃	Data out, channel 3
13	OUT ₂	Data out, channel 2
14	OUT ₁	Data out, channel 1
15	GND ₂	Ground return for V _{DD2} *
16	V _{DD2}	Supply voltage



IL715

IL716 Pin Connections

1	V _{DD1}	Supply voltage
2	GND ₁	Ground Return for V _{DD1} *
3	IN ₁	Data in, channel 1
4	IN ₂	Data in, channel 2
5	OUT ₃	Data out, channel 3
6	OUT ₄	Data out, channel 4
7	NC	No connection
8	GND ₁	Ground Return for V _{DD1} *
9	GND ₂	Ground Return for V _{DD2} *
10	NC	No connection
11	IN ₄	Data in, channel 4
12	IN ₃	Data in, channel 3
13	OUT ₂	Data out, channel 2
14	OUT ₁	Data out, channel 1
15	GND ₂	Ground Return for V _{DD2} *
16	V _{DD2}	Supply voltage

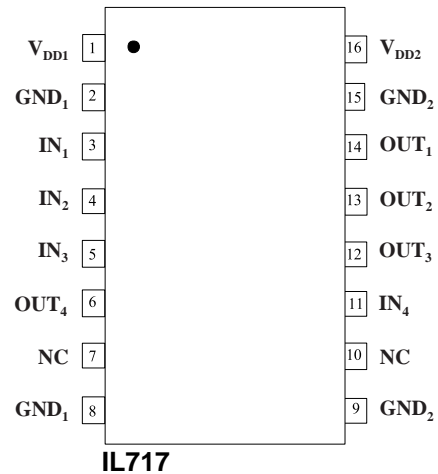


IL716

*NOTE: Pins 2 and 8 are internally connected, as are pins 9 and 15.

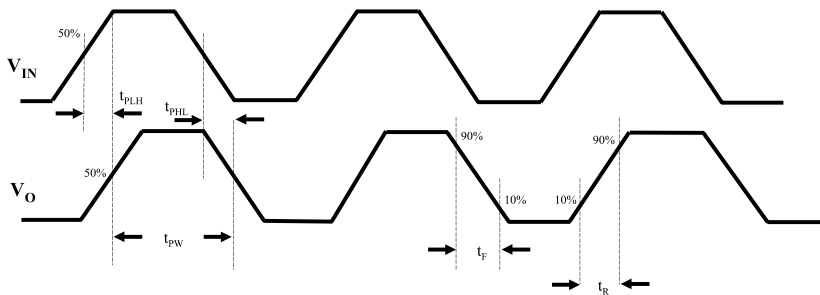
IL717 Pin Connections

1	V _{DD1}	Supply voltage
2	GND ₁	Ground return for V _{DD1} *
3	IN ₁	Data in, channel 1
4	IN ₂	Data in, channel 2
5	IN ₃	Data in, channel 3
6	OUT ₄	Data out, channel 4
7	NC	No connection
8	GND ₁	Ground return for V _{DD1} *
9	GND ₂	Ground return for V _{DD2} *
10	NC	No connection
11	IN ₄	Data in, channel 4
12	OUT ₃	Data out, channel 3
13	OUT ₂	Data out, channel 2
14	OUT ₁	Data out, channel 1
15	GND ₂	Ground return for V _{DD2} *
16	V _{DD2}	Supply voltage



*NOTE: Pins 2 and 8 are internally connected, as are pins 9 and 15.

Timing Diagram



Legend

t _{PLH}	Propagation Delay, Low to High
t _{PHL}	Propagation Delay, High to Low
t _{PW}	Minimum Pulse Width
t _R	Rise Time
t _F	Fall Time

3.3 Volt Electrical Specifications

Electrical specifications are T_{min} to T_{max} unless otherwise stated.

Parameters	Symbol	Min.	Typ.	Max.	Units	Test Conditions
DC Specifications						
Input Quiescent Supply Current						
IL715	I_{DD1}		16	20	μA	
IL716			3	4	mA	
IL717			1.5	2	mA	
Output Quiescent Supply Current						
IL715	I_{DD2}		6	8	mA	
IL716			3	4	mA	
IL717			4.5	6	mA	
Logic Input Current	I_I	-10		10	μA	
Logic High Output Voltage	V_{OH}	$V_{DD} - 0.1$	V_{DD}		V	$I_O = -20 \mu\text{A}, V_I = V_{IH}$
		$0.8 \times V_{DD}$	$0.9 \times V_{DD}$			$I_O = -4 \text{mA}, V_I = V_{IH}$
Logic Low Output Voltage	V_{OL}		0	0.1	V	$I_O = 20 \mu\text{A}, V_I = V_{IL}$
			0.5	0.8		$I_O = 4 \text{mA}, V_I = V_{IL}$
Switching Specifications						
Maximum Data Rate		100	110		Mbps	$C_L = 15 \text{pF}$
Pulse Width ⁽⁷⁾	PW	10			ns	50% Points, V_O
Propagation Delay Input to Output (High to Low)	t_{PHL}		12	18	ns	$C_L = 15 \text{pF}$
Propagation Delay Input to Output (Low to High)	t_{PLH}		12	18	ns	$C_L = 15 \text{pF}$
Pulse Width Distortion ⁽²⁾	PWD		2	3	ns	$C_L = 15 \text{pF}$
Propagation Delay Skew ⁽³⁾	t_{PSK}		4	6	ns	$C_L = 15 \text{pF}$
Output Rise Time (10%–90%)	t_R		2	4	ns	$C_L = 15 \text{pF}$
Output Fall Time (10%–90%)	t_F		2	4	ns	$C_L = 15 \text{pF}$
Common Mode Transient Immunity (Output Logic High or Logic Low) ⁽⁴⁾	$ CM_H , CM_L $	20	30		$\text{kV}/\mu\text{s}$	$V_{CM} = 300 \text{V}$
Channel-to-Channel Skew	t_{CSK}		2	3	ns	$C_L = 15 \text{pF}$
Dynamic Power Consumption ⁽⁶⁾			140	240	$\mu\text{A}/\text{MHz}$	per channel
Magnetic Field Immunity⁽⁸⁾ ($V_{DD2} = 3\text{V}, 3\text{V} < V_{DD1} < 5.5\text{V}$)						
Power Frequency Magnetic Immunity	H_{PF}	1000	1500		A/m	50Hz/60Hz
Pulse Magnetic Field Immunity	H_{PM}	1800	2000		A/m	$t_p = 8\mu\text{s}$
Damped Oscillatory Magnetic Field	H_{OSC}	1800	2000		A/m	0.1Hz – 1MHz
Cross-axis Immunity Multiplier ⁽⁹⁾	K_X		2.5			

5 Volt Electrical Specifications

Electrical specifications are T_{min} to T_{max} unless otherwise stated.

Parameters	Symbol	Min.	Typ.	Max.	Units	Test Conditions
DC Specifications						
Input Quiescent Supply Current						
IL715	I_{DD1}		24	30	μA	
IL716			4	6	mA	
IL717			2	3	mA	
Output Quiescent Supply Current						
IL715	I_{DD2}		8	12	mA	
IL716			4	6	mA	
IL717			6	9	mA	
Logic Input Current	I_I	-10		10	μA	
Logic High Output Voltage	V_{OH}	$V_{DD} - 0.1$	V_{DD}		V	$I_O = -20 \mu\text{A}, V_I = V_{IH}$
		$0.8 \times V_{DD}$	$0.9 \times V_{DD}$			$I_O = -4 \text{mA}, V_I = V_{IH}$
Logic Low Output Voltage	V_{OL}		0	0.1	V	$I_O = 20 \mu\text{A}, V_I = V_{IL}$
			0.5	0.8		$I_O = 4 \text{mA}, V_I = V_{IL}$
Switching Specifications						
Maximum Data Rate		100	110		Mbps	$C_L = 15 \text{pF}$
Pulse Width ⁽⁷⁾	PW	10			ns	50% Points, V_o
Propagation Delay Input to Output (High to Low)	t_{PHL}		10	15	ns	$C_L = 15 \text{pF}$
Propagation Delay Input to Output (Low to High)	t_{PLH}		10	15	ns	$C_L = 15 \text{pF}$
Pulse Width Distortion ⁽²⁾	PWD		2	3		$C_L = 15 \text{pF}$
Pulse Jitter ⁽¹⁰⁾	t_j		100		ps	$C_L = 15 \text{pF}$
Propagation Delay Skew ⁽³⁾	t_{PSK}		4	6	ns	$C_L = 15 \text{pF}$
Output Rise Time (10%–90%)	t_R		1	3	ns	$C_L = 15 \text{pF}$
Output Fall Time (10%–90%)	t_F		1	3	ns	$C_L = 15 \text{pF}$
Common Mode Transient Immunity (Output Logic High or Logic Low) ⁽⁴⁾	$ CM_H , CM_L $	20	30		$\text{kV}/\mu\text{s}$	$V_{cm} = 300 \text{V}$
Channel-to-Channel Skew	t_{CSK}		2	3	ns	$C_L = 15 \text{pF}$
Dynamic Power Consumption ⁽⁶⁾			200	340	$\mu\text{A}/\text{MHz}$	per channel
Magnetic Field Immunity⁽⁸⁾ ($V_{DD2} = 5\text{V}, 3\text{V} < V_{DD1} < 5.5\text{V}$)						
Power Frequency Magnetic Immunity	H_{PF}	2800	3500		A/m	50Hz/60Hz
Pulse Magnetic Field Immunity	H_{PM}	4000	4500		A/m	$t_p = 8 \mu\text{s}$
Damped Oscillatory Magnetic Field	H_{OSC}	4000	4500		A/m	0.1Hz – 1MHz
Cross-axis Immunity Multiplier ⁽⁹⁾	K_X		2.5			

Notes (apply to both 3.3 V and 5 V specifications):

- Absolute maximum ambient operating temperature means the device will not be damaged if operated under these conditions. It does not guarantee performance.
- PWD is defined as $|t_{PHL} - t_{PLH}|$. %PWD is equal to PWD divided by pulse width.
- t_{PSK} is the magnitude of the worst-case difference in t_{PHL} and/or t_{PLH} between devices at 25°C.
- CM_H is the maximum common mode voltage slew rate that can be sustained while maintaining $V_o > 0.8 V_{DD2}$. CM_L is the maximum common mode input voltage that can be sustained while maintaining $V_o < 0.8 \text{V}$. The common mode voltage slew rates apply to both rising and falling common mode voltage edges.
- Device is considered a two terminal device: pins 1–8 shorted and pins 9–16 shorted.
- Dynamic power consumption is calculated per channel and is supplied by the channel's input side power supply.
- Minimum pulse width is the minimum value at which specified PWD is guaranteed.
- The relevant test and measurement methods are given in the Electromagnetic Compatibility section on p. 7.
- External magnetic field immunity is improved by this factor if the field direction is “end-to-end” rather than to “pin-to-pin” (see diagram on p. 7).
- 66,535-bit pseudo-random binary signal (PRBS) NRZ bit pattern with no more than five consecutive 1s or 0s; 800 ps transition time.

Application Information

Electrostatic Discharge Sensitivity

This product has been tested for electrostatic sensitivity to the limits stated in the specifications. However, NVE recommends that all integrated circuits be handled with appropriate care to avoid damage. Damage caused by inappropriate handling or storage could range from performance degradation to complete failure.

Electromagnetic Compatibility

IsoLoop Isolators have the lowest EMC footprint of any isolation technology. IsoLoop Isolators' Wheatstone bridge configuration and differential magnetic field signaling ensure excellent EMC performance against all relevant standards.

These isolators are fully compliant with generic EMC standards EN50081, EN50082-1 and the umbrella line-voltage standard for Information Technology Equipment (ITE) EN61000. NVE has completed compliance tests in the categories below:

EN50081-1

Residential, Commercial & Light Industrial
Methods EN55022, EN55014

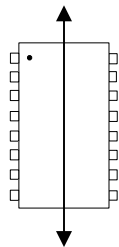
EN50082-2: Industrial Environment

Methods EN61000-4-2 (ESD), EN61000-4-3 (Electromagnetic Field Immunity), EN61000-4-4 (Electrical Transient Immunity), EN61000-4-6 (RFI Immunity), EN61000-4-8 (Power Frequency Magnetic Field Immunity), EN61000-4-9 (Pulsed Magnetic Field), EN61000-4-10 (Damped Oscillatory Magnetic Field)

ENV50204

Radiated Field from Digital Telephones (Immunity Test)

Immunity to external magnetic fields is even higher if the field direction is "end-to-end" rather than to "pin-to-pin" as shown in the diagram below:



Cross-axis Field Direction

Dynamic Power Consumption

IsoLoop Isolators achieve their low power consumption from the way they transmit data across the isolation barrier. By detecting the edge transitions of the input logic signal and converting these to narrow current pulses, a magnetic field is created around the GMR Wheatstone bridge. Depending on the direction of the magnetic field, the bridge causes the output comparator to switch following the input logic signal. Since the current pulses are narrow, about 2.5 ns, the power consumption is independent of mark-to-space ratio and solely dependent on frequency. This has obvious advantages over optocouplers, which have power consumption heavily dependent on mark-to-space ratio.

Power Supply Decoupling

Both power supplies to these devices should be decoupled with low ESR 47 nF ceramic capacitors. Ground planes for both GND₁ and GND₂ are highly recommended for data rates above 10 Mbps. Capacitors must be located as close as possible to the V_{DD} pins.

Signal Status on Start-up and Shut Down

To minimize power dissipation, input signals are differentiated and then latched on the output side of the isolation barrier to reconstruct the signal. This could result in an ambiguous output state depending on power up, shutdown and power loss sequencing. Therefore, the designer should consider including an initialization signal in the start-up circuit. Initialization consists of toggling the input either high then low, or low then high.

Data Transmission Rates

The reliability of a transmission system is directly related to the accuracy and quality of the transmitted digital information. For a digital system, those parameters which determine the limits of the data transmission are pulse width distortion and propagation delay skew.

Propagation delay is the time taken for the signal to travel through the device. This is usually different when sending a low-to-high than when sending a high-to-low signal. This difference, or error, is called pulse width distortion (PWD) and is usually in nanoseconds. It may also be expressed as a percentage:

$$\text{PWD}\% = \frac{\text{Maximum Pulse Width Distortion (ns)}}{\text{Signal Pulse Width (ns)}} \times 100\%$$

For example, with data rates of 12.5 Mbps:

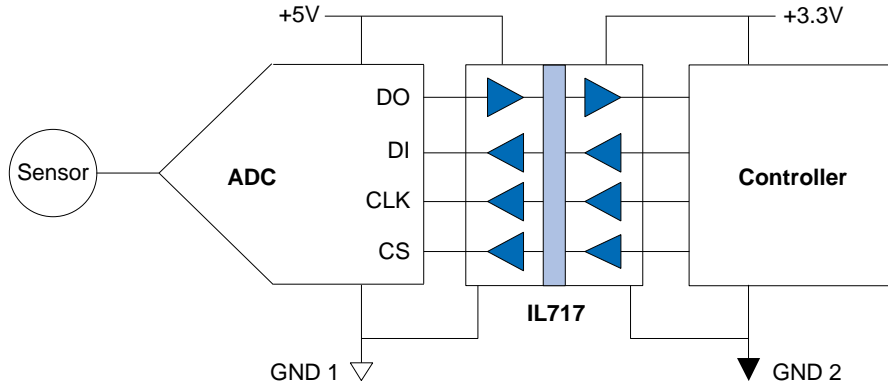
$$\text{PWD}\% = \frac{3 \text{ ns}}{80 \text{ ns}} \times 100\% = 3.75\%$$

This figure is almost **three times** better than any available optocoupler with the same temperature range, and **two times** better than any optocoupler regardless of published temperature range. IsoLoop isolators exceed the 10% maximum PWD recommended by PROFIBUS, and will run to nearly 35 Mb within the 10% limit.

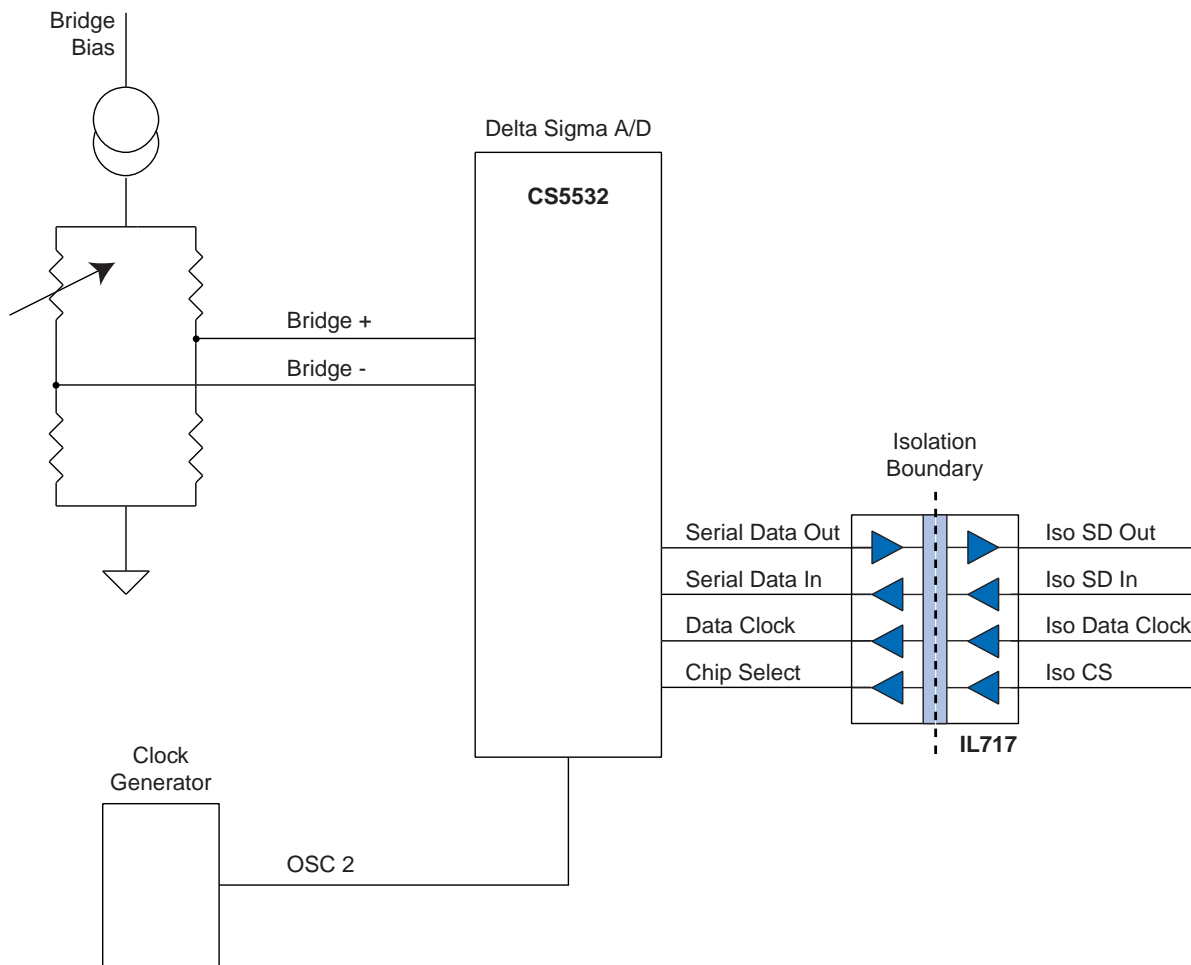
Propagation delay skew is the signal propagation difference between two or more channels. This becomes significant in clocked systems because it is undesirable for the clock pulse to arrive before the data has settled. Short propagation delay skew is therefore especially critical in high data rate parallel systems for establishing and maintaining accuracy and repeatability. Worst-case channel-to-channel skew in an IL700 Isolator is only 3 ns, which is **ten times** better than any optocoupler. IL700 Isolators have a maximum propagation delay skew of 6 ns, which is **five times** better than any optocoupler.

Application Diagrams

Isolated Logic Level Shifters



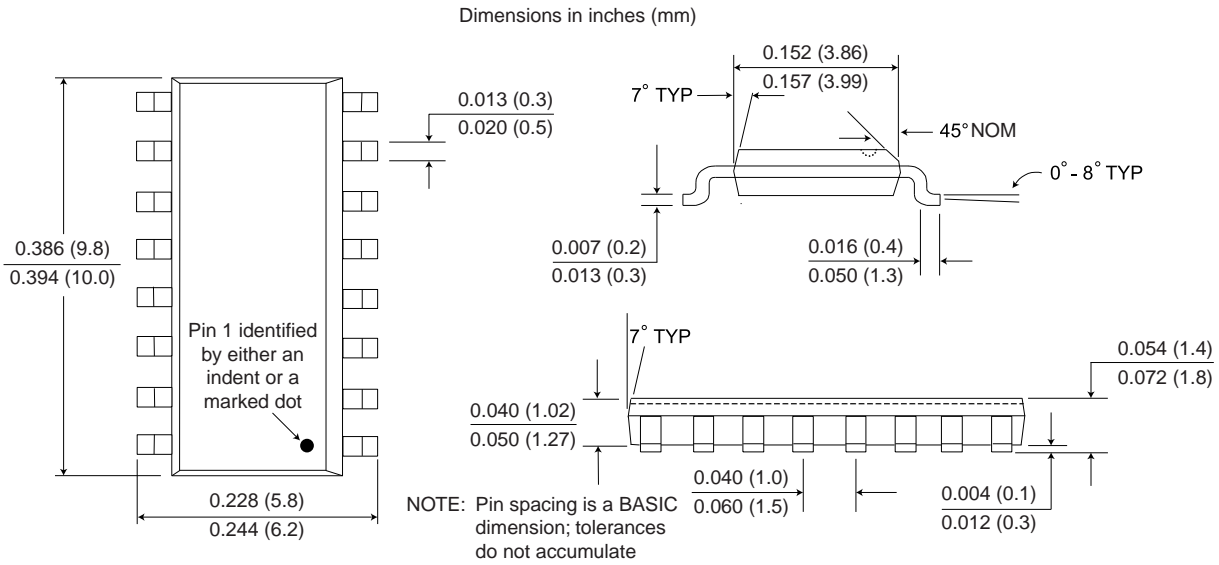
Single-Channel Isolated Delta-Sigma A/D Converter



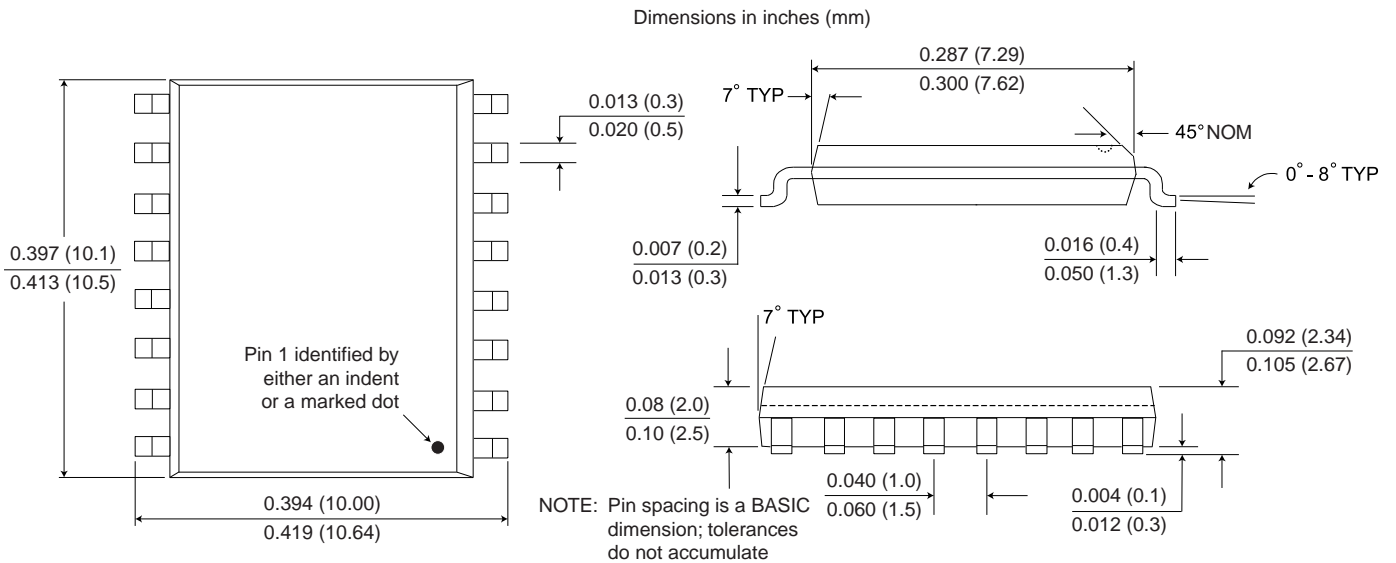
This circuit illustrates a typical single-channel delta-sigma ADC. The A/D is located on the bridge with no signal conditioning electronics between the bridge sensor and the ADC. In this case, the IL717 is the best choice for isolation. It isolates the control bus from the microcontroller. The system clock is located on the isolated side of the system.

Package Drawings, Dimensions and Specifications

0.15" SOIC Package

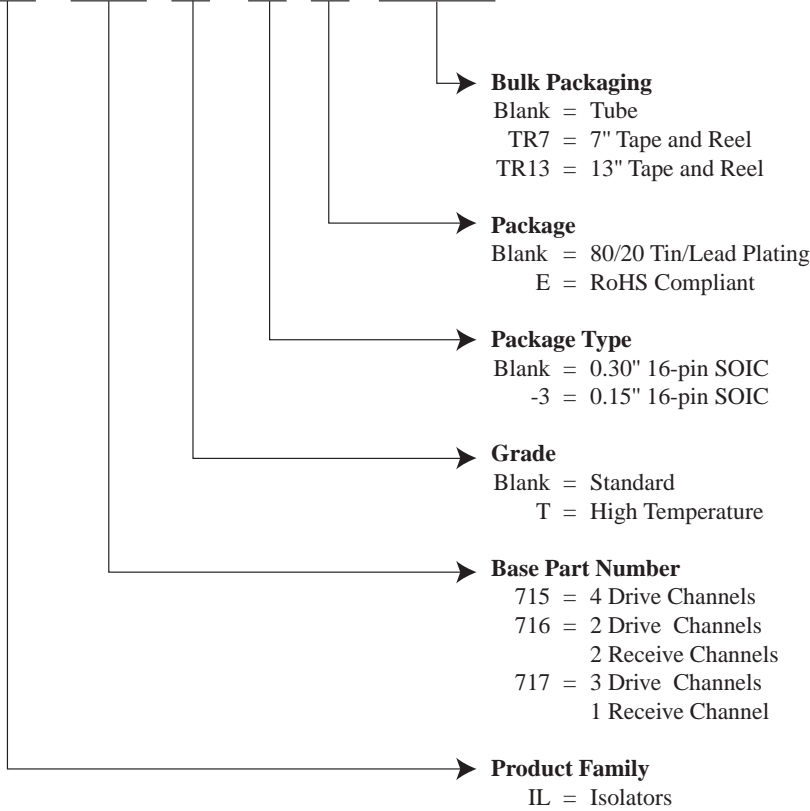


0.3" SOIC Package



Ordering Information and Valid Part Numbers

IL 716 T - 3 E TR13



Valid Part Numbers

IL715	IL716	IL717
IL715E	IL716E	IL717E
IL715-3	IL716-3	IL717-3
IL715-3E	IL716-3E	IL717-3E
IL715T	IL716T	IL717T
IL715TE	IL716TE	IL717TE
IL715T-3	IL716T-3	IL717T-3
IL715T-3E	IL716T-3E	IL717T-3E

All IL715, IL716, and IL717 part types are available on tape and reel.



ISB-DS-001-IL715/6/7-U
March 2012

Changes

- Tightened typical output quiescent supply spec. to 1.5 mA/channel at 3.3V.

ISB-DS-001-IL715/6/7-T

Changes

- Updates to terms and conditions.

ISB-DS-001-IL715/6/7-S

Changes

- Added clarification of internal ground connections (pp. 3-4).

ISB-DS-001-IL715/6/7-R

Changes

- Added typical jitter specification at 5V.

ISB-DS-001-IL715/6/7-Q

Changes

- Added EMC details.

ISB-DS-001-IL715/6/7-P

Changes

- Added magnetic field immunity and electromagnetic compatibility specifications.
- Added notes on package drawings that pin-spacing tolerances are non-accumulating.

ISB-DS-001-IL715/6/7-O

Changes

- Changed ordering information to reflect that devices are now fully RoHS compliant with no exemptions.

ISB-DS-001-IL715/6/7-N

Changes

- Eliminated soldering profile chart

ISB-DS-001-IL715/6/7-M

Changes

- Package drawings updated

ISB-DS-001-IL715/6/7-L

Changes

- T-Grades added
- Package drawings updated
- Order information updated

ISB-DS-001-IL715/6/7-K

Changes

- Update UL and IEC approvals
- Package characteristics added

Datasheet Limitations

The information and data provided in datasheets shall define the specification of the product as agreed between NVE and its customer, unless NVE and customer have explicitly agreed otherwise in writing. All specifications are based on NVE test protocols. In no event however, shall an agreement be valid in which the NVE product is deemed to offer functions and qualities beyond those described in the datasheet.

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ISB-DS-001-IL715/6/7-U

March 2012