# Micropower, Low Noise Precision Voltage References with Shutdown

25-05967

# ADR391/ADR392/ADR395

## FEATURES

- Compact 5-lead TSOT package
- Low temperature coefficient
  - B grade: 9 ppm/°C
  - A grade: 25 ppm/°C
- Initial accuracy
  - B grade: ±4 mV maximum (ADR391)
  - A grade: ±6 mV maximum
- Ultralow output noise: 5 µV p-p (0.1 Hz to 10 Hz)
- Low dropout: 300 mV
- Low supply current
  - 3 µA maximum in shutdown
  - 140 µA maximum in operation
- No external capacitor required
- Output current: 5 mA
- Automotive grade available
- Wide temperature range: −40°C to +125°C

## APPLICATIONS

- Battery-powered instrumentation
- Portable medical instrumentation
- Data acquisition systems
- Industrial process controls
- Automotive

## PIN CONFIGURATION

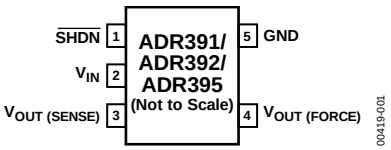


*Figure 1. 5-Lead TSOT (UJ Suffix)*

**Table 1.**

| Model | Output Voltage ($V_O$) | Temperature Coefficient (ppm/°C) | Accuracy (mV) |
|---|---|---|---|
| ADR391B | 2.5 | 9 | ±4 |
| ADR391A | 2.5 | 25 | ±6 |
| ADR392B | 4.096 | 9 | ±5 |
| ADR392A | 4.096 | 25 | ±6 |
| ADR395B | 5.0 | 9 | ±5 |
| ADR395A | 5.0 | 25 | ±6 |

## GENERAL DESCRIPTION

The ADR391/ADR392/ADR395 are precision 2.048 V, 2.5 V, 4.096 V, and 5 V band gap voltage references, respectively, featuring low power and high precision in a tiny footprint. Using patented temperature drift curvature correction techniques from Analog Devices, Inc., the ADR39x references achieve a low 9 ppm/°C of temperature drift in the TSOT package.

The ADR39x family of micropower, low dropout voltage references provides a stable output voltage from a minimum supply of 300 mV above the output. Their advanced design eliminates the need for external capacitors, which further reduces board space and system cost. The combination of low power operation, small size, and ease of use makes the ADR39x precision voltage references ideally suited for battery-operated applications.

Rev. H


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# SPECIFICATIONS

## ADR391 ELECTRICAL CHARACTERISTICS

$V_{IN}$ = 2.8 V to 15 V, $T_A$ = 25°C, unless otherwise noted.

**Table 2.**

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| OUTPUT VOLTAGE | $V_O$ | A grade | 2.494 | 2.5 | 2.506 | V |
| | | B grade | 2.496 | 2.5 | 2.504 | V |
| INITIAL ACCURACY | $V_{OERR}$ | A grade | | | 6 | mV |
| | | A grade | | | 0.24 | % |
| | | B grade | | | 4 | mV |
| | | B grade | | | 0.16 | % |
| TEMPERATURE COEFFICIENT | $TCV_O$ | A grade, −40°C < $T_A$ < +125°C | | | 25 | ppm/°C |
| | | B grade, −40°C < $T_A$ < +125°C | | | 9 | ppm/°C |
| SUPPLY VOLTAGE HEADROOM | $V_{IN} - V_O$ | | 300 | | | mV |
| LINE REGULATION | $\Delta V_O/\Delta V_{IN}$ | $V_{IN}$ = 2.8 V to 15 V, −40°C < $T_A$ < +125°C | | 10 | 25 | ppm/V |
| LOAD REGULATION | $\Delta V_O/\Delta I_{LOAD}$ | $I_{LOAD}$ = 0 mA to 5 mA, −40°C < $T_A$ < +85°C, $V_{IN}$ = 3 V | | | 60 | ppm/mA |
| | | $I_{LOAD}$ = 0 mA to 5 mA, −40°C < $T_A$ < +125°C, $V_{IN}$ = 3 V | | | 140 | ppm/mA |
| QUIESCENT CURRENT | $I_{IN}$ | No load | | | 120 | µA |
| | | −40°C < $T_A$ < +125°C | | | 140 | µA |
| VOLTAGE NOISE | $e_{n\ p-p}$ | 0.1 Hz to 10 Hz | | 5 | | µV p-p |
| TURN-ON SETTLING TIME | $t_R$ | | | 20 | | µs |
| LONG-TERM STABILITY[1] | $\Delta V_O$ | 1000 hours | | 50 | | ppm |
| OUTPUT VOLTAGE HYSTERESIS | $\Delta V_{O\_HYS}$ | | | 100 | | ppm |
| RIPPLE REJECTION RATIO | RRR | $f_{IN}$ = 60 Hz | | −80 | | dB |
| SHORT CIRCUIT TO GND | $I_{SC}$ | $V_{IN}$ = 5 V | | 25 | | mA |
| | | $V_{IN}$ = 15 V | | 30 | | mA |
| SHUTDOWN PIN | | | | | | |
| Shutdown Supply Current | $I_{SHDN}$ | | | | 3 | µA |
| Shutdown Logic Input Current | $I_{LOGIC}$ | | | | 500 | nA |
| Shutdown Logic Low | $V_{INL}$ | | | | 0.8 | V |
| Shutdown Logic High | $V_{INH}$ | | 2.4 | | | V |

[1] The long-term stability specification is noncumulative. The drift of subsequent 1000 hour periods is significantly lower than in the first 1000 hour period.

## ADR392 ELECTRICAL CHARACTERISTICS

$V_{IN}$ = 4.3 V to 15 V, $T_A$ = 25°C, unless otherwise noted.

**Table 3.**

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| OUTPUT VOLTAGE | $V_O$ | A grade | 4.090 | 4.096 | 4.102 | V |
| | | B grade | 4.091 | 4.096 | 4.101 | V |
| INITIAL ACCURACY | $V_{OERR}$ | A grade | | | 6 | mV |
| | | A grade | | | 0.15 | % |
| | | B grade | | | 5 | mV |
| | | B grade | | | 0.12 | % |
| TEMPERATURE COEFFICIENT | $TCV_O$ | A grade, −40°C < $T_A$ < +125°C | | | 25 | ppm/°C |
| | | B grade, −40°C < $T_A$ < +125°C | | | 9 | ppm/°C |
| SUPPLY VOLTAGE HEADROOM | $V_{IN} - V_O$ | | 300 | | | mV |
| LINE REGULATION | $\Delta V_O/\Delta V_{IN}$ | $V_{IN}$ = 4.3 V to 15 V, −40°C < $T_A$ < +125°C | | 10 | 25 | ppm/V |
| LOAD REGULATION | $\Delta V_O/\Delta I_{LOAD}$ | $I_{LOAD}$ = 0 mA to 5 mA, −40°C < $T_A$ < +125°C, $V_{IN}$ = 5 V | | | 140 | ppm/mA |
| QUIESCENT CURRENT | $I_{IN}$ | No load | | | 120 | µA |
| | | −40°C < $T_A$ < +125°C | | | 140 | µA |
| VOLTAGE NOISE | $e_{n\ p-p}$ | 0.1 Hz to 10 Hz | | 7 | | µV p-p |
| TURN-ON SETTLING TIME | $t_R$ | | | 20 | | µs |
| LONG-TERM STABILITY[1] | $\Delta V_O$ | 1000 hours | | 50 | | ppm |
| OUTPUT VOLTAGE HYSTERESIS | $\Delta V_{O\_HYS}$ | | | 100 | | ppm |
| RIPPLE REJECTION RATIO | RRR | $f_{IN}$ = 60 Hz | | −80 | | dB |
| SHORT CIRCUIT TO GND | $I_{SC}$ | $V_{IN}$ = 5 V | | 25 | | mA |
| | | $V_{IN}$ = 15 V | | 30 | | mA |
| SHUTDOWN PIN | | | | | | |
| Shutdown Supply Current | $I_{SHDN}$ | | | | 3 | µA |
| Shutdown Logic Input Current | $I_{LOGIC}$ | | | | 500 | nA |
| Shutdown Logic Low | $V_{INL}$ | | | | 0.8 | V |
| Shutdown Logic High | $V_{INH}$ | | 2.4 | | | V |

[1] The long-term stability specification is noncumulative. The drift of subsequent 1000 hour periods is significantly lower than in the first 1000 hour period.

## ADR395 ELECTRICAL CHARACTERISTICS

$V_{IN}$ = 5.3 V to 15 V, $T_A$ = 25°C, unless otherwise noted.

**Table 4.**

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| OUTPUT VOLTAGE | $V_O$ | A grade | 4.994 | 5.000 | 5.006 | V |
| | | B grade | 4.995 | 5.000 | 5.005 | V |
| INITIAL ACCURACY | $V_{OERR}$ | A grade | | | 6 | mV |
| | | A grade | | | 0.12 | % |
| | | B grade | | | 5 | mV |
| | | B grade | | | 0.10 | % |
| TEMPERATURE COEFFICIENT | $TCV_O$ | A grade, −40°C < $T_A$ < +125°C | | | 25 | ppm/°C |
| | | B grade, −40°C < $T_A$ < +125°C | | | 9 | ppm/°C |
| SUPPLY VOLTAGE HEADROOM | $V_{IN} - V_O$ | | 300 | | | mV |
| LINE REGULATION | $\Delta V_O/\Delta V_{IN}$ | $V_{IN}$ = 4.3 V to 15 V, −40°C < $T_A$ < +125°C | | 10 | 25 | ppm/V |
| LOAD REGULATION | $\Delta V_O/\Delta I_{LOAD}$ | $I_{LOAD}$ = 0 mA to 5 mA, −40°C < $T_A$ < +125°C, $V_{IN}$ = 6 V | | | 140 | ppm/mA |
| QUIESCENT CURRENT | $I_{IN}$ | No load | | | 120 | µA |
| | | −40°C < $T_A$ < +125°C | | | 140 | µA |
| VOLTAGE NOISE | $e_{n\ p\text{-}p}$ | 0.1 Hz to 10 Hz | | 8 | | µV p-p |
| TURN-ON SETTLING TIME | $t_R$ | | | 20 | | µs |
| LONG-TERM STABILITY[1] | $\Delta V_O$ | 1000 hours | | 50 | | ppm |
| OUTPUT VOLTAGE HYSTERESIS | $\Delta V_{O\_HYS}$ | | | 100 | | ppm |
| RIPPLE REJECTION RATIO | RRR | $f_{IN}$ = 60 Hz | | −80 | | dB |
| SHORT CIRCUIT TO GND | $I_{SC}$ | $V_{IN}$ = 5 V | | 25 | | mA |
| | | $V_{IN}$ = 15 V | | 30 | | mA |
| SHUTDOWN PIN | | | | | | |
| Shutdown Supply Current | $I_{SHDN}$ | | | | 3 | µA |
| Shutdown Logic Input Current | $I_{LOGIC}$ | | | | 500 | nA |
| Shutdown Logic Low | $V_{INL}$ | | | | 0.8 | V |
| Shutdown Logic High | $V_{INH}$ | | 2.4 | | | V |

[1] The long-term stability specification is noncumulative. The drift of subsequent 1000 hour periods is significantly lower than in the first 1000 hour period.

# ABSOLUTE MAXIMUM RATINGS

At 25°C, unless otherwise noted.

**Table 5.**

| Parameter | Rating |
|---|---|
| Supply Voltage | 18 V |
| Output Short-Circuit Duration to GND | See derating curves |
| Storage Temperature Range | −65°C to +125°C |
| Operating Temperature Range | −40°C to +125°C |
| Junction Temperature Range | −65°C to +125°C |
| Lead Temperature (Soldering, 60 sec) | 300°C |

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## THERMAL RESISTANCE

$\theta_{JA}$ is specified for the worst-case conditions, that is, for a device soldered in a circuit board for surface-mount packages.

**Table 6.**

| Package Type | $\theta_{JA}$ | $\theta_{JC}$ | Unit |
|---|---|---|---|
| TSOT (UJ-5) | 230 | 146 | °C/W |

## ESD CAUTION

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# TYPICAL PERFORMANCE CHARACTERISTICS

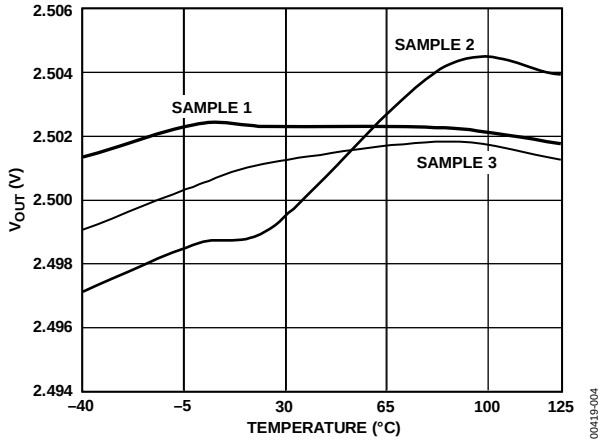



Figure 2. ADR391 Output Voltage ($V_{OUT}$) vs. Temperature

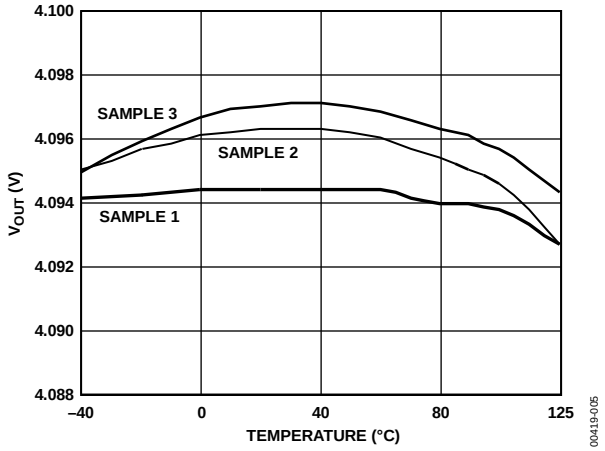



Figure 3. ADR392 Output Voltage ($V_{OUT}$) vs. Temperature

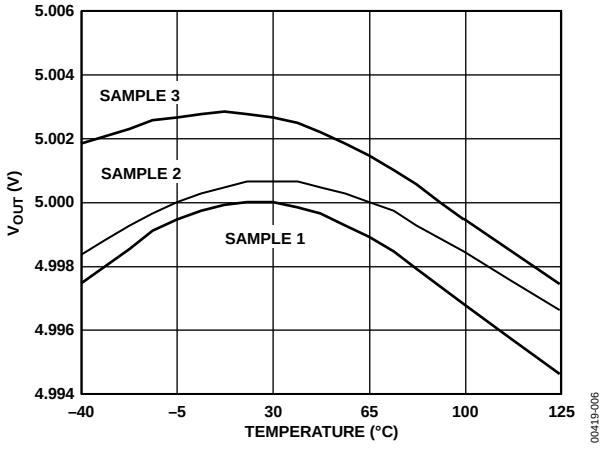



Figure 4. ADR395 Output Voltage ($V_{OUT}$) vs. Temperature

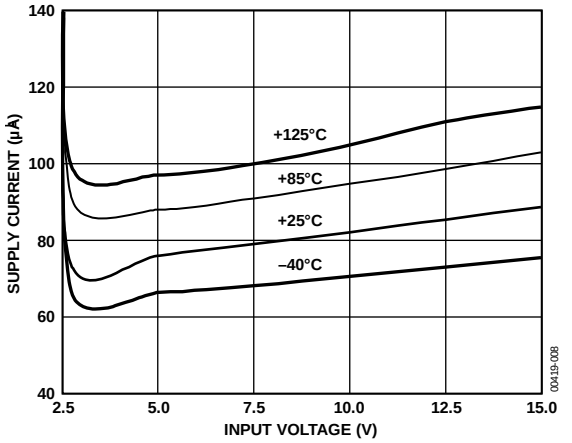



Figure 5. ADR391 Supply Current vs. Input Voltage

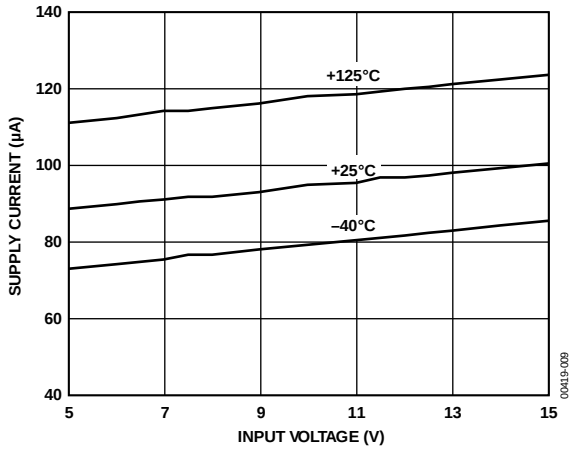



Figure 6. ADR392 Supply Current vs. Input Voltage

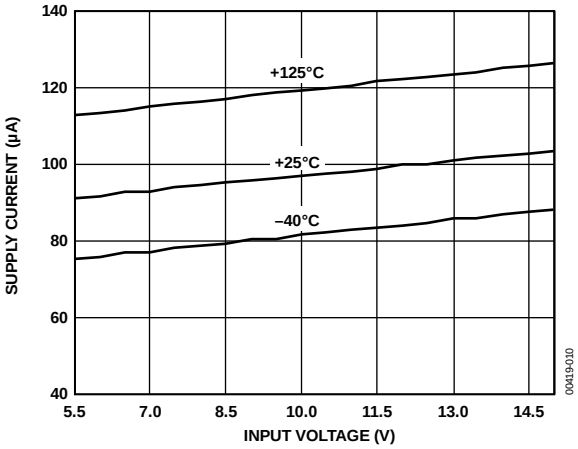



Figure 7. ADR395 Supply Current vs. Input Voltage

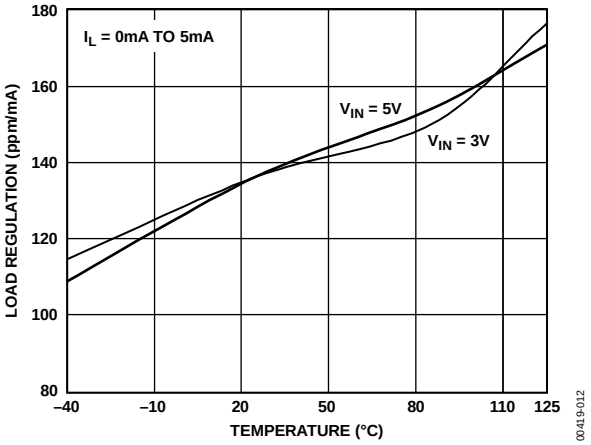



Figure 8. ADR391 Load Regulation vs. Temperature

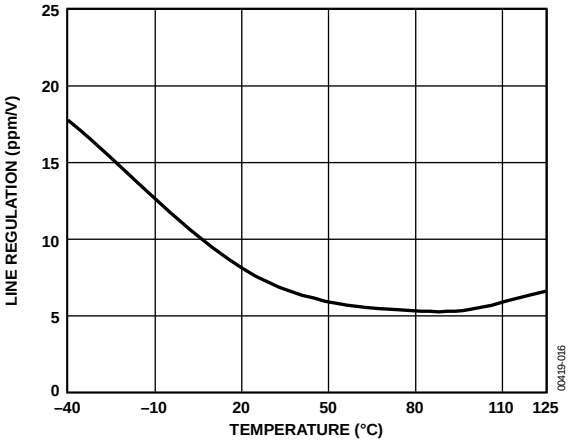



Figure 11. ADR391 Line Regulation vs. Temperature

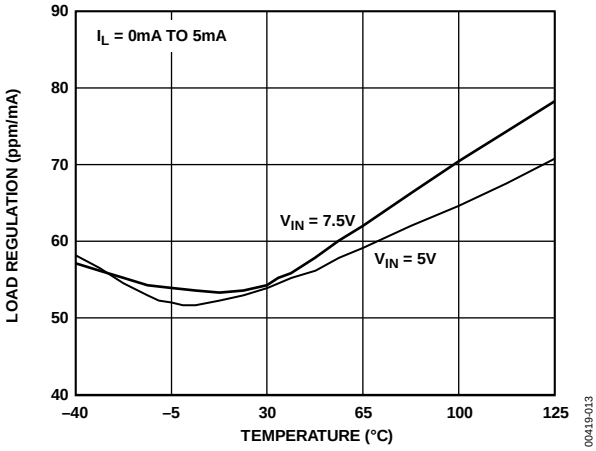



Figure 9. ADR392 Load Regulation vs. Temperature

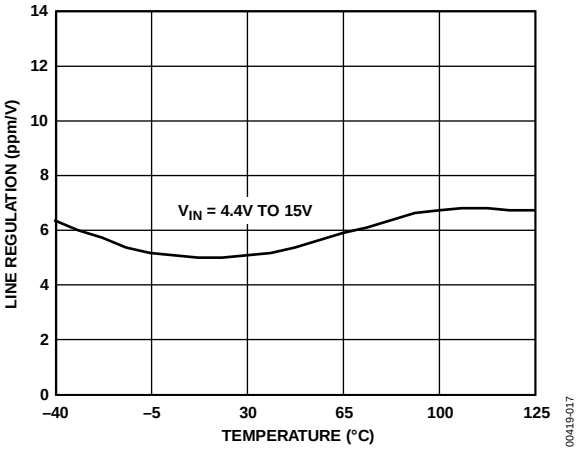



Figure 12. ADR392 Line Regulation vs. Temperature

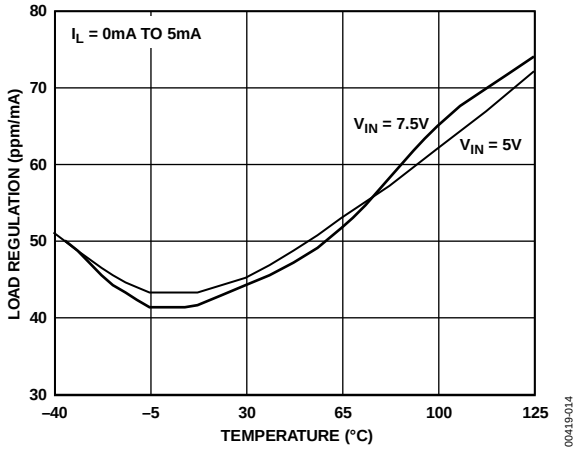



Figure 10. ADR395 Load Regulation vs. Temperature

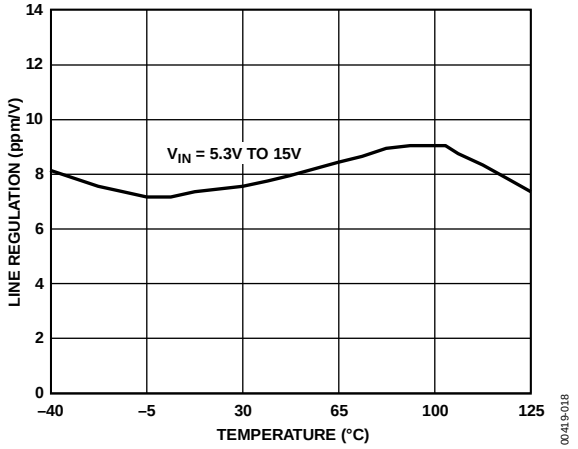



Figure 13. ADR395 Line Regulation vs. Temperature

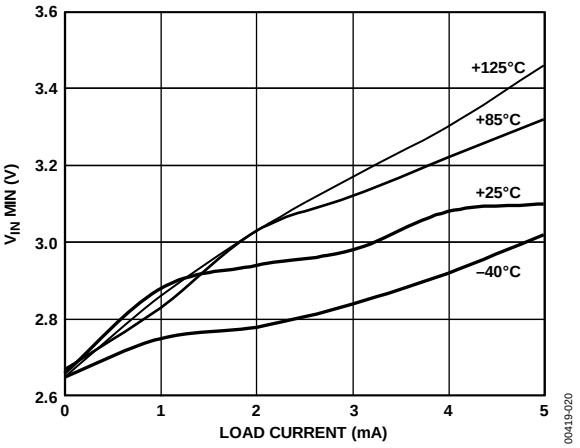



Figure 14. ADR391 Minimum Input Voltage ($V_{IN}$) vs. Load Current

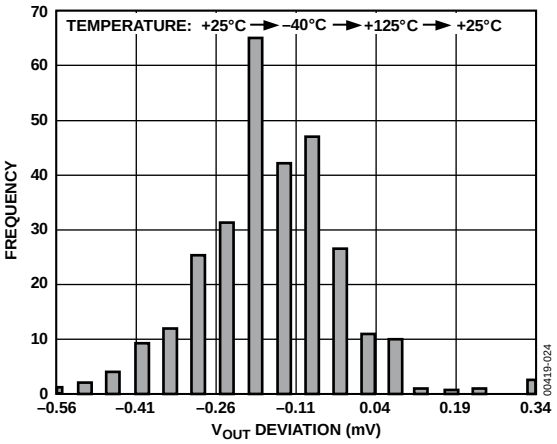



Figure 17. ADR391 $V_{OUT}$ Hysteresis Distribution

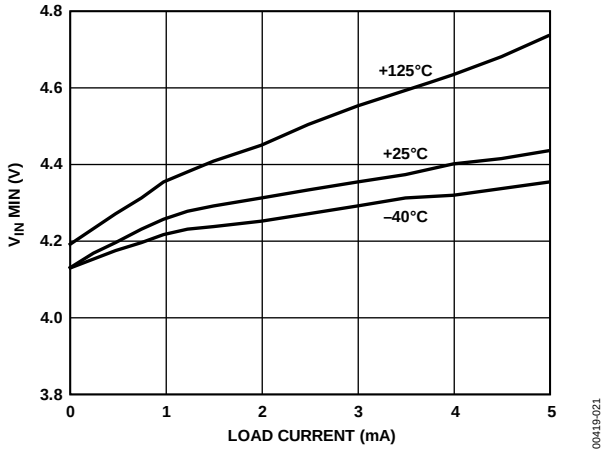



Figure 15. ADR392 Minimum Input Voltage ($V_{IN}$) vs. Load Current

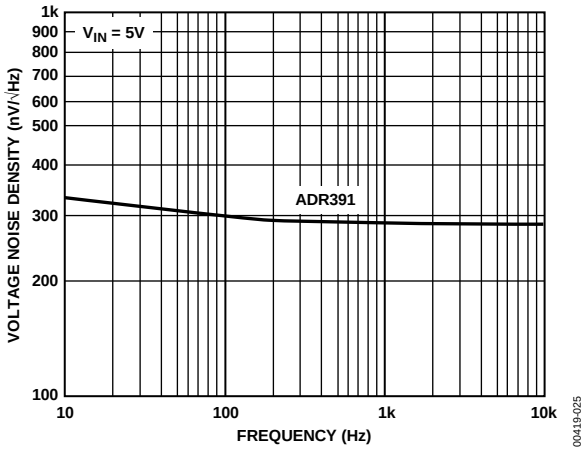



Figure 18. Voltage Noise Density vs. Frequency

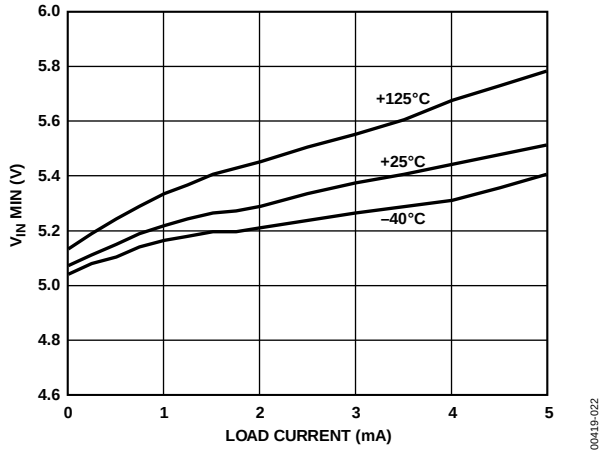



Figure 16. ADR395 Minimum Input Voltage ($V_{IN}$) vs. Load Current

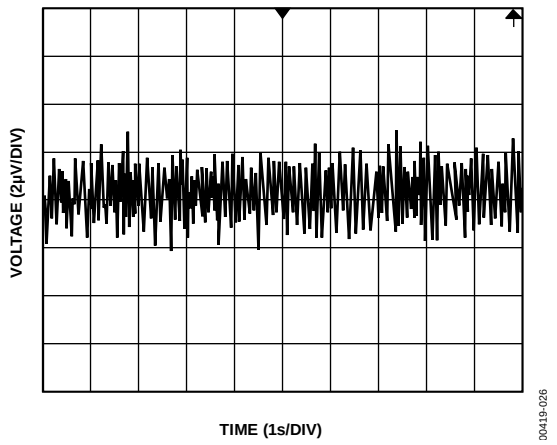



Figure 19. ADR391 Typical Voltage Noise 0.1 Hz to 10 Hz

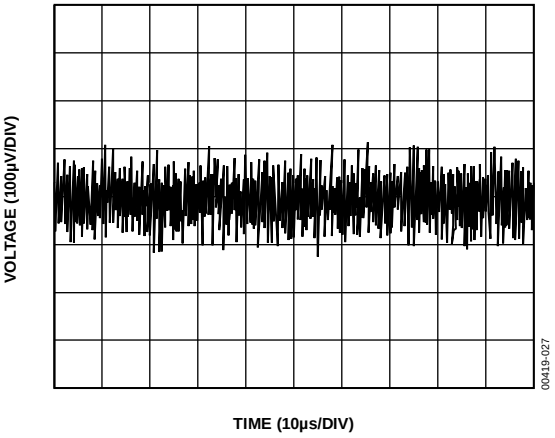



Figure 20. ADR391 Voltage Noise 10 Hz to 10 kHz

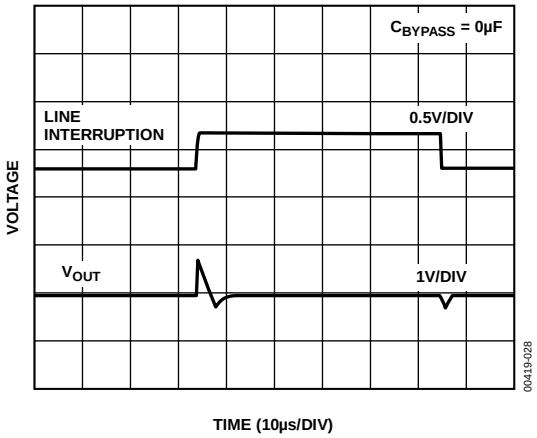



Figure 21. ADR391 Line Transient Response

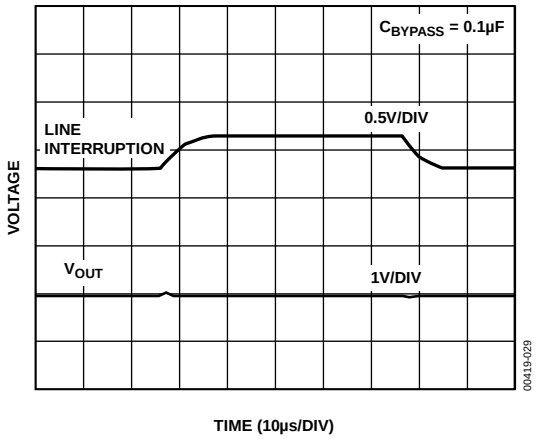



Figure 22. ADR391 Line Transient Response

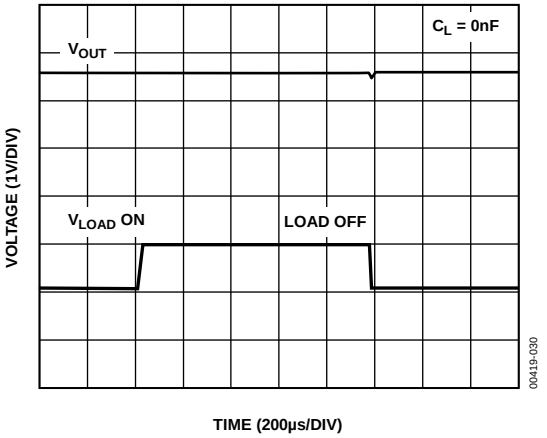



Figure 23. ADR391 Load Transient Response

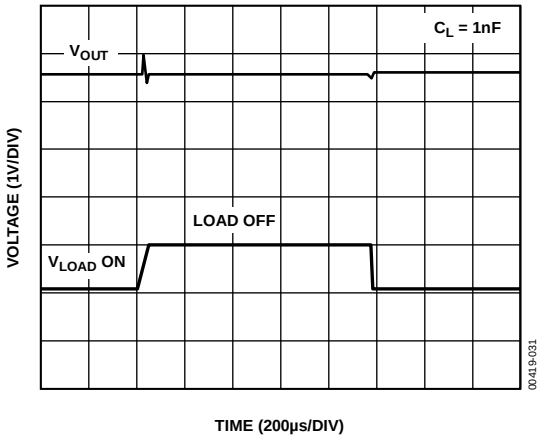



Figure 24. ADR391 Load Transient Response

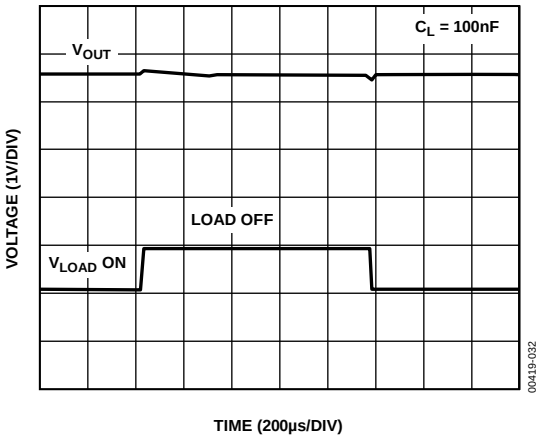



Figure 25. ADR391 Load Transient Response

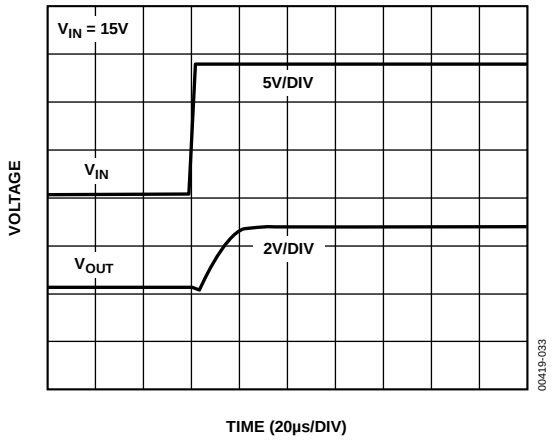



Figure 26. ADR391 Turn-On Response Time at 15 V

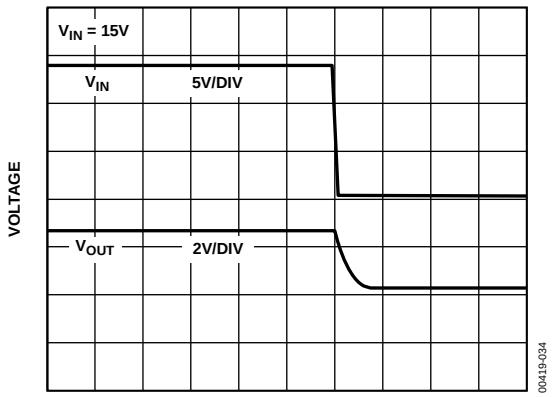



Figure 27. ADR391 Turn-Off Response at 15 V

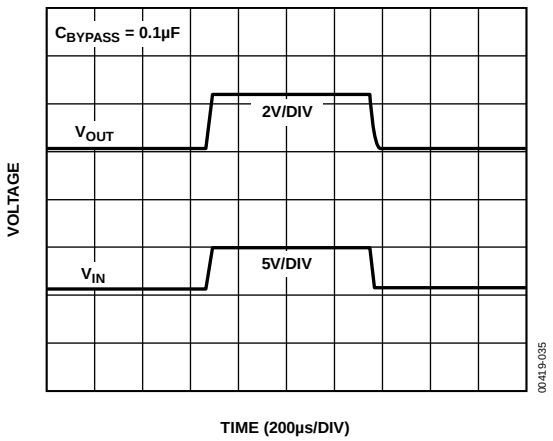



Figure 28. ADR391 Turn-On/Turn-Off Response at 5 V with Capacitance

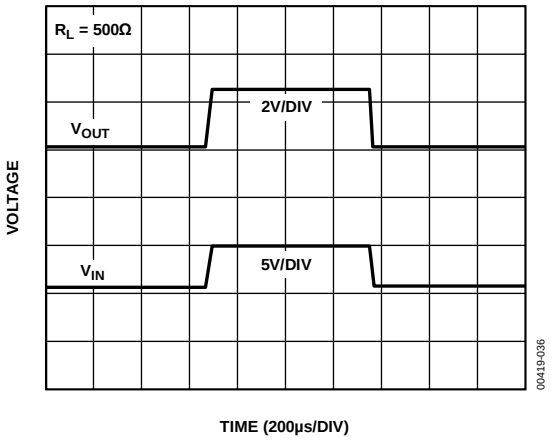



Figure 29. ADR391 Turn-On/Turn-Off Response at 5 V with Resistor Load

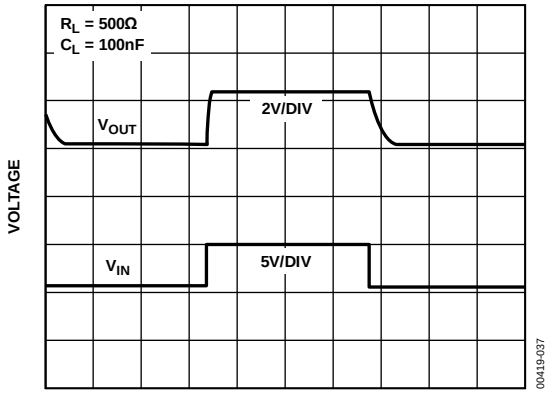



Figure 30. ADR391 Turn-On/Turn-Off Response at 5 V

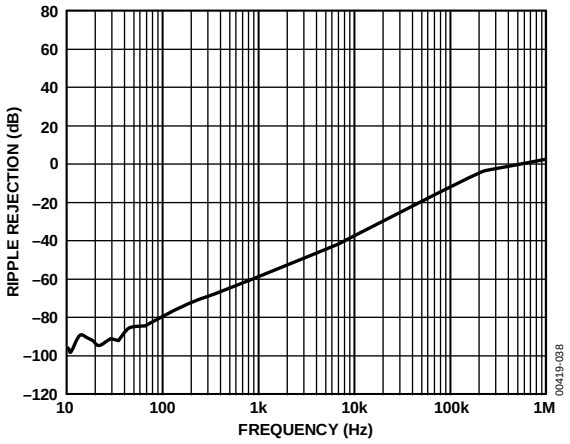



*Figure 31. Ripple Rejection vs. Frequency*

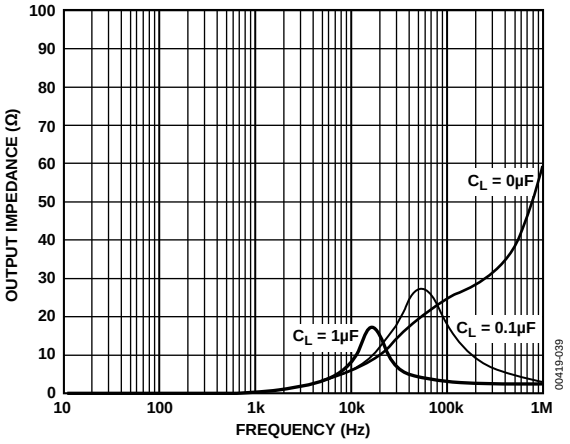



*Figure 32. Output Impedance vs. Frequency*

# TERMINOLOGY

**Temperature Coefficient**

The change of output voltage with respect to operating temperature changes normalized by the output voltage at 25°C. This parameter is expressed in ppm/°C and can be determined by

$$TCV_O[\text{ppm/°C}] = \frac{V_O(T_2) - V_O(T_1)}{V_O(25°\text{C}) \times (T_2 - T_1)} \times 10^6 \quad (1)$$

where:

$V_O$ (25°C) is $V_O$ at 25°C.

$V_O$ ($T_1$) is $V_O$ at Temperature 1.

$V_O$ ($T_2$) is $V_O$ at Temperature 2.

**Line Regulation**

The change in output voltage due to a specified change in input voltage. This parameter accounts for the effects of self-heating. Line regulation is expressed in either percent per volt, parts-per-million per volt, or microvolts per volt change in input voltage.

**Load Regulation**

The change in output voltage due to a specified change in load current. This parameter accounts for the effects of self-heating. Load regulation is expressed in either microvolts per milliampere, parts-per-million per milliampere, or ohms of dc output resistance.

**Long-Term Stability**

Typical shift of output voltage at 25°C on a sample of parts subjected to a test of 1000 hours at 25°C.

$$\Delta V_O = V_O(t_0) - V_O(t_1)$$

$$\Delta V_O[\text{ppm}] = \left( \frac{V_O(t_0) - V_O(t_1)}{V_O(t_0)} \times 10^6 \right) \quad (2)$$

where:

$V_O$ ($t_0$) is $V_O$ at 25°C at Time 0.

$V_O$ ($t_1$) is $V_O$ at 25°C after 1000 hours operation at 25°C.

**Thermally Induced Output Voltage Hysteresis**

The change of output voltage after the device cycles through the temperatures from +25°C to −40°C to +125°C and back to +25°C. This is a typical value from a sample of parts put through such a cycle.

$$V_{O\_HYS} = V_O(25°\text{C}) - V_{O\_TC} \quad (3)$$

$$V_{O\_HYS}[\text{ppm}] = \frac{V_O(25^\circ C) - V_{O\_TC}}{V_O(25^\circ C)} \times 10^6 \quad (4)$$

where:

$V_O$ (25°C) is $V_O$ at 25°C.

$V_{O\_TC}$ is $V_O$ at 25°C after a temperature cycle from +25°C to −40°C to +125°C and back to +25°C.

# THEORY OF OPERATION

Band gap references are the high performance solution for low supply voltage and low power voltage reference applications, and the ADR391/ADR392/ADR395 are no exception. The uniqueness of these devices lies in the architecture. As shown in Figure 33, the ideal zero TC band gap voltage is referenced to the output, not to ground. Therefore, if noise exists on the ground line, it is greatly attenuated on $V_{OUT}$. The band gap cell consists of the PNP pair, Q51 and Q52, running at unequal current densities. The difference in $V_{BE}$ results in a voltage with a positive TC, which is amplified by a ratio of

$$2 \times \frac{R58}{R54}$$

This PTAT voltage, combined with $V_{BE}$s of Q51 and Q52, produces a stable band gap voltage.

Reduction in the band gap curvature is performed by the ratio of Resistors R44 and R59, one of which is linearly temperature dependent. Precision laser trimming and other patented circuit techniques are used to further enhance the drift performance.

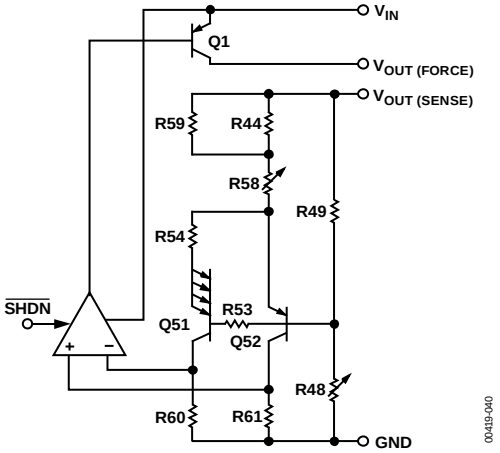



*Figure 33. Simplified Schematic*

## DEVICE POWER DISSIPATION CONSIDERATIONS

The ADR391/ADR392/ADR395 are capable of delivering load currents to 5 mA, with an input voltage that ranges from 2.8 V (ADR391 only) to 15 V. When these devices are used in applications with large input voltages, care should be taken to avoid exceeding the specified maximum power dissipation or junction temperature because it could result in premature device failure. The following formula should be used to calculate the maximum junction temperature or dissipation of the device:

$$P_D = \frac{T_J - T_A}{\theta_{JA}} \quad (5)$$

where:
$T_J$ and $T_A$ are, respectively, the junction and ambient temperatures.
$P_D$ is the device power dissipation.
$\theta_{JA}$ is the device package thermal resistance.

## SHUTDOWN MODE OPERATION

The ADR391/ADR392/ADR395 include a shutdown feature that is TTL/CMOS level compatible. A logic low or a zero volt condition on the $\overline{\text{SHDN}}$ pin is required to turn the devices off. During shutdown, the output of the reference becomes a high impedance state, where its potential would then be determined by external circuitry. If the shutdown feature is not used, the $\overline{\text{SHDN}}$ pin should be connected to $V_{IN}$ (Pin 2).

# APPLICATIONS INFORMATION

## BASIC VOLTAGE REFERENCE CONNECTION

The circuit shown in Figure 34 illustrates the basic configuration for the ADR39x family. Decoupling capacitors are not required for circuit stability. The ADR39x family is capable of driving capacitive loads from 0 µF to 10 µF. However, a 0.1 µF ceramic output capacitor is recommended to absorb and deliver the charge, as required by a dynamic load.

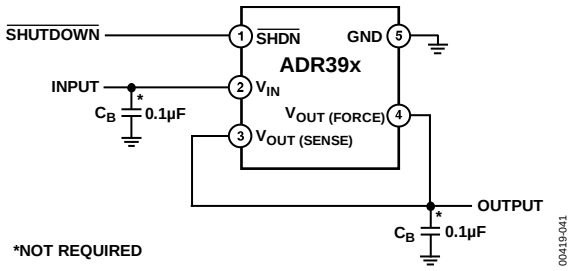



*Figure 34. Basic Configuration for the ADR39x Family*

### *Stacking Reference ICs for Arbitrary Outputs*

Some applications may require two reference voltage sources, which are a combined sum of standard outputs. Figure 35 shows how this stacked output reference can be implemented.

OUTPUT TABLE

| U1/U2 | $V_{OUT1}$ (V) | $V_{OUT2}$ (V) |
|---|---|---|
| ADR391/ADR391 | 2.5 | 5.0 |
| ADR392/ADR392 | 4.096 | 8.192 |
| ADR395/ADR395 | 5 | 10 |

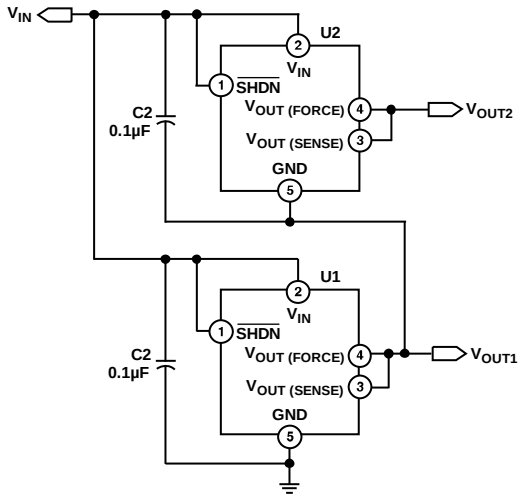



*Figure 35. Stacking Voltage References with the ADR391/ADR392/ADR395*

Two reference ICs are used, fed from an unregulated input, $V_{IN}$. The outputs of the individual ICs are connected in series, which provide two output voltages, $V_{OUT1}$ and $V_{OUT2}$. $V_{OUT1}$ is the terminal voltage of U1, while $V_{OUT2}$ is the sum of this voltage and the terminal voltage of U2. U1 and U2 are chosen for the two voltages that supply the required outputs (see the Output Table in Figure 35). For example, if both U1 and U2 are ADR391s, $V_{OUT1}$ is 2.5 V and $V_{OUT2}$ is 5.0 V.

While this concept is simple, a precaution is required. Because the lower reference circuit must sink a small bias current from U2 plus the base current from the series PNP output transistor in U2, either the external load of U1 or an external resistor must provide a path for this current. If the U1 minimum load is not well defined, the external resistor should be used and set to a value that conservatively passes 600 µA of current with the applicable $V_{OUT1}$ across it. Note that the two U1 and U2 reference circuits are treated locally as macrocells; each has its own bypasses at input and output for best stability. Both U1 and U2 in this circuit can source dc currents up to their full rating. The minimum input voltage, $V_{IN}$, is determined by the sum of the outputs, $V_{OUT2}$, plus the dropout voltage of U2.

### *A Negative Precision Reference without Precision Resistors*

A negative reference can be easily generated by adding an A1 op amp and is configured as shown in Figure 36. $V_{OUT\ (FORCE)}$ and $V_{OUT\ (SENSE)}$ are at virtual ground and, therefore, the negative reference can be taken directly from the output of the op amp. The op amp must be dual-supply, low offset, and rail-to-rail if the negative supply voltage is close to the reference output.

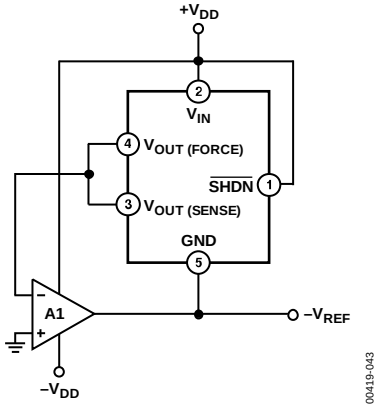



*Figure 36. Negative Reference*

### General-Purpose Current Source

Many times in low power applications, the need arises for a precision current source that can operate on low supply voltages. The ADR391/ADR392/ADR395 can be configured as a precision current source. As shown in Figure 37, the circuit configuration is a floating current source with a grounded load. The reference output voltage is bootstrapped across $R_{SET}$, which sets the output current into the load. With this configuration, circuit precision is maintained for load currents in the range from the reference supply current, typically 90 μA to approximately 5 mA.

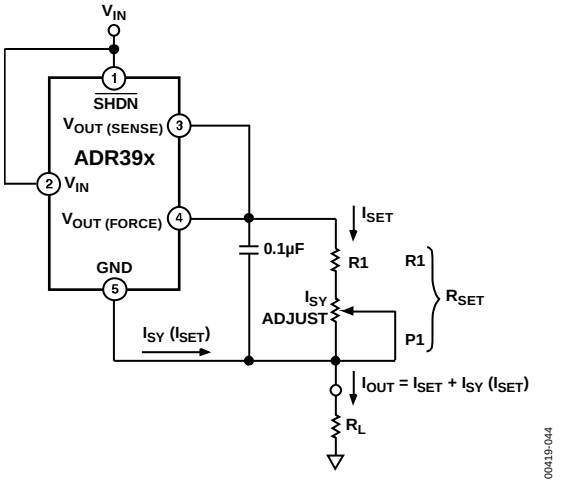



*Figure 37. A General-Purpose Current Source*

### High Power Performance with Current Limit

In some cases, the user may want higher output current delivered to a load and still achieve better than 0.5% accuracy out of the ADR39x. The accuracy for a reference is normally specified on the data sheet with no load. However, the output voltage changes with load current.

The circuit shown in Figure 38 provides high current without compromising the accuracy of the ADR39x. The series pass transistor, Q1, provides up to 1 A load current. The ADR39x delivers only the base drive to Q1 through the force pin. The sense pin of the ADR39x is a regulated output and is connected to the load.

The Transistor Q2 protects Q1 during short-circuit limit faults by robbing its base drive. The maximum current is

$$I_{LMAX} \approx 0.6\ V/R_S \quad (6)$$

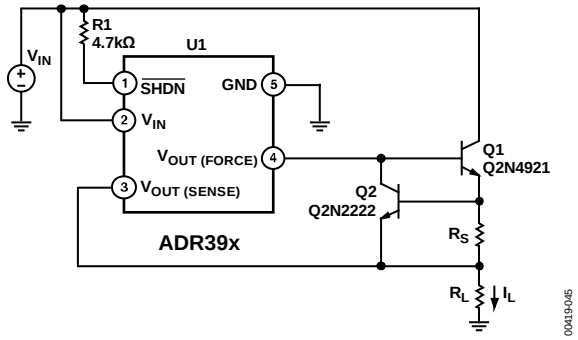



*Figure 38. ADR39x for High Power Performance with Current Limit*

A similar circuit function can also be achieved with the Darlington transistor configuration, as shown in Figure 39.

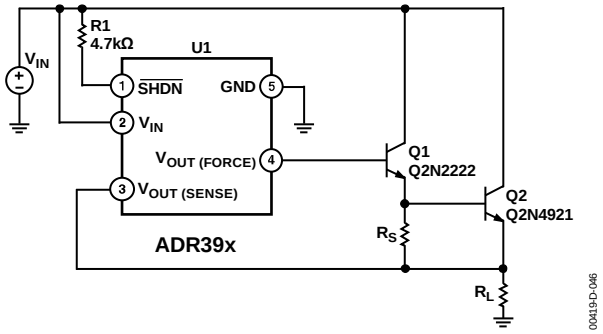



*Figure 39. ADR39x for High Output Current with Darlington Drive Configuration*

## CAPACITORS

### *Input Capacitor*

Input capacitors are not required on the ADR39x. There is no limit for the value of the capacitor used on the input, but a 1 µF to 10 µF capacitor on the input improves transient response in applications where the supply suddenly changes. An additional 0.1 µF in parallel also helps reduce noise from the supply.

### *Output Capacitor*

The ADR39x does not require output capacitors for stability under any load condition. An output capacitor, typically 0.1 µF, filters out any low level noise voltage and does not affect the operation of the part. On the other hand, the load transient response can improve with the addition of a 1 µF to 10 µF output capacitor in parallel. A capacitor here acts as a source of stored energy for a sudden increase in load current. The only parameter that degrades by adding an output capacitor is the turn-on time, and it depends on the size of the capacitor chosen.

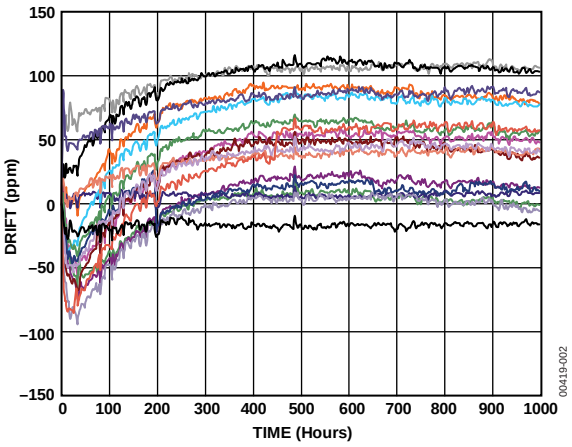
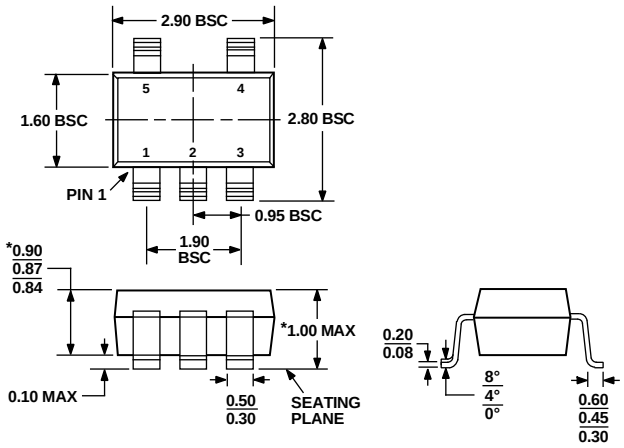



*Figure 40. ADR391 Typical Long-Term Drift over 1000 Hours*

# OUTLINE DIMENSIONS




*COMPLIANT TO JEDEC STANDARDS MO-193-AB WITH THE EXCEPTION OF PACKAGE HEIGHT AND THICKNESS.

*Figure 41. 5-Lead Thin Small Outline Transistor Package [TSOT] (UJ-5)*
*Dimensions shown in millimeters*

## ORDERING GUIDE

| Model | Output Voltage ($V_O$) | Initial Accuracy (mV) | Initial Accuracy (%) | Temperature Coefficient (ppm/°C) | Package Description | Package Option | Branding | Ordering Quantity | Temperature Range |
|---|---|---|---|---|---|---|---|---|---|
| ADR391AUJZ-REEL7[1] | 2.5 | ±6 | 0.24 | 25 | 5-Lead TSOT | UJ-5 | R1A | 3,000 | −40°C to +125°C |
| ADR391AUJZ-R2[1] | 2.5 | ±6 | 0.24 | 25 | 5-Lead TSOT | UJ-5 | R1A | 250 | −40°C to +125°C |
| ADR391BUJZ-REEL7[1] | 2.5 | ±4 | 0.16 | 9 | 5-Lead TSOT | UJ-5 | R1B | 3,000 | −40°C to +125°C |
| ADR391BUJZ-R2[1] | 2.5 | ±4 | 0.16 | 9 | 5-Lead TSOT | UJ-5 | R1B | 250 | −40°C to +125°C |
| ADR392AUJZ-REEL7[1] | 4.096 | ±6 | 0.15 | 25 | 5-Lead TSOT | UJ-5 | RCA | 3,000 | −40°C to +125°C |
| ADR392AUJZ-R2[1] | 4.096 | ±6 | 0.15 | 25 | 5-Lead TSOT | UJ-5 | RCA | 250 | −40°C to +125°C |
| ADR392BUJZ-REEL7[1] | 4.096 | ±5 | 0.12 | 9 | 5-Lead TSOT | UJ-5 | RCB | 3,000 | −40°C to +125°C |
| ADR392BUJZ-R2[1] | 4.096 | ±5 | 0.12 | 9 | 5-Lead TSOT | UJ-5 | RCB | 250 | −40°C to +125°C |
| ADR392WBUJZ-R7[1, 2] | 4.096 | ±5 | 0.12 | 9 | 5-Lead TSOT | UJ-5 | RCB | 3,000 | −40°C to +125°C |
| ADR395AUJZ-REEL7[1] | 5.0 | ±6 | 0.12 | 25 | 5-Lead TSOT | UJ-5 | RDA | 3,000 | −40°C to +125°C |
| ADR395AUJZ-R2[1] | 5.0 | ±6 | 0.12 | 25 | 5-Lead TSOT | UJ-5 | RDA | 250 | −40°C to +125°C |
| ADR395BUJZ-REEL7[1] | 5.0 | ±5 | 0.10 | 9 | 5-Lead TSOT | UJ-5 | RDB | 3,000 | −40°C to +125°C |
| ADR395BUJZ-R2[1] | 5.0 | ±5 | 0.10 | 9 | 5-Lead TSOT | UJ-5 | RDB | 250 | −40°C to +125°C |

[1] Z = RoHS Compliant Part.
[2] Automotive grade.

## NOTES

# NOTES


D00419-0-10/09(H)