8-BIT & 12-BIT PROGRAMMABLE PULSE GENERATORS

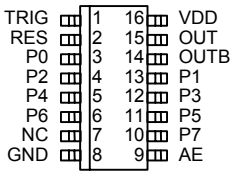
(SERIES 3D7608 & 3D7612: PARALLEL INTERFACE)

FEATURES

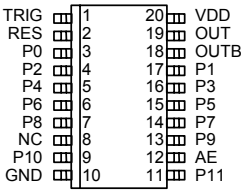
- All-silicon, low-power CMOS technology
- TTL/CMOS compatible inputs and outputs
- Vapor phase, IR and wave solderable
- Programmable via latched parallel interface
- **Increment range:** 0.25ns through 800us
- **Pulse width tolerance:** 1% (See Table 1)
- **Supply current:** 8mA typical
- **Temperature stability:** ±1.5% max (-40C to 85C)
- **Vdd stability:** ±0.5% max (4.75V to 5.25V)

RoHS Compliant

PACKAGES / PINOUTS



3D7608R-xx SOIC



3D7612W-xx SOL

For mechanical dimensions, click here.
For package marking details, click here.

FUNCTIONAL DESCRIPTION

The 3D7608 & 3D7612 devices are versatile 8- & 12-bit programmable monolithic pulse generators. A rising-edge on the trigger input (TRIG) initiates the pulse, which is presented on the output pins (OUT,OUTB). The pulse width, programmed via the parallel interface, can be varied over 255 (3D7608) or 4095 (3D7612) equal steps according to the formula:

$$t_{PW} = t_{inh} + addr * t_{inc}$$

where addr is the programmed address, t_{inc} is the pulse width increment (equal to the device dash number), and t_{inh} is the inherent (address zero) pulse width. The device also offers a reset input (RES), which can be used to terminate the pulse before the programmed time has expired.

PIN DESCRIPTIONS

TRIG	Trigger Input
RES	Reset Input
OUT	Pulse Output
OUTB	Complementary Pulse Output
AE	Address Enable Input
P0-P11	Address Inputs
VDD	+5 Volts
GND	Ground
NC	Do not connect externally

The all-CMOS 3D7608 & 3D7612 integrated circuits have been designed as reliable, economic alternatives to hybrid TTL pulse generators. The 3D7608 is offered in a standard 16-pin SOIC, and the 3D7612 is offered in a standard 20-pin SOL.

TABLE 1: PART NUMBER SPECIFICATIONS

PART # (8-BIT)	PART # (12-BIT)	Pulse Width Increment	Maximum P.W. (8-Bit)	Maximum P.W. (12-Bit)
3D7608R-0.25	3D7612W-0.25	0.25ns ± 0.12ns	77.25ns ± 3ns	1.04us ± 10ns
3D7608R-0.5	3D7612W-0.5	0.50ns ± 0.25ns	141.5ns ± 3ns	2.06us ± 21ns
3D7608R-1	3D7612W-1	1.0ns ± 0.5ns	269ns ± 3ns	4.11us ± 41ns
3D7608R-2	3D7612W-2	2.0ns ± 1.0ns	524ns ± 6ns	8.20us ± 82ns
3D7608R-5	3D7612W-5	5.0ns ± 2.5ns	1.29us ± 13ns	20.5us ± 205ns
3D7608R-10	3D7612W-10	10ns ± 5.0ns	2.56us ± 26ns	41.0us ± 410ns
3D7608R-20	3D7612W-20	20ns ± 10ns	5.11us ± 52ns	81.9us ± 819ns
3D7608R-50	3D7612W-50	50ns ± 25ns	12.8us ± 128ns	205us ± 2.1us
3D7608R-100	3D7612W-100	100ns ± 50ns	25.5us ± 255ns	410us ± 4.1us
3D7608R-200	3D7612W-200	200ns ± 100ns	51.0us ± 510ns	819us ± 8.2us
3D7608R-500	3D7612W-500	500ns ± 250ns	128us ± 1.3us	2.05ms ± 21us
3D7608R-1K	3D7612W-1K	1.0us ± 0.5us	255us ± 2.6us	4.10ms ± 41us
3D7608R-2K	3D7612W-2K	2.0us ± 1.0us	510us ± 5.2us	8.19ms ± 82us
3D7608R-5K	3D7612W-5K	5.0us ± 2.5us	1.28ms ± 13us	20.5ms ± 205us
3D7608R-10K	3D7612W-10K	10us ± 5.0us	2.55ms ± 26us	41.0ms ± 410us
3D7608R-20K	3D7612W-20K	20us ± 10us	5.10ms ± 52us	81.9ms ± 819us
3D7608R-50K	3D7612W-50K	50us ± 25us	12.8ms ± 128us	205ms ± 2.1 ms

PART # (8-BIT)	Pulse Width Increment	Maximum P.W. (8-Bit)
3D7608R-100K	100us ± 50us	25.5ms ± 260us
3D7608R-200K	200us ± 100us	51.0ms ± 510us
3D7608R-500K	500us ± 250us	128ms ± 1.3ms
3D7608R-800K	800us ± 400us	204ms ± 2.1ms

NOTE: Any increment between 0.25ns and 800us (50us for the 12-bit generator) not shown is also available as a standard device.

APPLICATION NOTES

GENERAL INFORMATION

Figure 1 illustrates the main functional blocks of the 3D7608 & 3D7612. Since these devices are CMOS designs, all unused input pins must be returned to well-defined logic levels, VDD or Ground.

The pulse generator architecture is comprised of a number of delay cells (for fine control) and an oscillator & counter (for coarse control). Each device is individually trimmed for maximum accuracy and linearity throughout the address range. The change in pulse width from one address setting to the next is called the *increment*, or LSB. It is nominally equal to the device dash number. The minimum pulse width, achieved by setting the address to zero, is called the *inherent pulse width*.

For best performance, it is essential that the power supply pin be adequately bypassed and filtered. In addition, the power bus should be of as low an impedance construction as possible. Power planes are preferred. Also, signal traces should be kept as short as possible.

PULSE WIDTH ACCURACY

There are a number of ways of characterizing the pulse width accuracy of a programmable pulse generator. The first is the *differential nonlinearity* (DNL), also referred to as the increment error. It is defined as the deviation of the increment at a given address from its nominal value. For most dash numbers, the DNL is within 0.5 LSB at every address (see Table 1: Pulse Width Step).

The *integrated nonlinearity* (INL) is determined by first constructing the least-squares best fit straight line through the pulse-width-versus-address data. The INL is then the deviation of a given width from this line. For all dash numbers, the INL is within 1.0 LSB at every address.

The *relative error* is defined as follows:

$$e_{rel} = (t_{PW} - t_{inh}) - addr * t_{inc}$$

where addr is the address, t_{PW} is the measured width at this address, t_{inh} is the measured inherent width, and t_{inc} is the nominal increment. It is very similar to the INL, but simpler to calculate. For most dash numbers, the relative error is less than 1.0 LSB at every address (see Table 1).

The *absolute error* is defined as follows:

$$e_{abs} = t_{PW} - (t_{inh} + addr * t_{inc})$$

where t_{inh} is the nominal inherent delay. The absolute error is limited to 1.5 LSB or 3.0 ns, whichever is greater, at every address.

The *inherent pulse width error* is the deviation of the inherent width from its nominal value. It is limited to 2.0 ns from the nominal inherent pulse width of 14 ns.

PULSE WIDTH STABILITY

The characteristics of CMOS integrated circuits are strongly dependent on power supply and temperature. The 3D7608 & 3D7612 utilize novel compensation circuitry to minimize the performance variations induced by fluctuations in power supply and/or temperature.

With regard to stability, the output pulse width of the 3D7608 & 3D7612 at a given address, addr, can be split into two components: the *inherent pulse width* (t_{inh}) and the *relative pulse width* (t_{PW} - t_{inh}). These components exhibit very different stability coefficients, both of which must be considered in very critical applications.

The thermal coefficient of the relative pulse width is limited to ±250 PPM/C, which is equivalent to a variation, over the -40C to 85C operating range, of ±1.5% from the room-temperature pulse width. This holds for all dash numbers. The thermal coefficient of the inherent pulse width is nominally +10ps/C for dash numbers less than 1, and +15ps/C for all other dash numbers.

The power supply sensitivity of the relative pulse width is ±0.5% over the 4.75V to 5.25V operating range, with respect to the pulse width at the nominal 5.0V power supply. This holds for all dash numbers. The sensitivity of the inherent pulse width is nominally –1ps/mV for all dash numbers.

It should also be noted that the DNL is also adversely affected by thermal and supply variations, particularly at the MSL/LSB crossovers (ie, 63 to 64, 127 to 128, etc).

APPLICATION NOTES (CONT'D)

TRIGGER & RESET TIMING

Figure 2 shows the timing diagram of the device when the reset input (RES) is not used. In this case, the pulse is triggered by the rising edge of the TRIG signal and ends at a time determined by the address loaded into the device. While the pulse is active, any additional triggers occurring are ignored. Once the pulse has ended, and after a short recovery time, the next trigger is recognized. Figure 3 shows the timing for the case where a reset is issued before the pulse has ended. Again, there is a short recovery time required before the next trigger can occur.

ADDRESS UPDATE

The 3D7608/3D7612 can operate in one of two addressing modes. In the transparent mode (AE held high), the parallel address inputs must persist for the duration of the output pulse, in accordance with Figure 4. In the latched mode, the address data is stored internally, which allows the parallel inputs to be connected to a multi-purpose data bus. Timing for this mode is also shown in Figure 4.

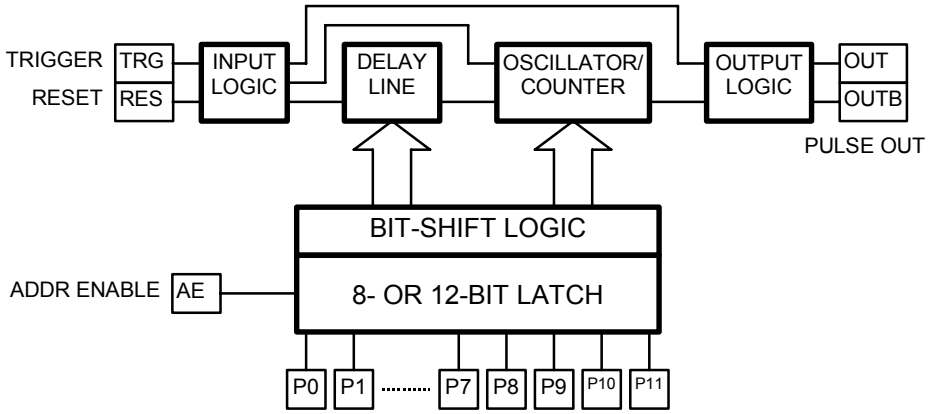


Figure 1: Functional block diagram

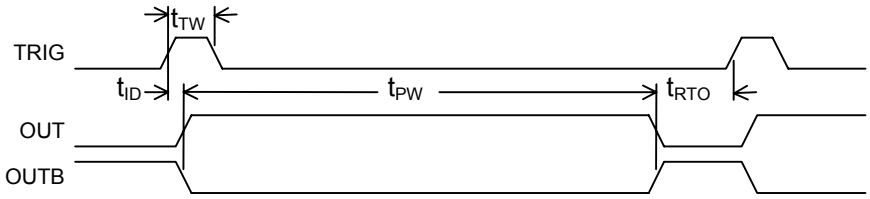


Figure 2: Timing Diagram (RES=0)

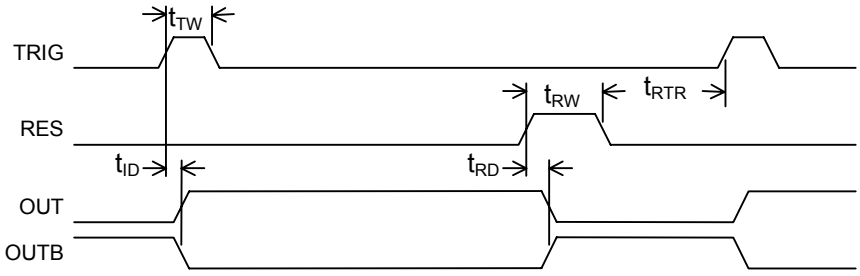


Figure 3: Timing Diagram (with reset)

APPLICATION NOTES (CONT'D)

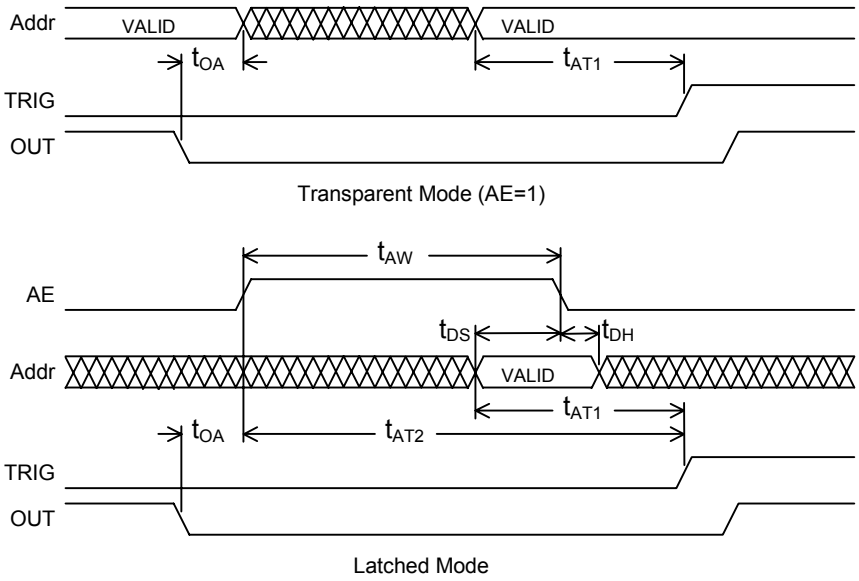


Figure 4: Address Update

DEVICE SPECIFICATIONS

TABLE 2: ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
DC Supply Voltage	V_{DD}	-0.3	7.0	V	
Input Pin Voltage	V_{IN}	-0.3	V_{DD}+0.3	V	
Input Pin Current	I_{IN}	-10	10	mA	25C
Storage Temperature	T_{STRG}	-55	150	C	
Lead Temperature	T_{LEAD}		300	C	10 sec

TABLE 3: DC ELECTRICAL CHARACTERISTICS

(-40C to 85C, 4.75V to 5.25V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Static Supply Current*	I_{DD}		8.0	12.0	mA	
High Level Input Voltage	V_{IH}	2.0			V	
Low Level Input Voltage	V_{IL}			0.8	V	
High Level Input Current	I_{IH}			1.0	µA	$V_{IH} = V_{DD}$
Low Level Input Current	I_{IL}			1.0	µA	$V_{IL} = 0V$
High Level Output Current	I_{OH}		-35.0	-4.0	mA	$V_{DD} = 4.75V$ $V_{OH} = 2.4V$
Low Level Output Current	I_{OL}	4.0	15.0		mA	$V_{DD} = 4.75V$ $V_{OL} = 0.4V$
Output Rise & Fall Time	T_R & T_F		2.0	2.5	ns	C_{LD} = 5 pf

*I_{DD}(Dynamic) = 2 * C_{LD} * V_{DD} * F
where: C_{LD} = Average capacitance load/output (pf)
F = Trigger frequency (GHz)

Input Capacitance = 5 pf typical
Output Load Capacitance (C_{LD}) = 25 pf max

TABLE 4: AC ELECTRICAL CHARACTERISTICS

(-40C to 85C, 4.75V to 5.25V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	REFER TO
Trigger Width	t_{TW}	5			ns	Figure 2 & 3
Trigger Inherent Delay	t_{ID}			5	ns	Figure 2 & 3
Output Pulse Width	t_{PW}				ns	Figure 2
Re-trigger Time	t_{RTO}	3			ns	Figure 2
Reset Width	t_{RW}	TBD			ns	Figure 3
Reset to Output Low	t_{RD}			5	ns	Figure 3
End of Reset to Next Trigger	t_{RTR}	3			ns	Figure 3
AE Width	t_{AW}	12			ns	Figure 4
Data Setup to AE Low	t_{DS}	10			ns	Figure 4
Data Hold from AE Low	t_{DH}	3			ns	Figure 4
Output Low to AE High	t_{OA}	3			ns	Figure 4
Data Valid to Trigger	t_{AT1}	10			ns	Figure 4
AE High to Trigger	t_{AT2}	10			ns	Figure 4

TYPICAL APPLICATIONS

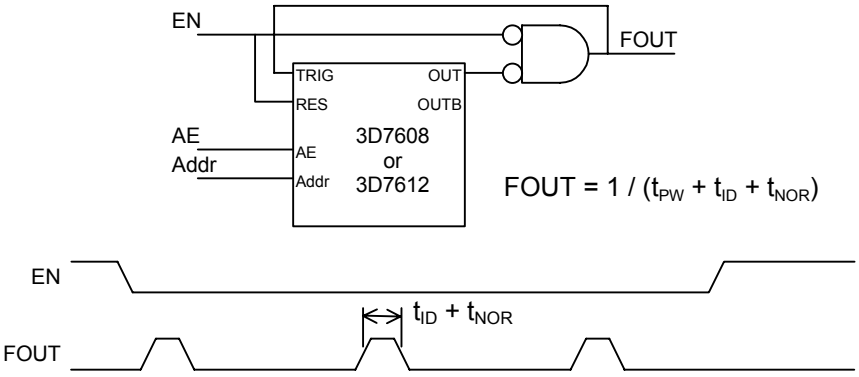


Figure 5: Programmable Oscillator

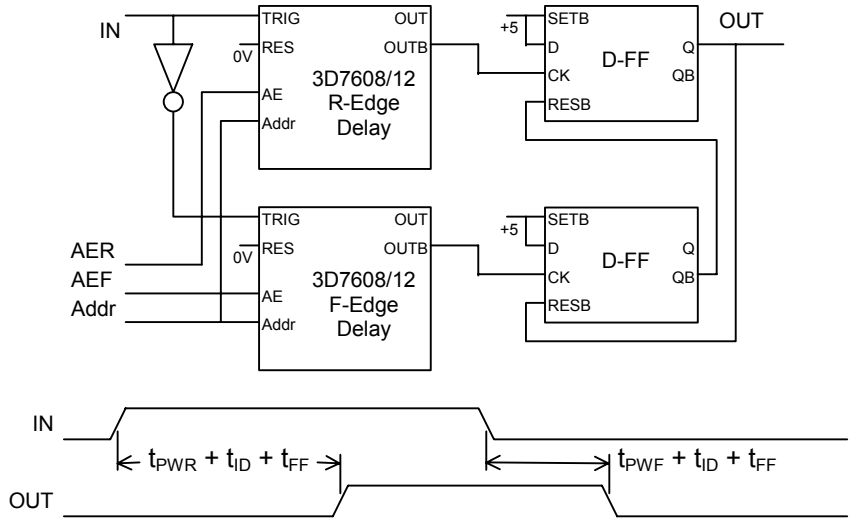


Figure 6: Programmable Delay Line

SILICON DEVICE AUTOMATED TESTING

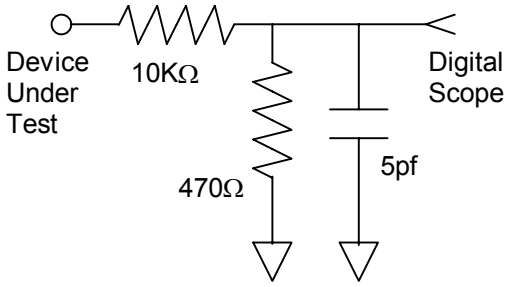
TEST CONDITIONS

INPUT:

Ambient Temperature: 25°C ± 3°C
Supply Voltage (Vcc): 5.0V ± 0.1V
Input Pulse: High = 3.0V ± 0.1V
Low = 0.0V ± 0.1V
Source Impedance: 50Ω Max.
Rise/Fall Time: 3.0 ns Max. (measured between 0.6V and 2.4V)
Pulse Width: PW_{IN} = 20ns
Period: PER_{IN} = 2 x Prog'd Pulse Width

OUTPUT:

R_{load}: 10KΩ ± 10%
C_{load}: 5pf ± 10%
Threshold: 1.5V (Rising & Falling)



NOTE: The above conditions are for test only and do not in any way restrict the operation of the device.

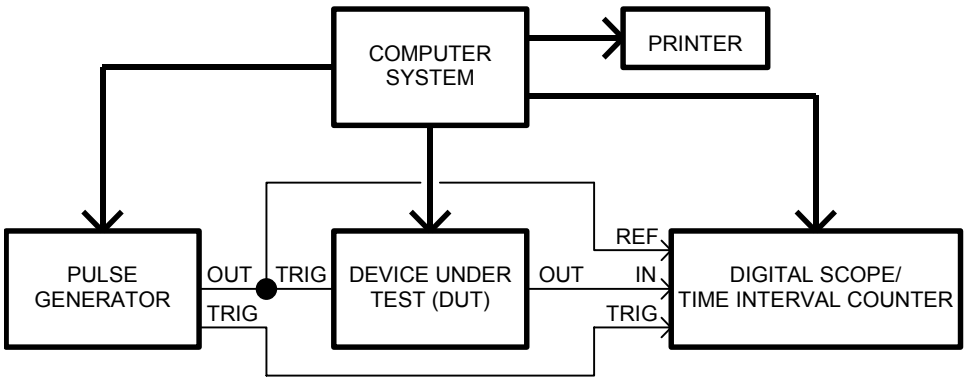


Figure 7: Test Setup

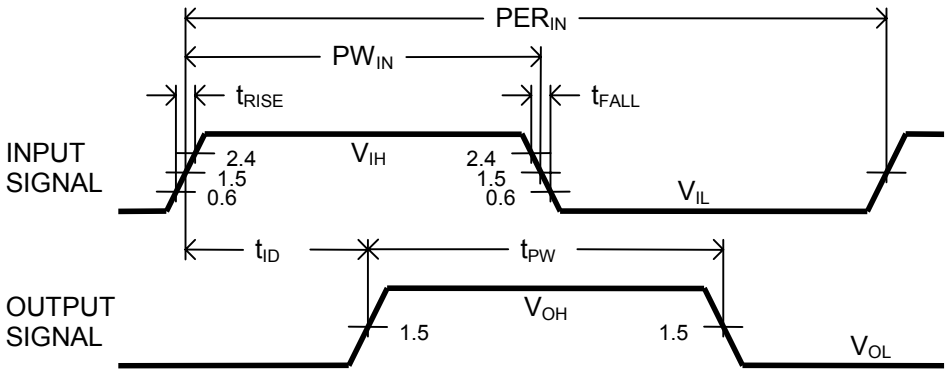


Figure 8: Timing Diagram