September 11, 2009

National Semiconductor

LM8261 Single

RRIO, High Output Current & Unlimited Cap Load Op Amp in SOT23-5

General Description

The LM8261 is a Rail-to-Rail input and output Op Amp which can operate with a wide supply voltage range. This device has high output current drive, greater than Rail-to-Rail input common mode voltage range, unlimited capacitive load drive capability, and provides tested and guaranteed high speed and slew rate while requiring only 0.97mA supply current. It is specifically designed to handle the requirements of flat panel TFT panel V_{COM} driver applications as well as being suitable for other low power, and medium speed applications which require ease of use and enhanced performance over existing devices.

Greater than Rail-to-Rail input common mode voltage range with 50dB of Common Mode Rejection, allows high side and low side sensing, among many applications, without having any concerns over exceeding the range and no compromise in accuracy. Exceptionally wide operating supply voltage range of 2.5V to 30V alleviates any concerns over functionality under extreme conditions and offers flexibility of use in multitude of applications. In addition, most device parameters are insensitive to power supply variations; this design enhancement is yet another step in simplifying its usage. The output stage has low distortion (0.05% THD+N) and can supply a respectable amount of current (15mA) with minimal headroom from either rail (300mV).

The LM8261 is offered in the space saving SOT23-5 package.

Features

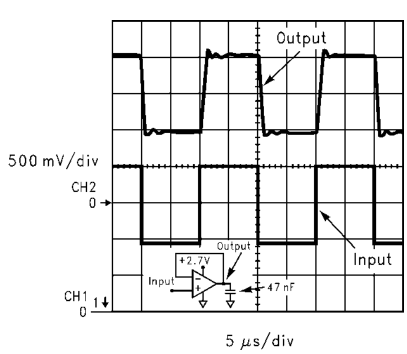
(V_S = 5V, T_A = 25°C, Typical values unless specified).

- GBWP 21MHz
- Wide supply voltage range 2.5V to 30V
- Slew rate 12V/µs
- Supply current 0.97 mA
- Cap load limit Unlimited
- Output short circuit current +53mA/−75mA
- ±5% Settling time 400ns (500pF, 100mV_{PP} step)
- Input common mode voltage 0.3V beyond rails
- Input voltage noise 15nV/$\sqrt{Hz}$
- Input current noise 1pA/$\sqrt{Hz}$
- THD+N < 0.05%

Applications

- TFT-LCD flat panel V_{COM} driver
- A/D converter buffer
- High side/low side sensing
- Headphone amplifier

Output Response with Heavy Capacitive Load



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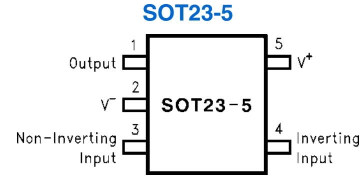
Connection Diagram

SOT23-5



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Top View

Ordering Information

Package	Ordering Info	Pkg Marking	Supplied As	NSC Drawing
5-Pin SOT-23	LM8261M5	A45A	1K Units Tape and Reel	MF05A
	LM8261M5 NOPB			
	LM8261M5X		3K Units Tape and Reel	
	LM8261M5X NOPB			

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

ESD Tolerance	
Human Body Model	2KV (Note 2)
Machine Model	200V(Note 9)
V_{IN} Differential	+/−10V
Output Short Circuit Duration	(Note 3, Note 11)
Supply Voltage (V+ - V−)	32V
Voltage at Input/Output pins	V+ +0.8V, V− −0.1V
Storage Temperature Range	−65°C to +150°C
Junction Temperature (Note 4)	+150°C
Soldering Information:	
Infrared or Convection (20 sec.)	235°C
Wave Soldering (10 sec.)	260°C

Operating Ratings

Supply Voltage (V+ - V−)	2.5V to 30V
Temperature Range(Note 4)	−40°C to +85°C
Package Thermal Resistance, θ_{JA},(Note 4)	
SOT23-5	325°C/W

2.7V Electrical Characteristics (Note 13)

Unless otherwise specified, all limits guaranteed for T_A = 25°C, V+ = 2.7V, V− = 0V, V_{CM} = 0.5V, V_O = V+/2, and R_L > 1MΩ to V−. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Typ (Note 5)	Limit (Note 6)	Units
V_{OS}	Input Offset Voltage	V_{CM} = 0.5V & V_{CM} = 2.2V	+/−0.7	+/−5 **+/−7**	mV max
TC V_{OS}	Input Offset Average Drift	V_{CM} = 0.5V & V_{CM} = 2.2V (Note 12)	+/−2	–	µV/C
I_B	Input Bias Current	V_{CM} = 0.5V (Note 7)	−1.20	−2.00 **−2.70**	µA max
		V_{CM} = 2.2V (Note 7)	+0.49	+1.00 **+1.60**	
I_{OS}	Input Offset Current	V_{CM} = 0.5V & V_{CM} = 2.2V	20	250 **400**	nA max
CMRR	Common Mode Rejection Ratio	V_{CM} stepped from 0V to 1.0V	100	76 **60**	dB min
		V_{CM} stepped from 1.7V to 2.7V	100		
		V_{CM} stepped from 0V to 2.7V	70	58 **50**	
+PSRR	Positive Power Supply Rejection Ratio	V+ = 2.7V to 5V	104	78 **74**	dB min
CMVR	Input Common-Mode Voltage Range	CMRR > 50dB	−0.3	−0.1 **0.0**	V max
			3.0	2.8 **2.7**	V min
A_{VOL}	Large Signal Voltage Gain	V_O = 0.5 to 2.2V, R_L = 10K to V−	78	70 **67**	dB min
		V_O = 0.5 to 2.2V, R_L = 2K to V−	73	67 **63**	dB min
V_O	Output Swing High	R_L = 10K to V−	2.59	2.49 **2.46**	V min
		R_L = 2K to V−	2.53	2.45 **2.41**	
	Output Swing Low	R_L = 10K to V−	90	100 **120**	mV max
I_{SC}	Output Short Circuit Current	Sourcing to V− V_{ID} = 200mV (Note 10)	48	30 **20**	mA min
		Sinking to V+ V_{ID} = −200mV (Note 10)	65	50 **30**	mA min

Symbol	Parameter	Condition	Typ (Note 5)	Limit (Note 6)	Units
I_S	Supply Current	No load, V_{CM} = 0.5V	0.95	1.20 **1.50**	mA max
SR	Slew Rate (Note 8)	A_V = +1, V_I = $2V_{PP}$	9	–	V/μs
f_u	Unity Gain-Frequency	V_I = 10mV, R_L = 2KΩ to $V^+/2$	10	–	MHz
GBWP	Gain Bandwidth Product	f = 50KHz	21	15.5 **14**	MHz min
Phi_m	Phase Margin	V_I = 10mV	50	–	Deg
e_n	Input-Referred Voltage Noise	f = 2KHz, R_S = 50Ω	15	–	$nV/\sqrt{Hz}$
i_n	Input-Referred Current Noise	f = 2KHz	1		$pA/\sqrt{Hz}$
f_{MAX}	Full Power Bandwidth	Z_L = (20pF ǁ 10KΩ) to $V^+/2$	1	–	MHz

5V Electrical Characteristics (Note 13)

Unless otherwise specified, all limited guaranteed for T_A = 25°C, V^+ = 5V, V^- = 0V, V_{CM} = 1V, V_O = $V^+/2$, and R_L > 1MΩ to V^-. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Typ (Note 5)	Limit (Note 6)	Units
V_{OS}	Input Offset Voltage	V_{CM} = 1V & V_{CM} = 4.5V	+/−0.7	+/−5 **+/− 7**	mV max
TC V_{OS}	Input Offset Average Drift	V_{CM} = 1V & V_{CM} = 4.5V (Note 12)	+/−2	–	μV/°C
I_B	Input Bias Current	V_{CM} = 1V (Note 7)	−1.18	−2.00 **−2.70**	μA max
		V_{CM} = 4.5V (Note 7)	+0.49	+1.00 **+1.60**	
I_{OS}	Input Offset Current	V_{CM} = 1V & V_{CM} = 4.5V	20	250 **400**	nA max
CMRR	Common Mode Rejection Ratio	V_{CM} stepped from 0V to 3.3V	110	84 **72**	dB min
		V_{CM} stepped from 4V to 5V	100	–	
		V_{CM} stepped from 0V to 5V	80	64 **61**	
+PSRR	Positive Power Supply Rejection Ratio	V^+ = 2.7V to 5V, V_{CM} = 0.5V	104	78 **74**	dB min
CMVR	Input Common-Mode Voltage Range	CMRR > 50dB	−0.3	−0.1 **0.0**	V max
			5.3	5.1 **5.0**	V min
A_{VOL}	Large Signal Voltage Gain	V_O = 0.5 to 4.5V, R_L = 10K to V^-	84	74 **70**	dB min
		V_O = 0.5 to 4.5V, R_L = 2K to V^-	80	70 **66**	
V_O	Output Swing High	R_L = 10K to V^-	4.87	4.75 **4.72**	V min
		R_L = 2K to V^-	4.81	4.70 **4.66**	
	Output Swing Low	R_L = 10K to V^-	86	125 **135**	mV max

Symbol	Parameter	Condition	Typ (Note 5)	Limit (Note 6)	Units
I_{SC}	Output Short Circuit Current	Sourcing to V− V_{ID} = 200mV (Note 10)	53	35 **20**	mA min
		Sinking to V+ V_{ID} = −200mV (Note 10)	75	60 **50**	
I_S	Supply Current	No load, V_{CM} = 1V	0.97	1.25 **1.75**	mA max
SR	Slew Rate (Note 8)	A_V = +1, V_I = $5V_{PP}$	12	10 **7**	V/μs min
f_u	Unity Gain Frequency	V_I = 10mV, R_L = 2KΩ to V+/2	10.5	–	MHz
GBWP	Gain-Bandwidth Product	f = 50KHz	21	16 **15**	MHz min
Phi_m	Phase Margin	V_I = 10mV	53	–	Deg
e_n	Input-Referred Voltage Noise	f = 2KHz, R_S = 50Ω	15	–	$nV/\sqrt{Hz}$
i_n	Input-Referred Current Noise	f = 2KHz	1	–	$pA/\sqrt{Hz}$
f_{MAX}	Full Power Bandwidth	Z_L = (20pF ‖ 10kΩ) to V+/2	900	–	KHz
t_S	Settling Time (±5%)	$100mV_{PP}$ Step, 500pF load	400	–	ns
THD+N	Total Harmonic Distortion + Noise	R_L = 1KΩ to V+/2 f = 10KHz to A_V= +2, $4V_{PP}$ swing	0.05	–	%

±15V Electrical Characteristics (Note 13)

Unless otherwise specified, all limited guaranteed for T_A = 25°C, V+ = 15V, V− = −15V, V_{CM} = 0V, V_O = 0V, and R_L > 1MΩ to 0V. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Typ (Note 5)	Limit (Note 6)	Units
V_{OS}	Input Offset Voltage	V_{CM} = −14.5V & V_{CM} = 14.5V	+/−0.7	+/−7 **+/− 9**	mV max
TC V_{OS}	Input Offset Average Drift	V_{CM} = −14.5V & V_{CM} = 14.5V (Note 12)	+/−2	–	μV/°C
I_B	Input Bias Current	V_{CM} = −14.5V (Note 7)	−1.05	−2.00 **−2.80**	μA max
		V_{CM} = 14.5V (Note 7)	+0.49	+1.00 **+1.50**	
I_{OS}	Input Offset Current	V_{CM} = −14.5V & V_{CM} = 14.5V	30	275 **550**	nA max
CMRR	Common Mode Rejection Ratio	V_{CM} stepped from −15V to 13V	100	84 **80**	dB min
		V_{CM} stepped from 14V to 15V	100	–	
		V_{CM} stepped from −15V to 15V	88	74 **72**	
+PSRR	Positive Power Supply Rejection Ratio	V+ = 12V to 15V	100	70 **66**	dB min
−PSRR	Negative Power Supply Rejection Ratio	V− = −12V to −15V	100	70 **66**	dB min
CMVR	Input Common-Mode Voltage Range	CMRR > 50dB	−15.3	−15.1 **−15.0**	V max
			15.3	15.1 **15.0**	V min

Symbol	Parameter	Condition	Typ (Note 5)	Limit (Note 6)	Units
A_{VOL}	Large Signal Voltage Gain	V_O = 0V to ±13V, R_L = 10KΩ	85	78 **74**	dB min
		V_O = 0V to ±13V, R_L = 2KΩ	79	72 **66**	
V_O	Output Swing High	R_L = 10KΩ	14.83	14.65 **14.61**	V min
		R_L = 2KΩ	14.73	14.60 **14.55**	
	Output Swing Low	R_L = 10KΩ	−14.91	−14.75 **−14.65**	V max
		R_L = 2KΩ	−14.83	−14.65 **−14.60**	
I_{SC}	Output Short Circuit Current	Sourcing to ground V_{ID} = 200mV (Note 10)	60	40 **25**	mA min
		Sinking to ground V_{ID} = 200mV (Note 10)	100	70 **60**	
I_S	Supply Current	No load, V_{CM} = 0V	1.30	1.50 **1.90**	mA max
SR	Slew Rate (Note 8)	A_V = +1, V_I = $24V_{PP}$	15	10 **8**	V/μs min
f_u	Unity Gain Frequency	V_I = 10mV, R_L = 2KΩ	14	–	MHz
GBWP	Gain-Bandwidth Product	f = 50KHz	24	18 **16**	MHz min
Phi_m	Phase Margin	V_I = 10mV	58	–	Deg
e_n	Input-Referred Voltage Noise	f = 2KHz, R_S = 50Ω	15	–	$nV/\sqrt{Hz}$
i_n	Input-Referred Current Noise	f = 2KHz	1	–	$pA/\sqrt{Hz}$
f_{MAX}	Full Power Bandwidth	Z_L = 20pF ‖ 10KΩ	160	–	KHz
t_s	Settling Time (±1%, A_V = +1)	Positive Step, $5V_{PP}$	320	–	ns
		Negative Step, $5V_{PP}$	600	–	
THD+N	Total Harmonic Distortion +Noise	R_L = 1KΩ, f = 10KHz, A_V = +2, $28V_{PP}$ swing	0.01	–	%

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Rating indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.

Note 2: Human Body Model is 1.5kΩ in series with 100pF.

Note 3: Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C.

Note 4: The maximum power dissipation is a function of $T_{J(max)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly onto a PC board.

Note 5: Typical Values represent the most likely parametric norm.

Note 6: All limits are guaranteed by testing or statistical analysis.

Note 7: Positive current corresponds to current flowing into the device.

Note 8: Slew rate is the slower of the rising and falling slew rates. Connected as a Voltage Follower.

Note 9: Machine Model, 0Ω is series with 200pF.

Note 10: Short circuit test is a momentary test. See Note 11.

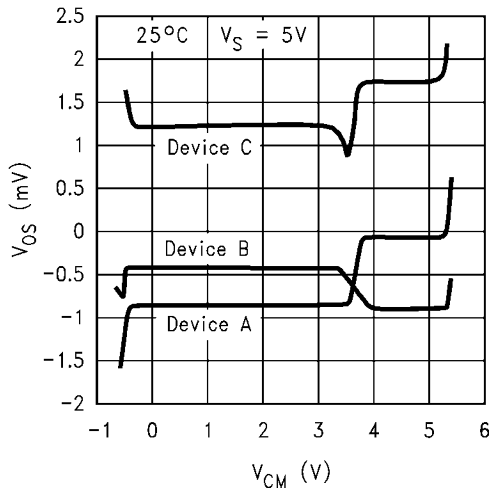
Note 11: Output short circuit duration is infinite for $V_S \leq 6V$ at room temperature and below. For $V_S > 6V$, allowable short circuit duration is 1.5ms.

Note 12: Offset voltage average drift determined by dividing the change in V_{OS} at temperature extremes into the total temperature change.

Note 13: Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No guarantee of parametric performance is indicated in the electrical tables under conditions of internal self heating where $T_J > T_A$.

Typical Performance Characteristics $T_A = 25°C$, Unless Otherwise Noted

V_{OS} vs. V_{CM} for 3 Representative Units



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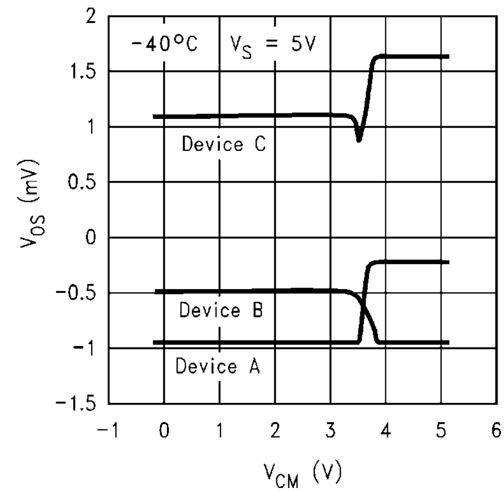
V_{OS} vs. V_{CM} for 3 Representative Units



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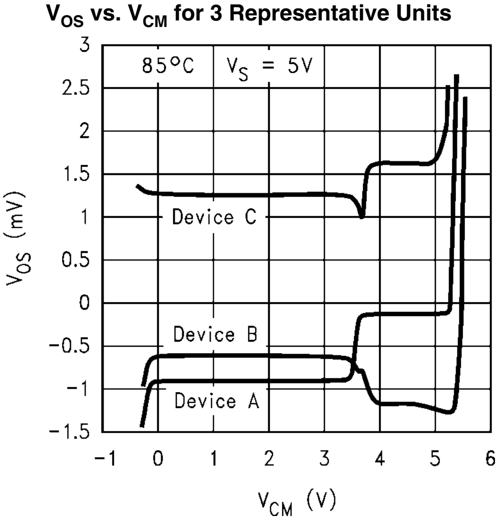
V_{OS} vs. V_{CM} for 3 Representative Units



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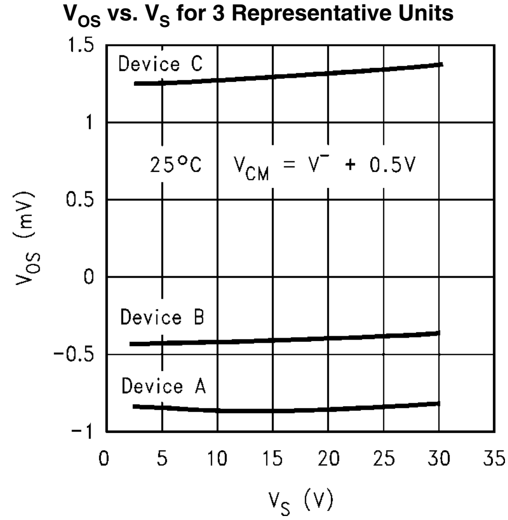
V_{OS} vs. V_S for 3 Representative Units



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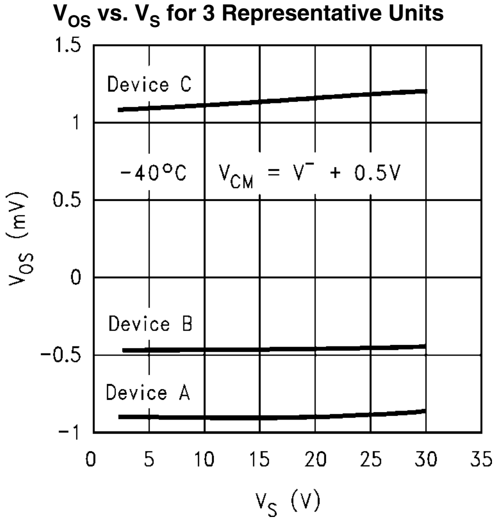
V_{OS} vs. V_S for 3 Representative Units



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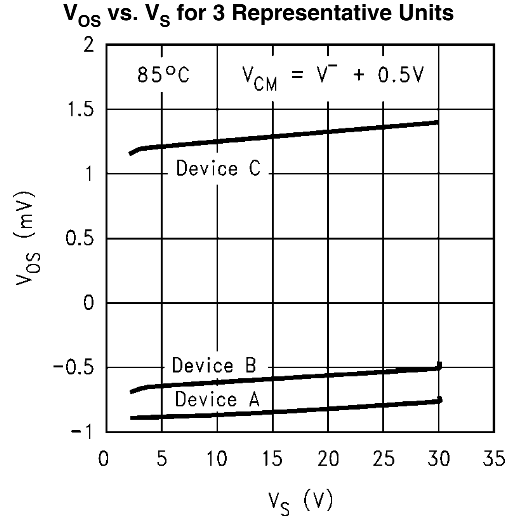
V_{OS} vs. V_S for 3 Representative Units



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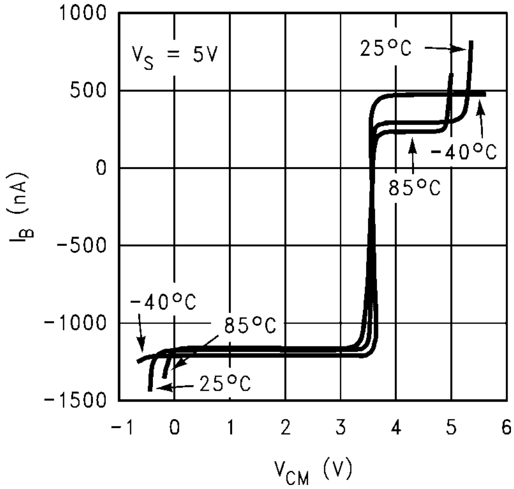
I_B vs. V_{CM}



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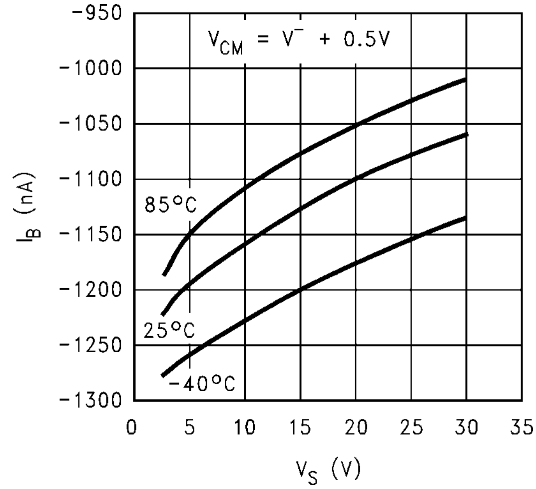
I_B vs. V_S



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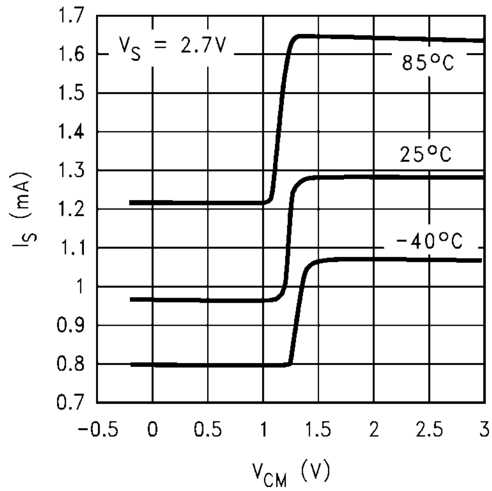
I_S vs. V_{CM}



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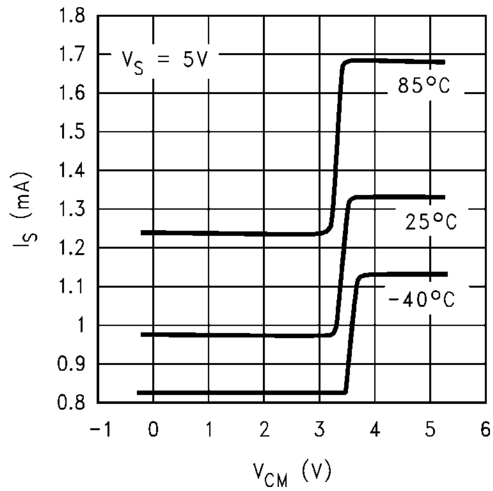
I_S vs. V_{CM}



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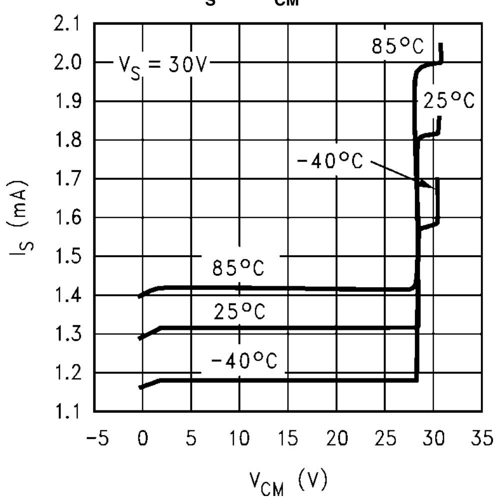
I_S vs. V_{CM}



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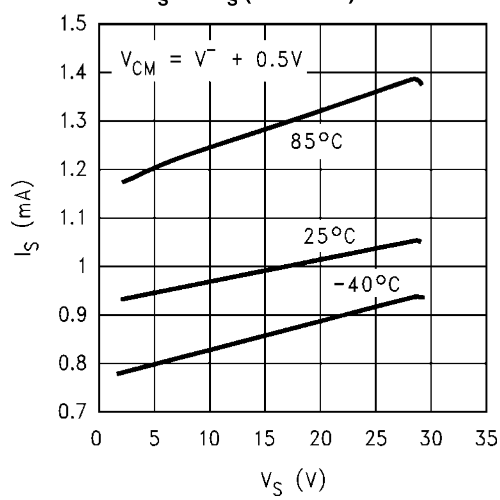
I_S vs. V_S (PNP side)



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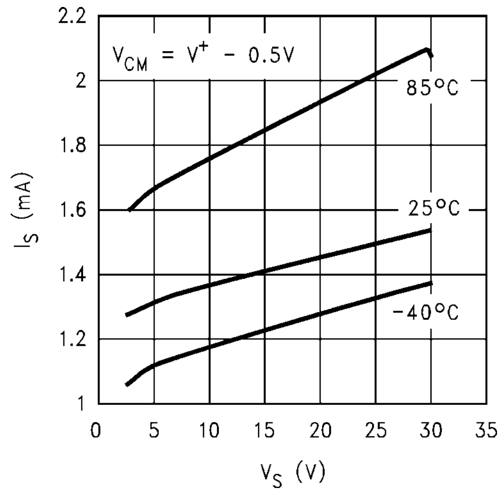
I_S vs. V_S (NPN side)



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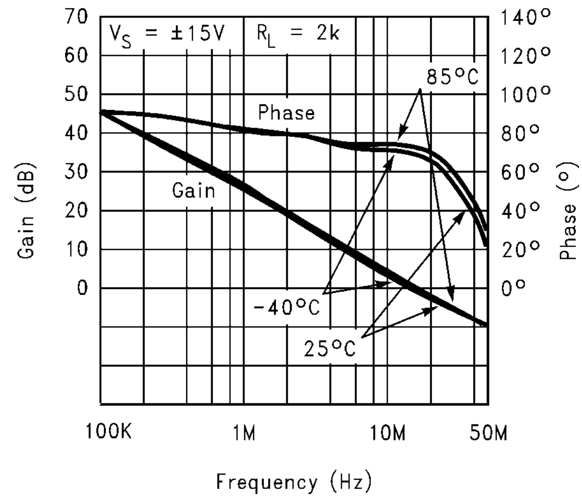
Gain/Phase vs. Frequency



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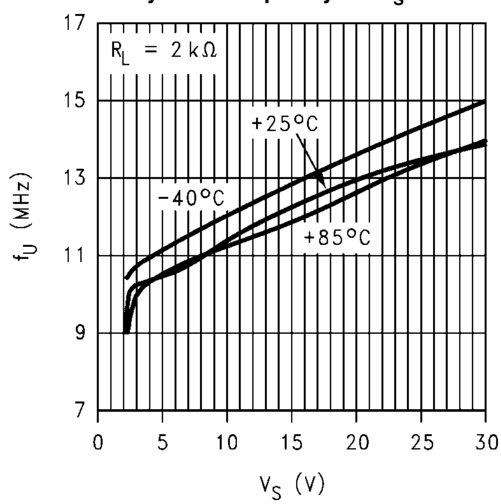
Unity Gain Frequency vs. V_S



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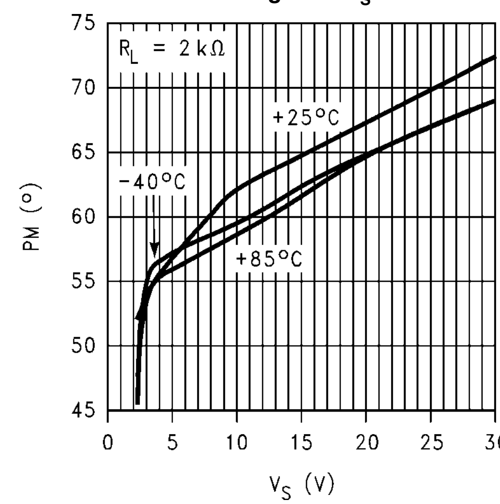
Phase Margin vs. V_S



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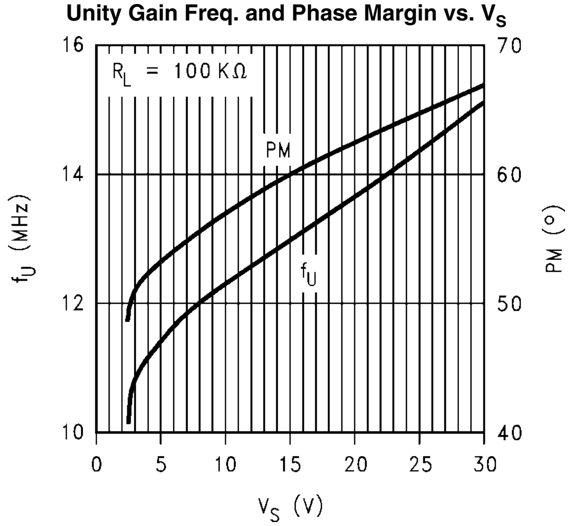
Unity Gain Freq. and Phase Margin vs. V_S



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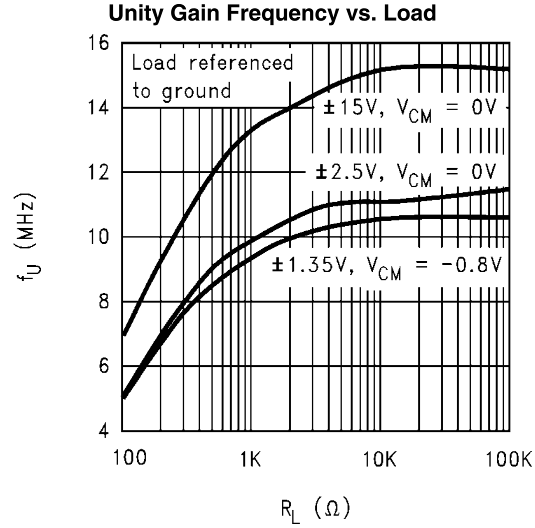
Unity Gain Frequency vs. Load



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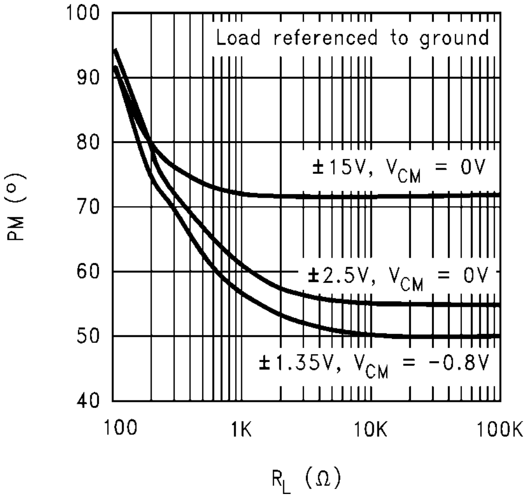
Phase Margin vs. Load



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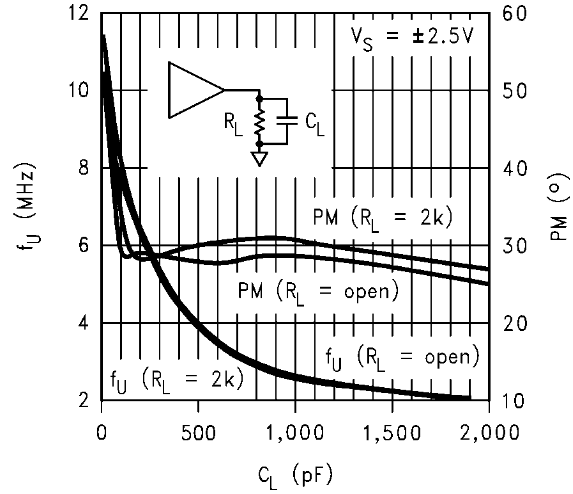
Unity Gain Freq. and Phase Margin vs. C_L



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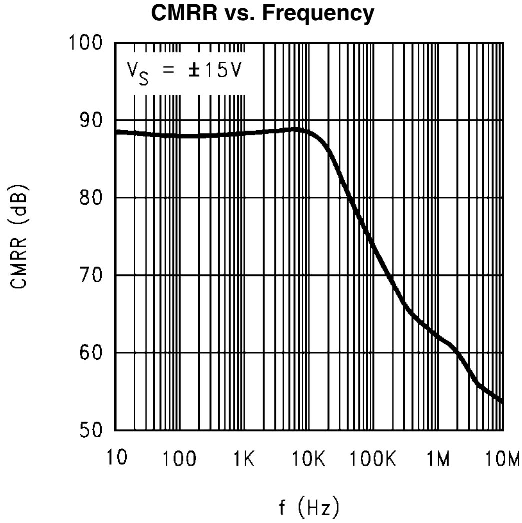
CMRR vs. Frequency



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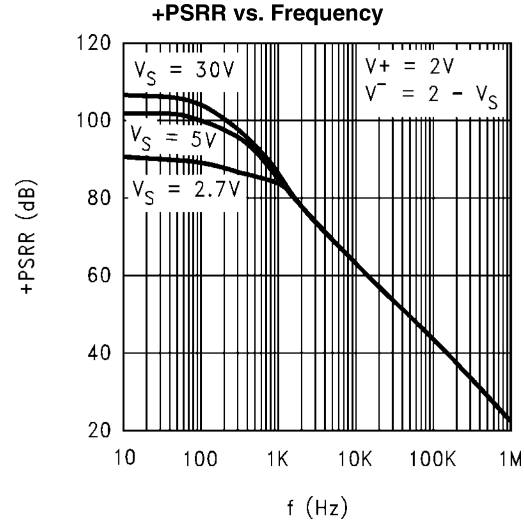
+PSRR vs. Frequency



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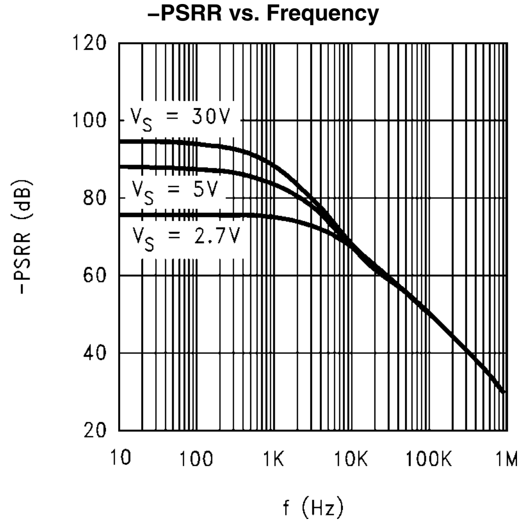
–PSRR vs. Frequency



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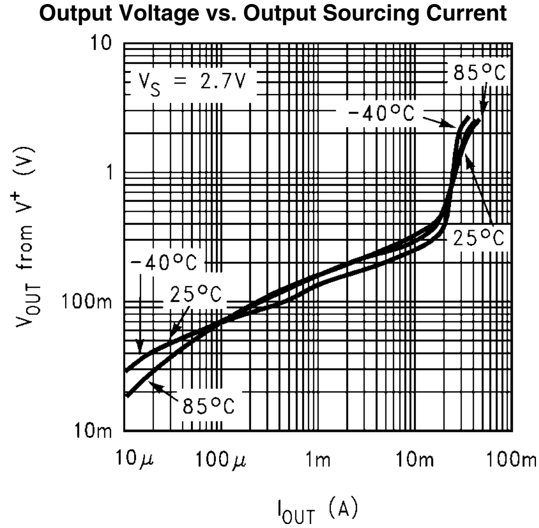
Output Voltage vs. Output Sourcing Current



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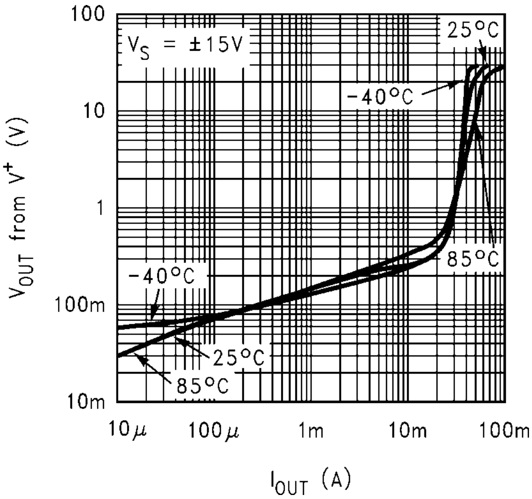
Output Voltage vs. Output Sourcing Current



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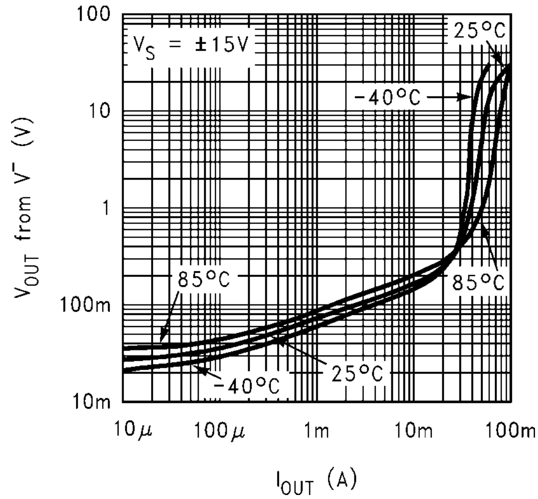
Output Voltage vs. Output Sinking Current



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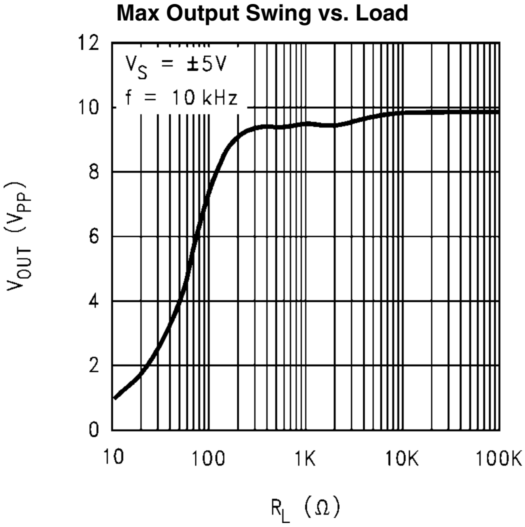
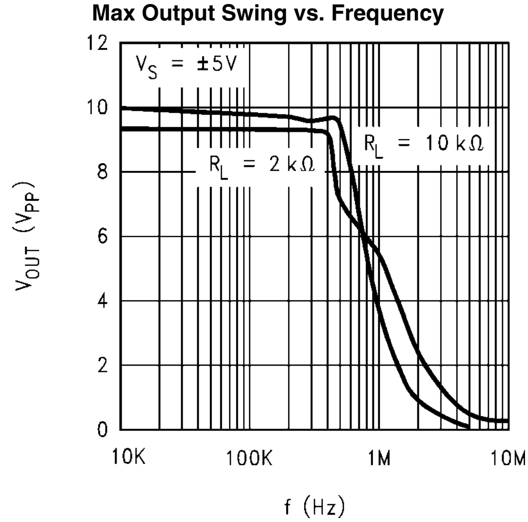
Max Output Swing vs. Load



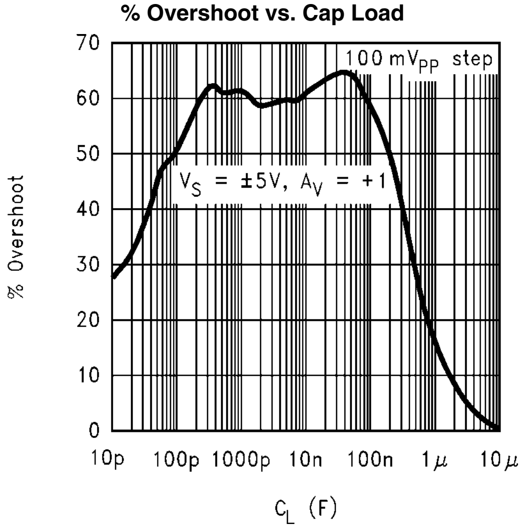
10108410

Max Output Swing vs. Frequency



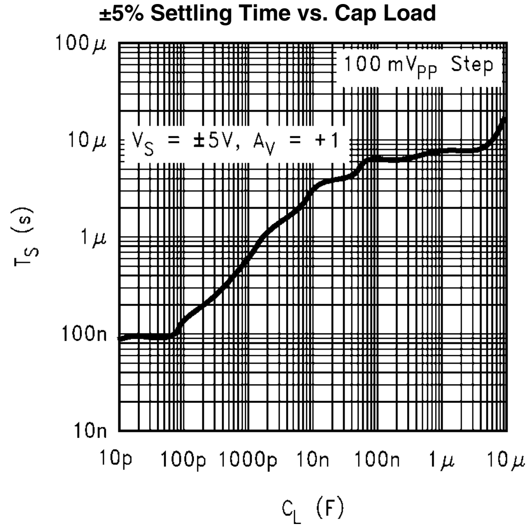
10108411

% Overshoot vs. Cap Load



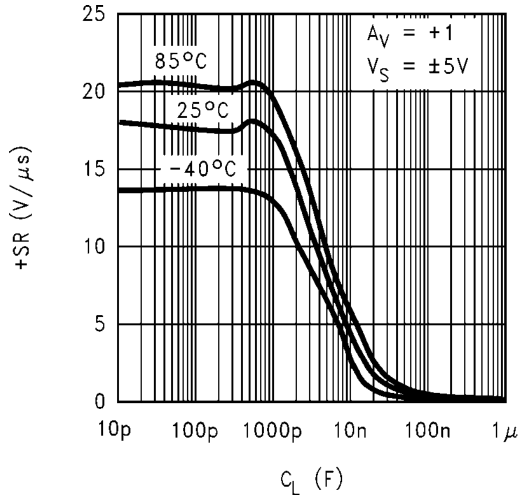
10108448

±5% Settling Time vs. Cap Load



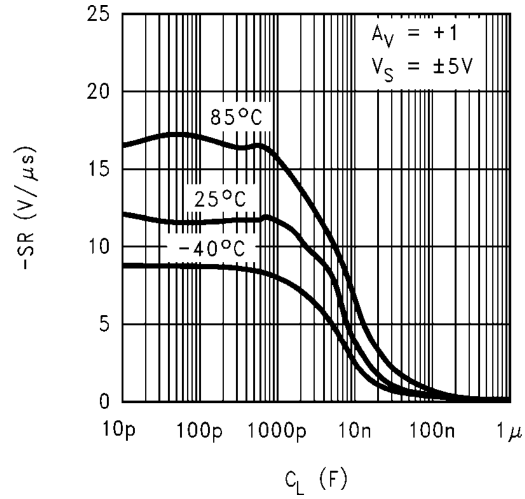
10108447

+SR vs. Cap Load



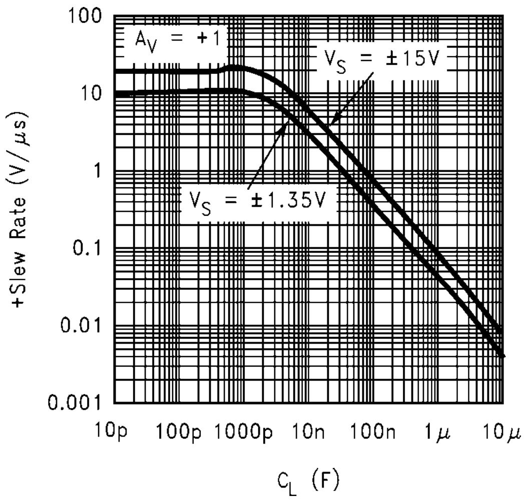
10108451

−SR vs. Cap Load



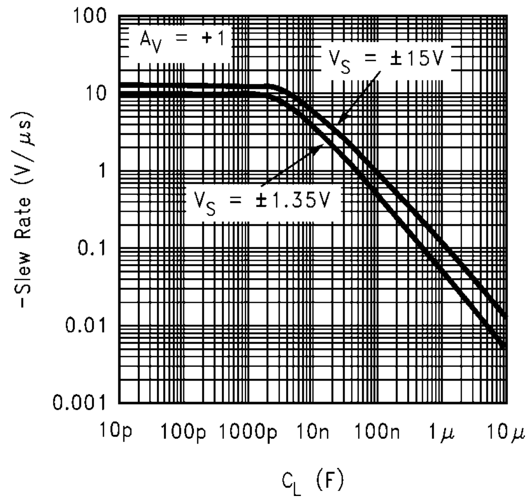
10108452

+SR vs. Cap Load



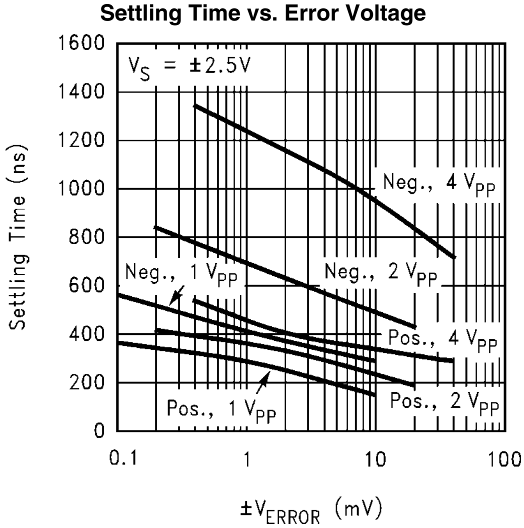
10108449

−SR vs. Cap Load



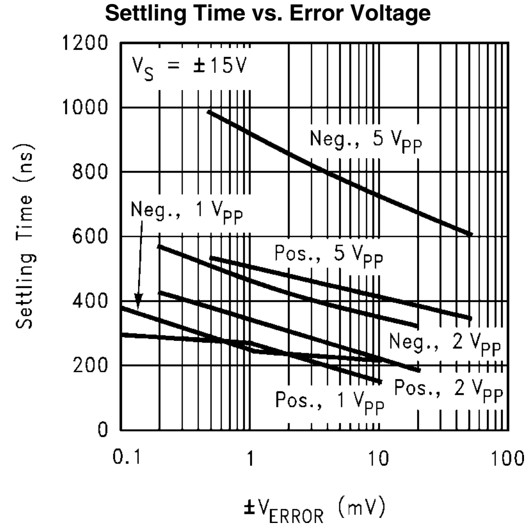
10108450

Settling Time vs. Error Voltage



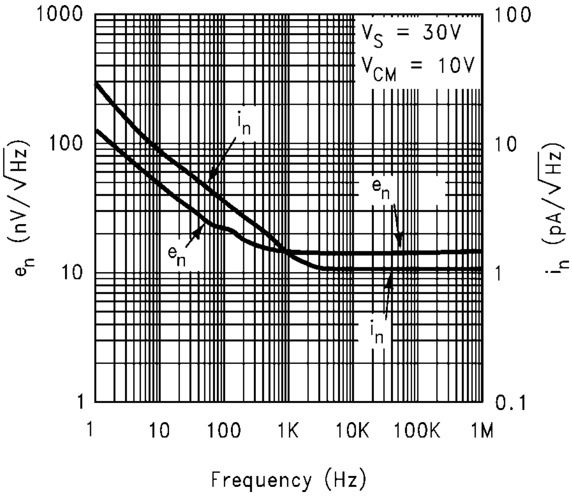
10108443

Settling Time vs. Error Voltage



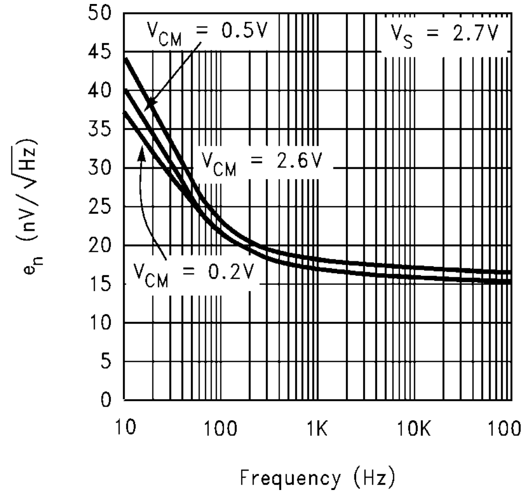
10108442

Input Noise Voltage/Current vs. Frequency



10108415

Input Noise Voltage for Various V_{CM}



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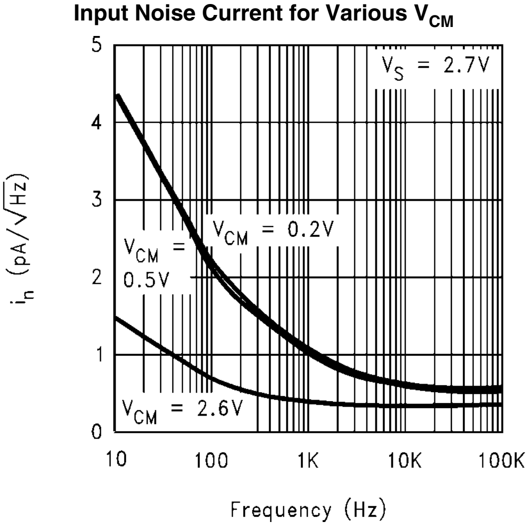
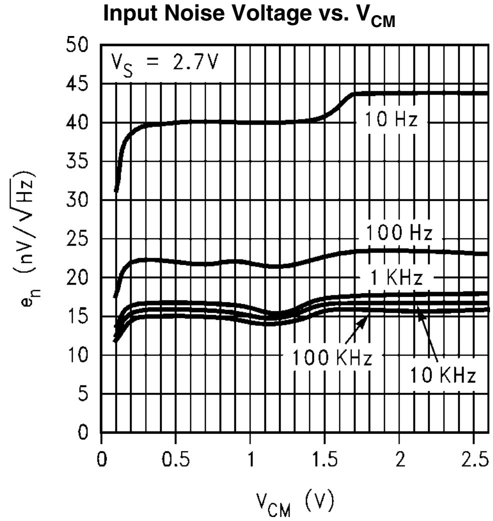
Input Noise Current for Various V_{CM}



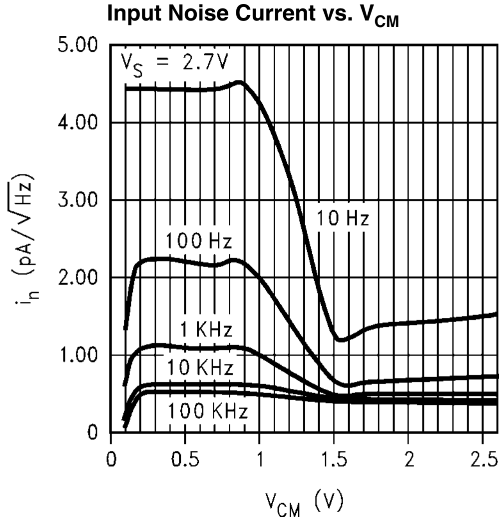
10108412

Input Noise Voltage vs. V_{CM}



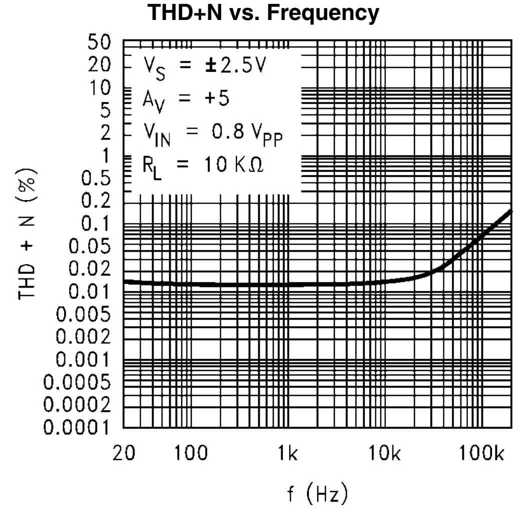
10108455

Input Noise Current vs. V_{CM}



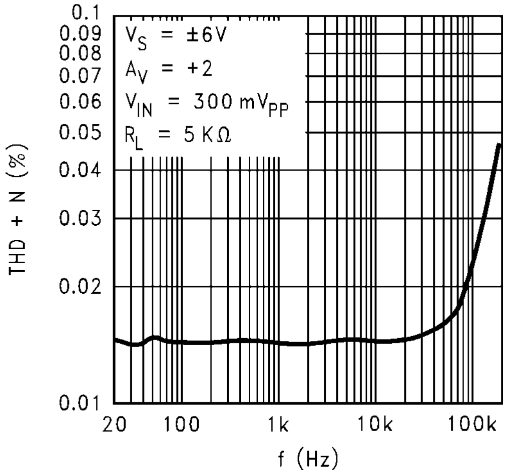
10108454

THD+N vs. Frequency



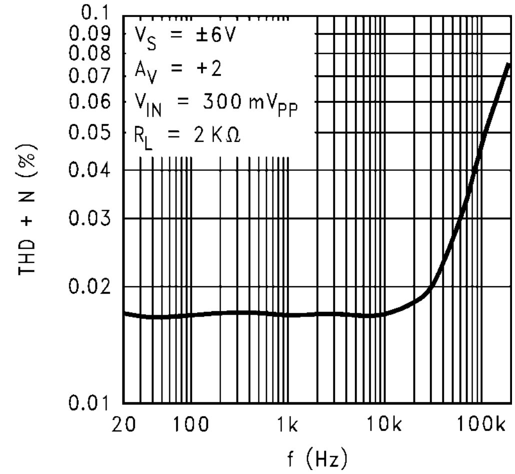
10108423

THD+N vs. Frequency



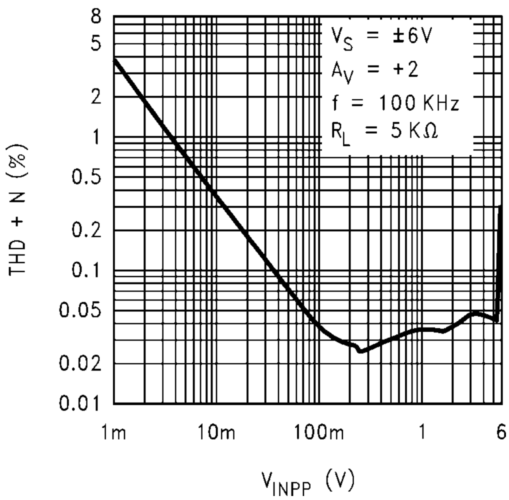
10108422

THD+N vs. Frequency



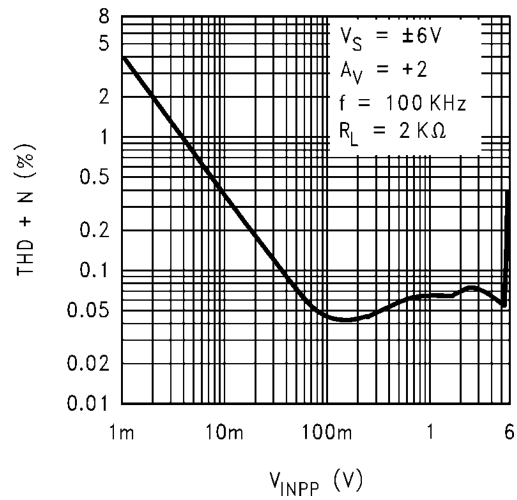
10108421

THD+N vs. Amplitude



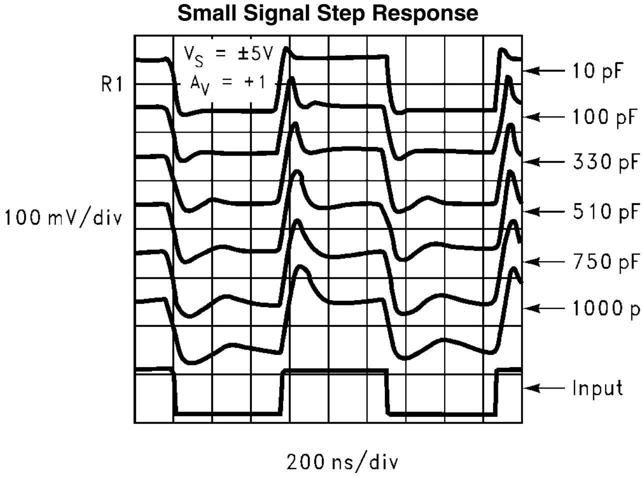
10108419

THD+N vs. Amplitude



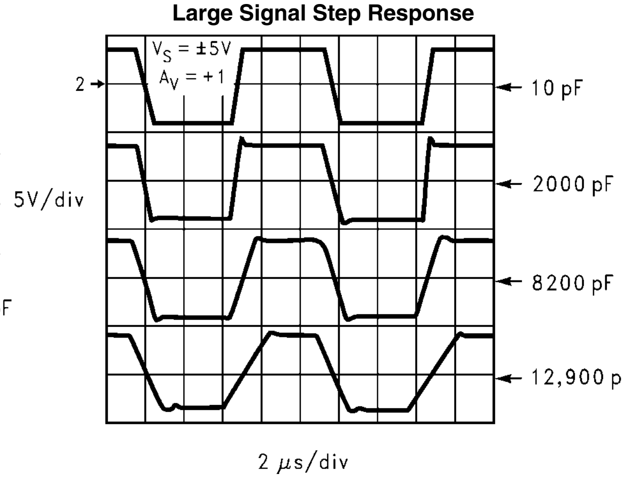
10108420

Small Signal Step Response



10108438

Large Signal Step Response



10108440

Application Hints

BLOCK DIAGRAM AND OPERATIONAL DESCRIPTION

A) Input Stage

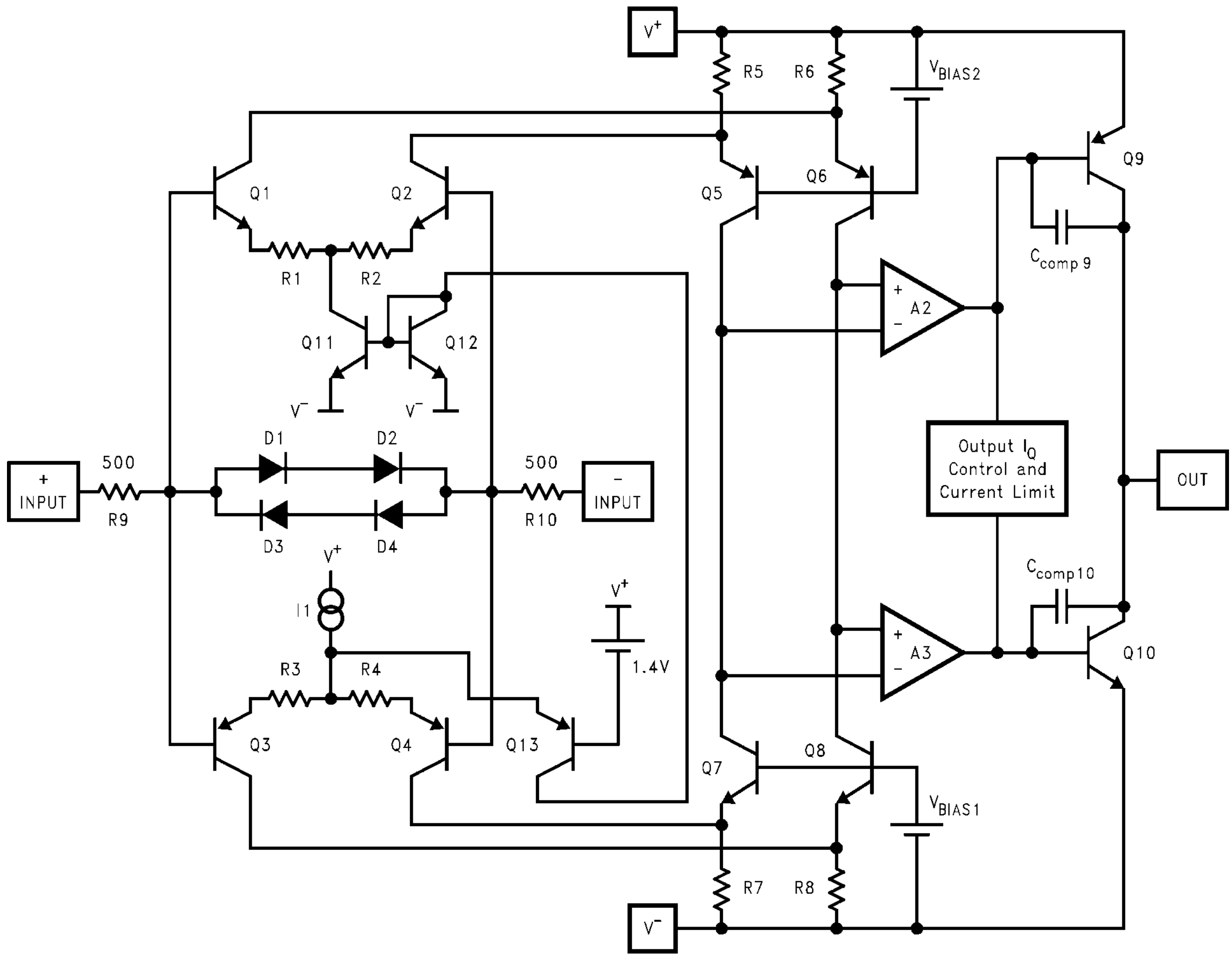


FIGURE 1. Simplified Schematic Diagram

As can be seen from the simplified schematic in *Figure 1*, the input stage consists of two distinct differential pairs (Q1-Q2 and Q3-Q4) in order to accommodate the full Rail-to-Rail input common mode voltage range. The voltage drop across R5, R6, R7, and R8 is kept to less than 200mV in order to allow the input to exceed the supply rails. Q13 acts as a switch to steer current away from Q3-Q4 and into Q1-Q2, as the input increases beyond 1.4V of V+. This in turn shifts the signal path from the bottom stage differential pair to the top one and causes a subsequent increase in the supply current.

In transitioning from one stage to another, certain input stage parameters (V_{OS}, I_b, I_{OS}, e_n, and i_n) are determined based on which differential pair is "on" at the time. Input Bias current, I_B, will change in value and polarity as the input crosses the transition region. In addition, parameters such as PSRR and CMRR which involve the input offset voltage will also be effected by changes in V_{CM} across the differential pair transition region.

The input stage is protected with the combination of R9-R10 and D1, D2, D3, and D4 against differential input over-voltages. This fault condition could otherwise harm the differential pairs or cause offset voltage shift in case of prolonged over voltage. As shown in *Figure 2*, if this voltage reaches approximately ±1.4V at 25°C, the diodes turn on and current flow is limited by the internal series resistors (R9 and R10). The Absolute Maximum Rating of ±10V differential on V_{IN} still needs to be observed. With temperature variation, the point were the diodes turn on will change at the rate of 5mV/°C.

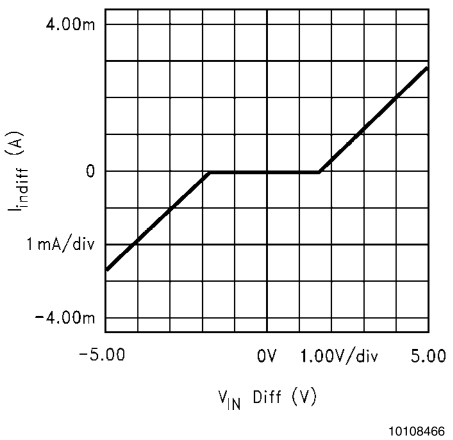


FIGURE 2. Input Stage Current vs. Differential Input Voltage

B) Output Stage

The output stage *Figure 1* is comprised of complementary NPN and PNP common-emitter stages to permit voltage swing to within a $V_{CE(SAT)}$ of either supply rail. Q9 supplies the sourcing and Q10 supplies the sinking current load. Output current limiting is achieved by limiting the V_{CE} of Q9 and Q10; using this approach to current limiting, alleviates the draw back to the conventional scheme which requires one V_{BE} reduction in output swing.

The frequency compensation circuit includes Miller capacitors from collector to base of each output transistor (see *Figure 1*, C_{comp9} and C_{comp10}). At light capacitive loads, the high frequency gain of the output transistors is high, and the Miller effect increases the effective value of the capacitors thereby stabilizing the Op Amp. Large capacitive loads greatly decrease the high frequency gain of the output transistors thus lowering the effective internal Miller capacitance - the internal pole frequency increases at the same time a low frequency pole is created at the Op Amp output due to the large load capacitor. In this fashion, the internal dominant pole compensation, which works by reducing the loop gain to less than 0dB when the phase shift around the feedback loop is more than 180°C, varies with the amount of capacitive load and becomes less dominant when the load capacitor has increased enough. Hence the Op Amp is very stable even at high values of load capacitance resulting in the uncharacteristic feature of stability under all capacitive loads.

DRIVING CAPACITIVE LOADS

The LM8261 is specifically designed to drive unlimited capacitive loads without oscillations (See Settling Time and Percent Overshoot vs. Cap Load plots in the typical performance characteristics section). In addition, the output current handling capability of the device allows for good slewing characteristics even with large capacitive loads (see Slew Rate vs. Cap Load plots). The combination of these features is ideal for applications such as TFT flat panel buffers, A/D converter input amplifiers, etc.

However, as in most Op Amps, addition of a series isolation resistor between the Op Amp and the capacitive load improves the settling and overshoot performance.

Output current drive is an important parameter when driving capacitive loads. This parameter will determine how fast the output voltage can change. Referring to the Slew Rate vs. Cap Load Plots (typical performance characteristics section), two distinct regions can be identified. Below about 10,000pF, the output Slew Rate is solely determined by the Op Amp's compensation capacitor value and available current into that capacitor. Beyond 10nF, the Slew Rate is determined by the Op Amp's available output current. Note that because of the lower output sourcing current compared to the sinking one, the Slew Rate limit under heavy capacitive loading is determined by the positive transitions. An estimate of positive and negative slew rates for loads larger than 100nF can be made by dividing the short circuit current value by the capacitor.

For the LM8261, the available output current increases with the input overdrive. Referring to *Figure 3* and *Figure 4*, Output Short Circuit Current vs. Input Overdrive, it can be seen that both sourcing and sinking short circuit current increase as input overdrive increases. In a closed loop amplifier configuration, during transient conditions while the fed back output has not quite caught up with the input, there will be an overdrive imposed on the input allowing more output current than would normally be available under steady state condition. Because of this feature, the Op Amp's output stage quiescent current can be kept to a minimum, thereby reducing power consumption, while enabling the device to deliver large output current when the need arises (such as during transients).

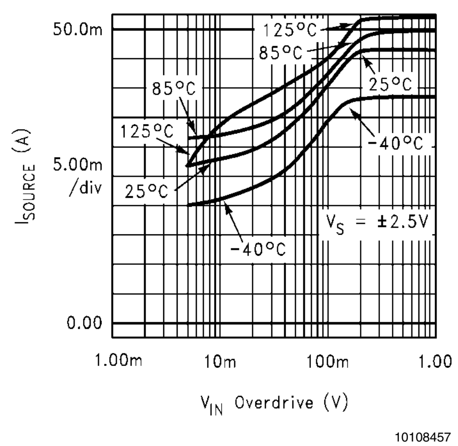


FIGURE 3. Output Short Circuit Sourcing Current vs. Input Overdrive

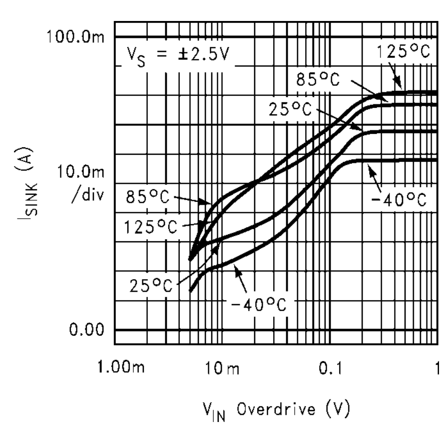


FIGURE 4. Output Short Circuit Sinking Current vs. Input Overdrive

Figure 5 shows the output voltage, output current, and the resulting input overdrive with the device set for A_V = +1 and the input tied to a $1V_{PP}$ step function driving a 47nF capacitor. As can be seen, during the output transition, the input overdrive reaches 1V peak and is more than enough to cause the output current to increase to its maximum value (see *Figure 3* and *Figure 4* plots). Note that because of the larger output sinking current compared to the sourcing one, the output negative transition is faster than the positive one.

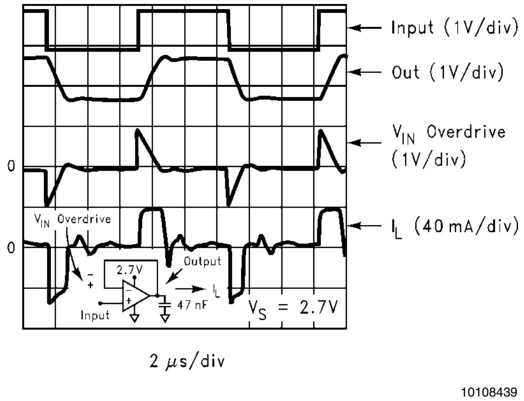


FIGURE 5. Buffer Amplifier scope photo

ESTIMATING THE OUTPUT VOLTAGE SWING

It is important to keep in mind that the steady state output current will be less than the current available when there is an input overdrive present. For steady state conditions, the Output Voltage vs. Output Current plot (Typical Performance Characteristics section) can be used to predict the output swing. *Figure 6* and *Figure 7* show this performance along with several load lines corresponding to loads tied between the output and ground. In each cases, the intersection of the device plot at the appropriate temperature with the load line would be the typical output swing possible for that load. For example, a 1KΩ load can accommodate an output swing to within 250mV of V^- and to 330mV of V^+ (V_S = ±15V) corresponding to a typical $29.3V_{PP}$ unclipped swing.

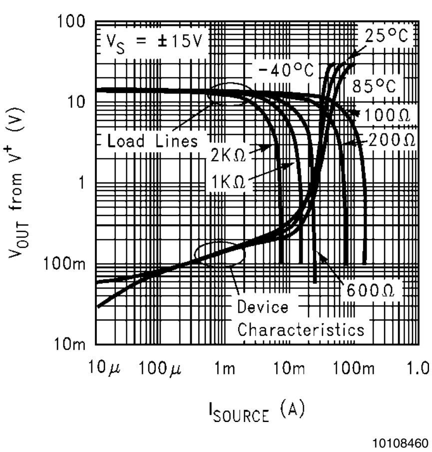


FIGURE 6. Output Sourcing Characteristics with Load Lines

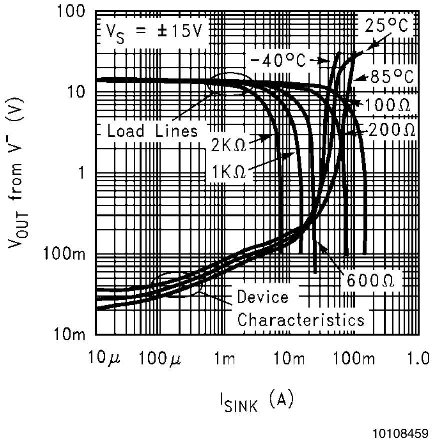


FIGURE 7. Output Sinking Characteristics with Load Lines

TFT APPLICATIONS

Figure 8 below, shows a typical application where the LM8261 is used as a buffer amplifier for the V_{COM} signal employed in a TFT LCD flat panel:

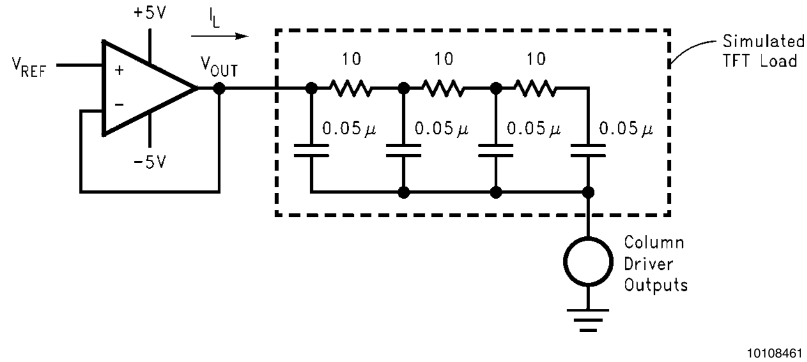


FIGURE 8. V_{COM} Driver Application Schematic

Figure 9 shows the time domain response of the amplifier when used as a V_{COM} buffer/driver with V_{REF} at ground. In this application, the Op Amp loop will try and maintain its output voltage based on the voltage on its non-inverting input (V_{REF}) despite the current injected into the TFT simulated load. As long as this load current is within the range tolerable by the LM8261 (45mA sourcing and 65mA sinking for ±5V supplies), the output will settle to its final value within less than 2μs.

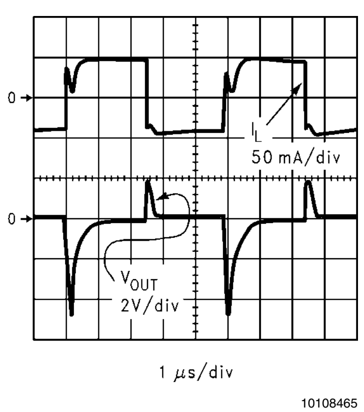


FIGURE 9. V_{COM} driver performance scope photo

OUTPUT SHORT CIRCUIT CURRENT AND DISSIPATION ISSUES

The LM8261 output stage is designed for maximum output current capability. Even though momentary output shorts to ground and either supply can be tolerated at all operating voltages, longer lasting short conditions can cause the junction temperature to rise beyond the absolute maximum rating of the device, especially at higher supply voltage conditions. Below supply voltage of 6V, output short circuit condition can be tolerated indefinitely.

With the Op Amp tied to a load, the device power dissipation consists of the quiescent power due to the supply current flow into the device, in addition to power dissipation due to the load current. The load portion of the power itself could include an average value (due to a DC load current) and an AC component. DC load current would flow if there is an output voltage offset, or the output AC average current is non-zero, or if the Op Amp operates in a single supply application where the output is maintained somewhere in the range of linear operation. Therefore:

$P_{TOTAL} = P_Q + P_{DC} + P_{AC}$

$P_Q = I_S \cdot V_S$ Op Amp Quiescent Power Dissipation

$P_{DC} = I_O \cdot (V_R - V_O)$ DC Load Power

P_{AC} = See Table 1 below AC Load Power

where:

I_S: Supply Current

V_S: Total Supply Voltage ($V^+ - V^-$)

I_O: Average load current

V_O: Average Output Voltage

V_R: V^+ for sourcing and V^- for sinking current

Table 1 below shows the maximum AC component of the load power dissipated by the Op Amp for standard Sinusoidal, Triangular, and Square Waveforms:

TABLE 1. Normalized AC Power Dissipated in the Output Stage for Standard Waveforms

P_{AC} (W.Ω/V²)		
Sinusoidal	Triangular	Square
50.7×10^{-3}	46.9×10^{-3}	62.5×10^{-3}

The table entries are normalized to V_S^2/R_L. To figure out the AC load current component of power dissipation, simply multiply the table entry corresponding to the output waveform by the factor V_S^2/R_L. For example, with ±15V supplies, a 600Ω load, and triangular waveform power dissipation in the output stage is calculated as:

$P_{AC} = (46.9 \times 10^{-3}) \cdot [30^2/600] = 70.4mW$

Other Application Hints

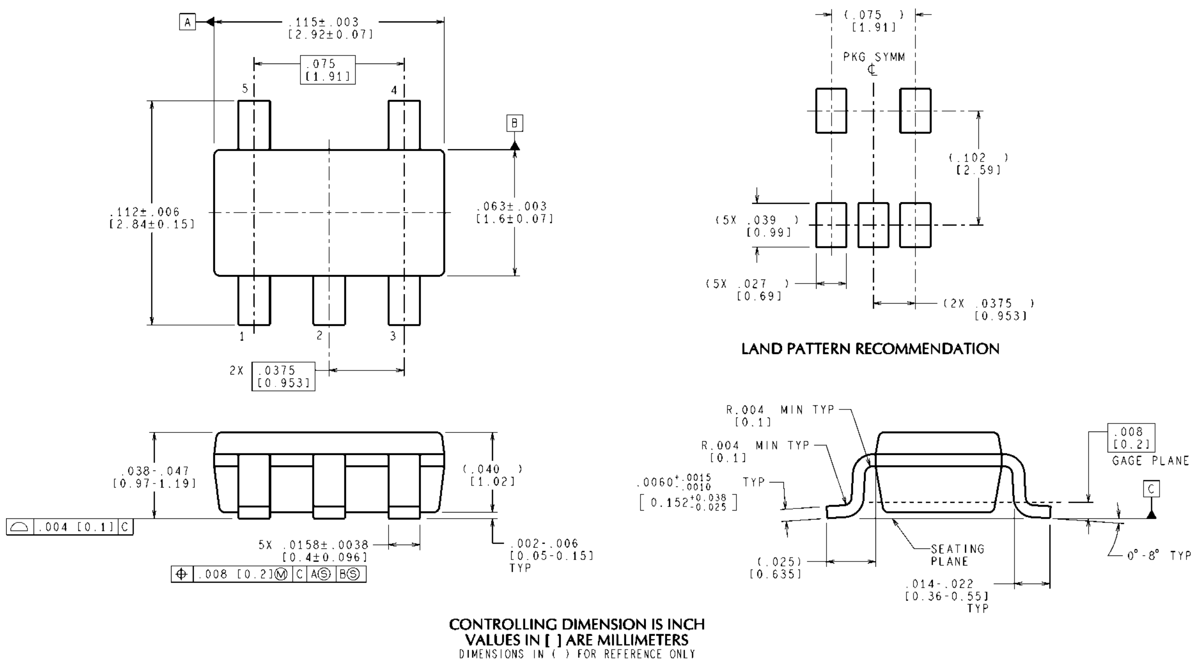
The use of supply decoupling is mandatory in most applications. As with most relatively high speed/high output current Op Amps, best results are achieved when each supply line is decoupled with two capacitors; a small value ceramic capacitor (~0.01μF) placed very close to the supply lead in addition to a large value Tantalum or Aluminum (> 4.7μF). The large capacitor can be shared by more than one device if necessary. The small ceramic capacitor maintains low supply impedance at high frequencies while the large capacitor will act as the charge "bucket" for fast load current spikes at the Op Amp output. The combination of these capacitors will provide supply decoupling and will help keep the Op Amp oscillation free under any load.

LM8261 ADVANTAGES

Compared to other Rail-to-Rail Input/Output devices, the LM8261 offers several advantages such as:

- Improved cross over distortion.
- Nearly constant supply current throughout the output voltage swing range and close to either rail.
- Consistent stability performance for all input/output voltage and current conditions.
- Nearly constant Unity gain frequency (f_u) and Phase Margin (Phi_m) for all operating supplies and load conditions.
- No output phase reversal under input overload condition.

Physical Dimensions inches (millimeters) unless otherwise noted



MF05A (Rev D)

5-Pin SOT23-5
NS Package Number MF05A

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