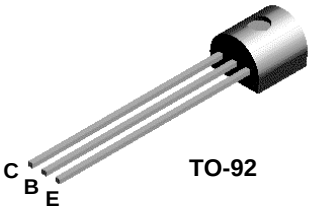
25-05124

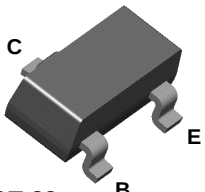
FAIRCHILD SEMICONDUCTOR™

2N3906



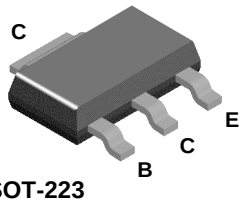
TO-92

MMBT3906



SOT-23
Mark: 2A

PZT3906



SOT-223

PNP General Purpose Amplifier

This device is designed for general purpose amplifier and switching applications at collector currents of 10 µA to 100 mA.

Absolute Maximum Ratings*

T_A = 25°C unless otherwise noted

Symbol	Parameter	Value	Units
V_{CEO}	Collector-Emitter Voltage	40	V
V_{CBO}	Collector-Base Voltage	40	V
V_{EBO}	Emitter-Base Voltage	5.0	V
I_C	Collector Current - Continuous	200	mA
T_J, T_{stg}	Operating and Storage Junction Temperature Range	-55 to +150	°C

*These ratings are limiting values above which the serviceability of any semiconductor device may be impaired.

NOTES:
1) These ratings are based on a maximum junction temperature of 150 degrees C.
2) These are steady state limits. The factory should be consulted on applications involving pulsed or low duty cycle operations.
3) All voltages (V) and currents (A) are negative polarity for PNP transistors.

Thermal Characteristics

T_A = 25°C unless otherwise noted

Symbol	Characteristic	Max			Units
		2N3906	*MMBT3906	**PZT3906	
P_D	Total Device Dissipation Derate above 25°C	625 5.0	350 2.8	1,000 8.0	mW mW/°C
$R_{\theta JC}$	Thermal Resistance, Junction to Case	83.3			°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	200	357	125	°C/W

*Device mounted on FR-4 PCB 1.6" X 1.6" X 0.06."

**Device mounted on FR-4 PCB 36 mm X 18 mm X 1.5 mm; mounting pad for the collector lead min. 6 cm^2.

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PNP General Purpose Amplifier
(continued)

Electrical Characteristics
T_A = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Max	Units
OFF CHARACTERISTICS					
$V_{(BR)CEO}$	Collector-Emitter Breakdown Voltage*	I_C = 1.0 mA, I_B = 0	40		V
$V_{(BR)CBO}$	Collector-Base Breakdown Voltage	I_C = 10 µA, I_E = 0	40		V
$V_{(BR)EBO}$	Emitter-Base Breakdown Voltage	I_E = 10 µA, I_C = 0	5.0		V
I_{BL}	Base Cutoff Current	V_{CE} = 30 V, V_{BE} = 3.0 V		50	nA
I_{CEX}	Collector Cutoff Current	V_{CE} = 30 V, V_{BE} = 3.0 V		50	nA
ON CHARACTERISTICS					
h_{FE}	DC Current Gain *	I_C = 0.1 mA, V_{CE} = 1.0 V I_C = 1.0 mA, V_{CE} = 1.0 V I_C = 10 mA, V_{CE} = 1.0 V I_C = 50 mA, V_{CE} = 1.0 V I_C = 100 mA, V_{CE} = 1.0 V	60 80 100 60 30	300	
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage	I_C = 10 mA, I_B = 1.0 mA I_C = 50 mA, I_B = 5.0 mA		0.25 0.4	V V
$V_{BE(sat)}$	Base-Emitter Saturation Voltage	I_C = 10 mA, I_B = 1.0 mA I_C = 50 mA, I_B = 5.0 mA	0.65	0.85 0.95	V V
SMALL SIGNAL CHARACTERISTICS					
f_T	Current Gain - Bandwidth Product	I_C = 10 mA, V_{CE} = 20 V, f = 100 MHz	250		MHz
C_{obo}	Output Capacitance	V_{CB} = 5.0 V, I_E = 0, f = 100 kHz		4.5	pF
C_{ibo}	Input Capacitance	V_{EB} = 0.5 V, I_C = 0, f = 100 kHz		10.0	pF
NF	Noise Figure	I_C = 100 µA, V_{CE} = 5.0 V, R_S =1.0kΩ,f=10 Hz to 15.7 kHz		4.0	dB
SWITCHING CHARACTERISTICS					
t_d	Delay Time	V_{CC} = 3.0 V, V_{BE} = 0.5 V, I_C = 10 mA, I_{B1} = 1.0 mA		35	ns
t_r	Rise Time			35	ns
t_s	Storage Time	V_{CC} = 3.0 V, I_C = 10mA I_{B1} = I_{B2} = 1.0 mA		225	ns
t_f	Fall Time			75	ns

*Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2.0%

NOTE: All voltages (V) and currents (A) are negative polarity for PNP transistors.

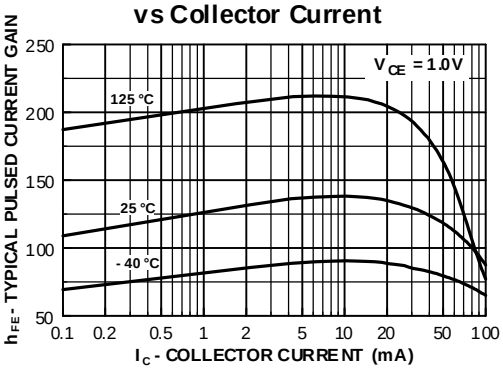
Spice Model

PNP (Is=1.41f Xti=3 Eg=1.11 Vaf=18.7 Bf=180.7 Ne=1.5 Ise=0 Ikf=80m Xtb=1.5 Br=4.977 Nc=2 Isc=0 Ikr=0 Rc=2.5 Cjc=9.728p Mjc=.5776 Vjc=.75 Fc=.5 Cje=8.063p Mje=.3677 Vje=.75 Tr=33.42n Tf=179.3p Itf=.4 Vtf=4 Xtf=6 Rb=10)

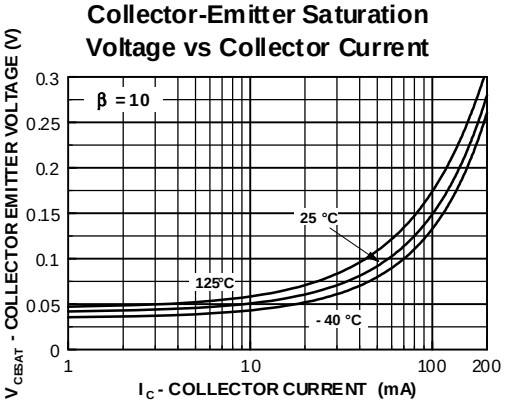
PNP General Purpose Amplifier
(continued)

Typical Characteristics

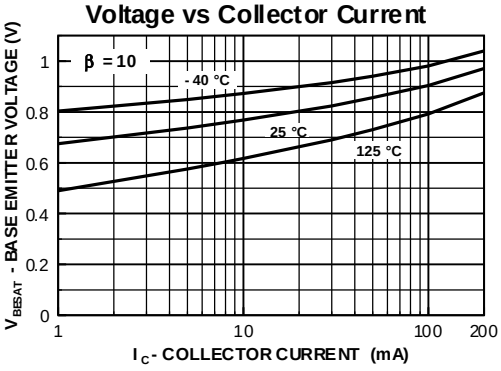
Typical Pulsed Current Gain vs Collector Current



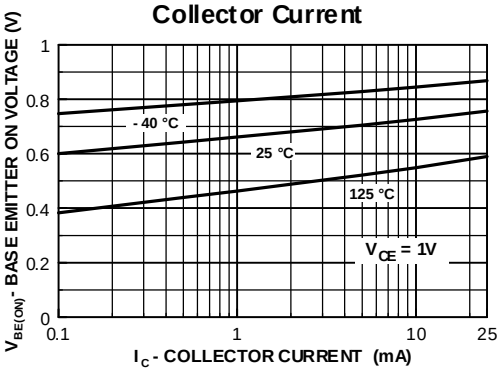
Collector-Emitter Saturation Voltage vs Collector Current



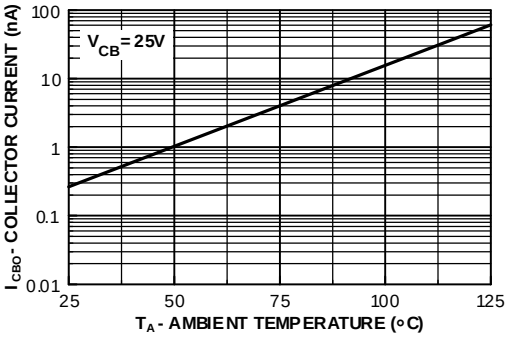
Base-Emitter Saturation Voltage vs Collector Current



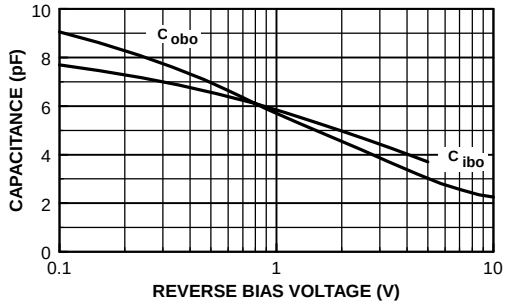
Base Emitter ON Voltage vs Collector Current



Collector-Cutoff Current vs Ambient Temperature

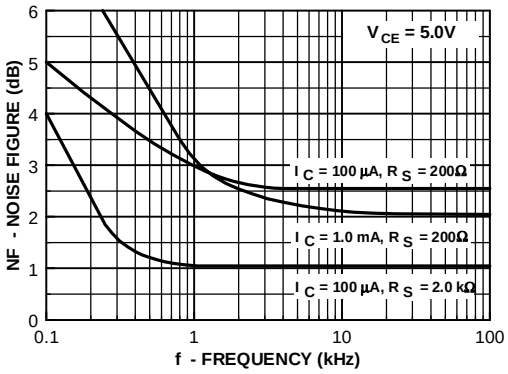


Common-Base Open Circuit Input and Output Capacitance vs Reverse Bias Voltage

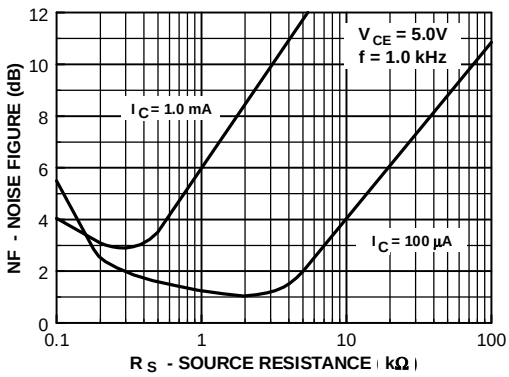


Typical Characteristics (continued)

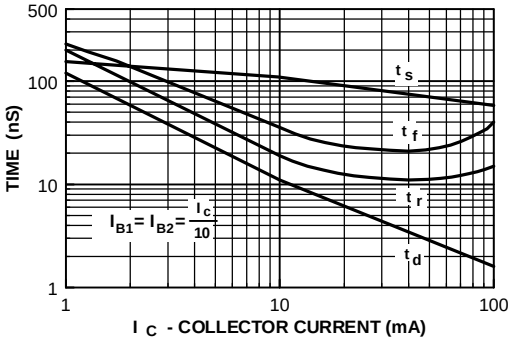
Noise Figure vs Frequency



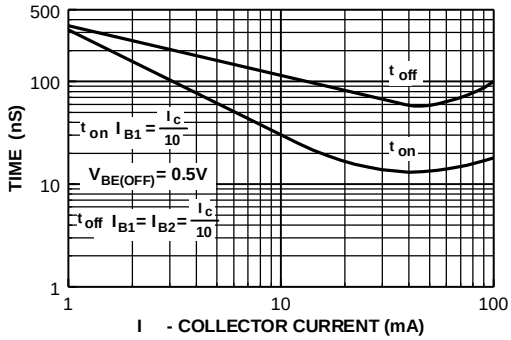
Noise Figure vs Source Resistance



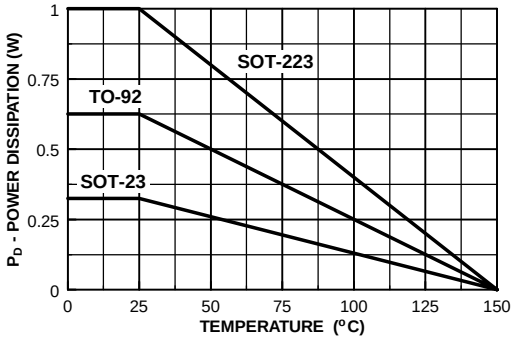
Switching Times vs Collector Current



Turn On and Turn Off Times vs Collector Current

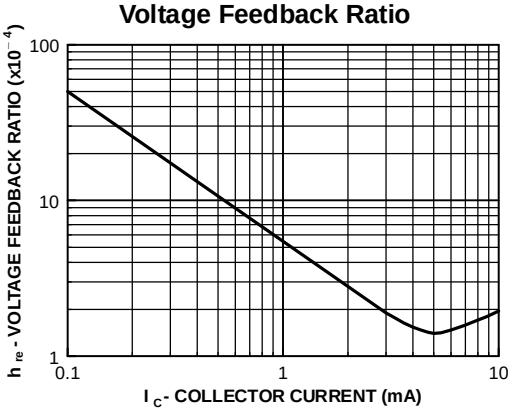


Power Dissipation vs Ambient Temperature

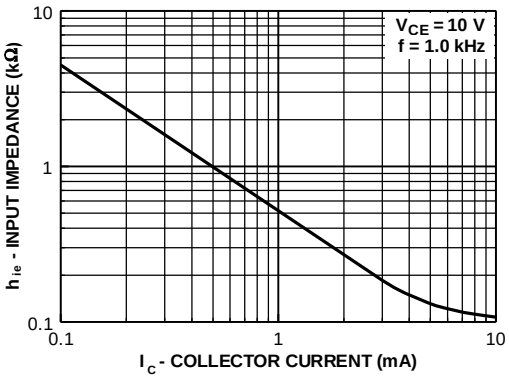


Typical Characteristics (continued)

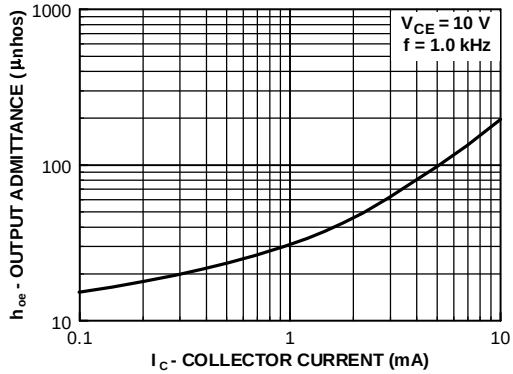
Voltage Feedback Ratio



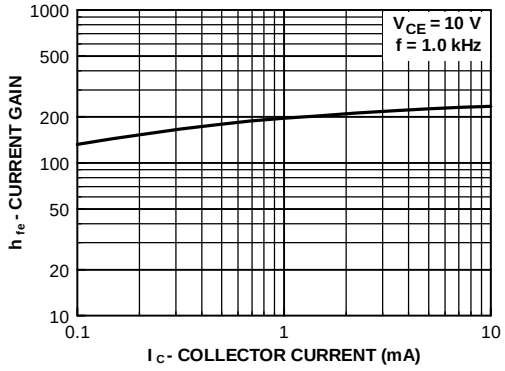
Input Impedance



Output Admittance



Current Gain



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PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
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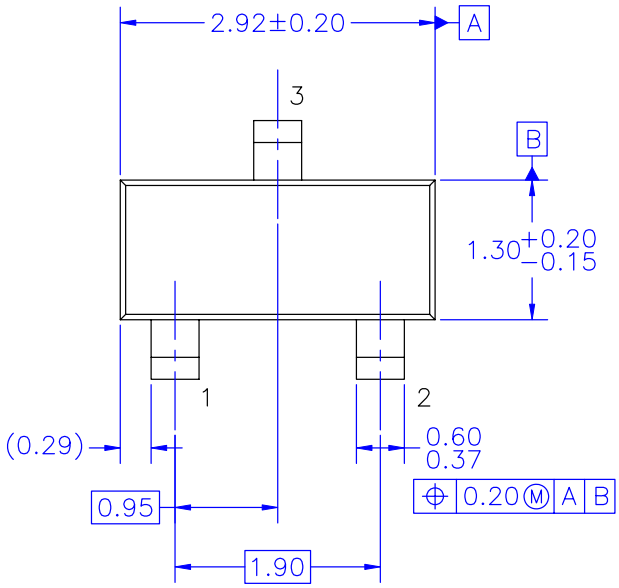
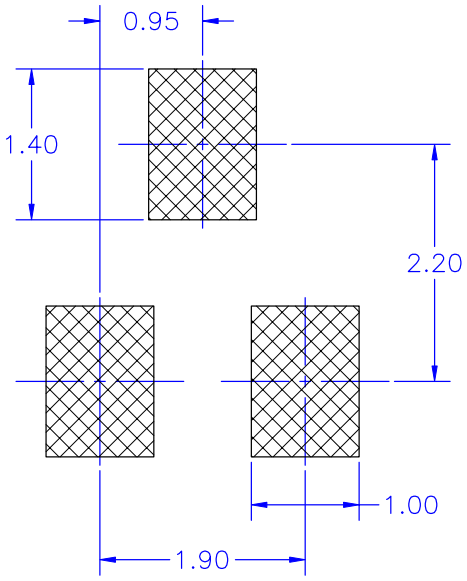
APPROVED
October 10, 2008

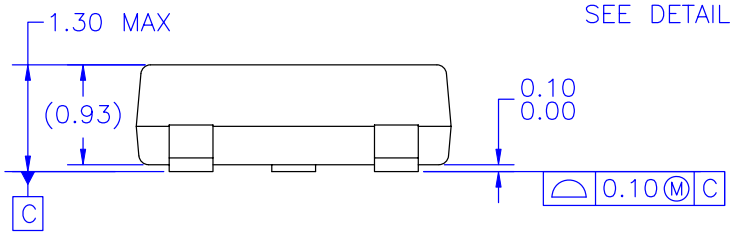
REVISIONS

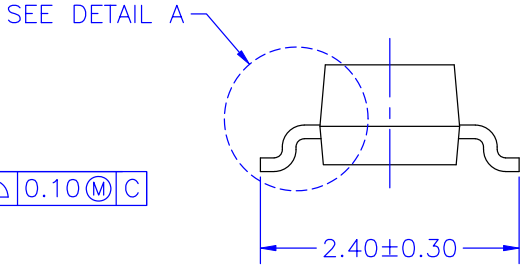
LTR	DESCRIPTION	DATE	NAME/SITE
F	REVISE & REDRAW PER CURRENT STDA; ADD LAND PATTERN	NOV.30,1995	TL
G	ADD 0.004 [0.10] COPLANARITY; NOTE 1: 200 WAS 150; 5.08 WAS 3.81.	FEB.23,1998	MS
H	CHG DWG TEMPL FR NSC TO FSC; CHG DIM STD FR DUAL TO SINGLE; CHG PKG LEN DIM FR 2.92+/-0.13 TO 2.92+/-0.20; CHG PKG WID FR 1.30+/-0.10 TO 1.30+0.20/-0.15; CHG TOT PKG THIC FR 0.88-1.08 TO 1.30 MAX; CHG PROFILE FR 0.013-0.103 TO 0.00-0.10; CHG LD THIC FR 0.13+/-0.05 TO 0.08-0.23; CHG LD WID FR 0.445+/-0.064 TO 0.37-0.60; CHG LD PITCH FR 0.953+/-0.064 TO 0.95 BSC; CHG TOT LD PITCH FR 1.91+/-0.13 TO 1.90 BSC; CHG LAND PATTERN DIM FR 0.762 TYP TO 1.00, FR 0.762 TYP TO 1.40, FR 2.286 TYP TO 2.20; ADDED DIM (0.29); CHG NOTE A FR "STD LD FINISH SPEC" TO "JEDEC REF"; CHG NOTE B FR "JEDEC REF" TO "DIM REF"; ADDED NOTE C&D; ADD LD POS TOL	12AUG2003	MRG
9	CHG DRW NO FR MKT-M03B TO MKT-MA03D.	28 JULY 2008	MRG/CB

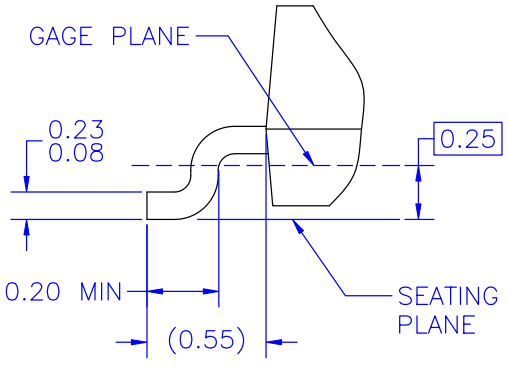




LAND PATTERN RECOMMENDATION







DETAIL A
SCALE: 2X

NOTES: UNLESS OTHERWISE SPECIFIED

A) REFERENCE JEDEC REGISTRATION TO-236, VARIATION AB, ISSUE H.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS ARE INCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR EXTRUSIONS.
D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M - 1994.
E) DRAWING FILE NAME: MA03DREV9

APPROVALS	DATE
DRAWN: J.U. COMPARATIVO JR.	07AUG2008
CHECKED: L. GALERA	
APPROVED: M. GESTOLE	
G.S. BAJE	

FAIRCHILD SEMICONDUCTOR TM

3LD, SOT23, JEDEC TO-236, LOW PROFILE

PROJECTION	SCALE	SIZE	DRAWING NUMBER	REV
INCH [MM]	1:1	NA	MKT-MA03D	9

FORMERLY: N/A | SHEET : 1 OF 1