25-05121

FAIRCHILD SEMICONDUCTOR TM

October 1997

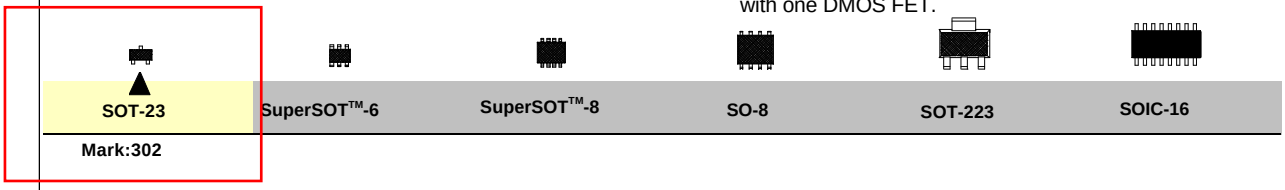
FDV302P
Digital FET, P-Channel

General Description

This P-Channel logic level enhancement mode field effect transistor is produced using Fairchild's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance. This device has been designed especially for low voltage applications as a replacement for digital transistors. Since bias resistors are not required, this one P-channel FET can replace several digital transistors with different bias resistors such as the DTCx and DCDx series.

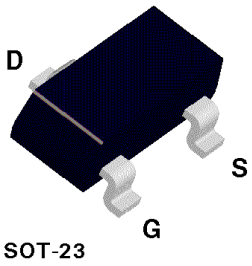
Features

- -25 V, -0.12 A continuous, -0.5 A Peak.
  $R_{DS(ON)}$ = 13 Ω @ V_{GS}= -2.7 V
  $R_{DS(ON)}$ = 10 Ω @ V_{GS} = -4.5 V.
- Very low level gate drive requirements allowing direct operation in 3V circuits. $V_{GS(th)}$ < 1.5V.
- Gate-Source Zener for ESD ruggedness. >6kV Human Body Model
- Compact industry standard SOT-23 surface mount package.
- Replace many PNP digital transistors (DTCx and DCDx) with one DMOS FET.

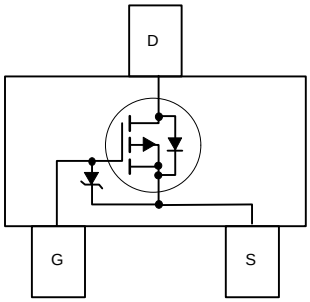


SOT-23 | SuperSOT™-6 | SuperSOT™-8 | SO-8 | SOT-223 | SOIC-16

Mark:302



SOT-23



Absolute Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter	FDV302P	Units
V_{DSS}	Drain-Source Voltage	-25	V
V_{GSS}	Gate-Source Voltage	-8	V
I_D	Drain Current - Continuous	-0.12	A
	- Pulsed	-0.5	
P_D	Maximum Power Dissipation	0.35	W
T_J,T_{STG}	Operating and Storage Temperature Range	-55 to 150	°C
ESD	Electrostatic Discharge Rating MIL-STD-883D Human Body Model (100pf / 1500 Ohm)	6.0	kV
THERMAL CHARACTERISTICS			
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	357	°C/W

Electrical Characteristics (T_A = 25 °C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = -250 µA	-25			V
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	I_D = -250 µA, Referenced to 25 °C		-20		mV /°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = -20 V, V_{GS} = 0 V			-1	µA
		T_J = 55°C			-10	µA
I_{GSS}	Gate - Body Leakage Current	V_{GS} = -8 V, V_{DS} = 0 V			-100	nA
ON CHARACTERISTICS (Note)						
$\Delta V_{GS(th)}/\Delta T_J$	Gate Threshold Voltage Temp. Coefficient	I_D = -250 µA, Referenced to 25 °C		1.9		mV /°C
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = -250 µA	-0.65	-1	-1.5	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = -2.7 V, I_D = -0.05 A		10.6	13	Ω
		V_{GS} = -4.5 V, I_D = -0.2 A		7.9	10	
		T_J =125°C		12	18	
$I_{D(ON)}$	On-State Drain Current	V_{GS} = -2.7 V, V_{DS} = -5 V	-0.05			A
g_{FS}	Forward Transconductance	V_{DS} = -5 V, I_D = -0.2 A		0.135		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = -10 V, V_{GS} = 0 V, f = 1.0 MHz		11		pF
C_{oss}	Output Capacitance			7		pF
C_{rss}	Reverse Transfer Capacitance			1.4		pF
SWITCHING CHARACTERISTICS (Note)						
$t_{D(on)}$	Turn - On Delay Time	V_{DD} = -6 V, I_D = -0.2 A, V_{GS} = -4.5 V, R_{GEN} = 50 Ω		5	12	ns
t_r	Turn - On Rise Time			8	16	ns
$t_{D(off)}$	Turn - Off Delay Time			9	18	ns
t_f	Turn - Off Fall Time			5	10	ns
Q_g	Total Gate Charge	V_{DS} = -5 V, I_D = -0.2 A, V_{GS} = -4.5 V		0.22	0.31	nC
Q_{gs}	Gate-Source Charge			0.11		nC
Q_{gd}	Gate-Drain Charge			0.04		nC
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
I_S	Maximum Continuous Drain-Source Diode Forward Current				-0.2	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = -0.2 A (Note)		-1	-1.5	V

Note:
Pulse Test: Pulse Width ≤ 300µs, Duty Cycle ≤ 2.0%.

Typical Electrical Characteristics

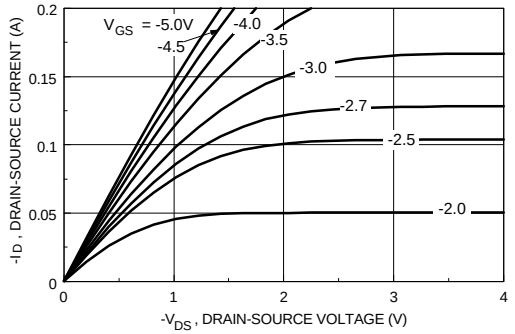


Figure 1. On-Region Characteristics.

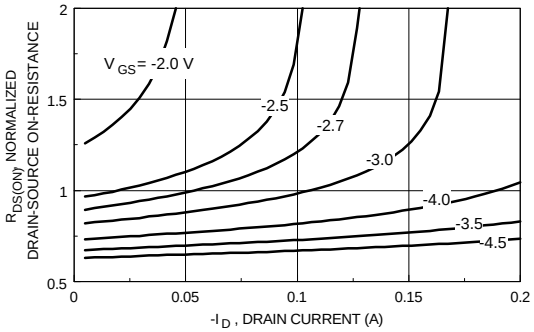


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

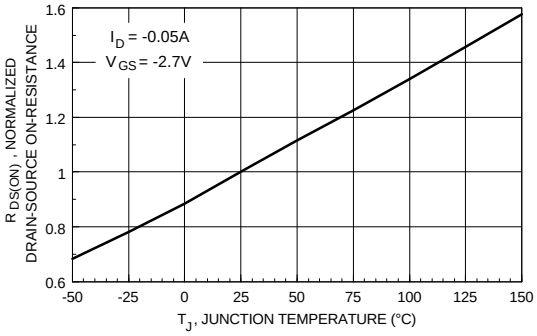


Figure 3. On-Resistance Variation with Temperature.

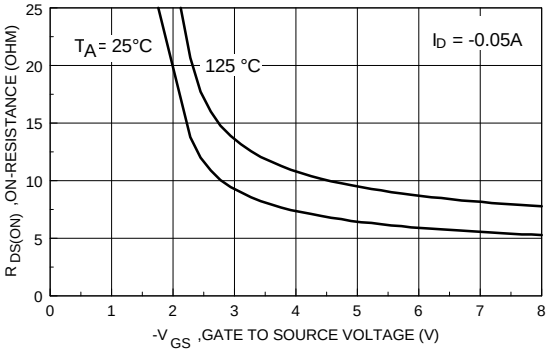


Figure 4. On Resistance Variation with Gate-To- Source Voltage.

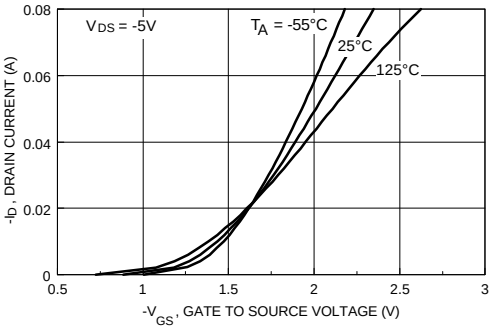


Figure 5. Transfer Characteristics.

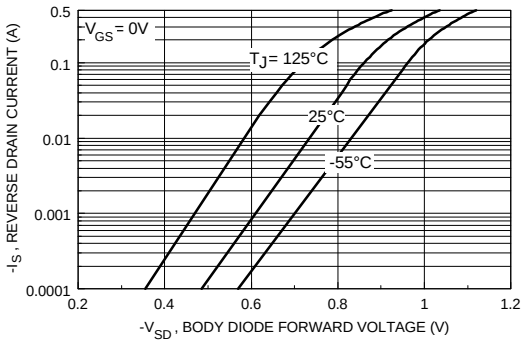


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Electrical And Thermal Characteristics

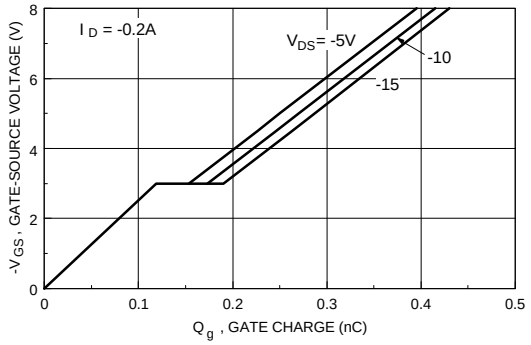


Figure 7. Gate Charge Characteristics.

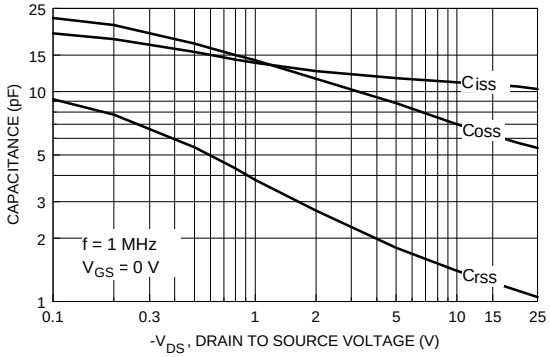


Figure 8. Capacitance Characteristics.

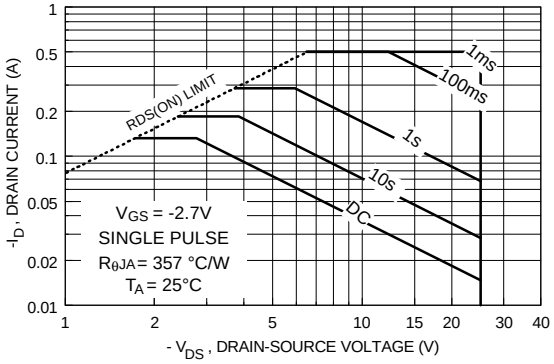


Figure 9. Maximum Safe Operating Area.

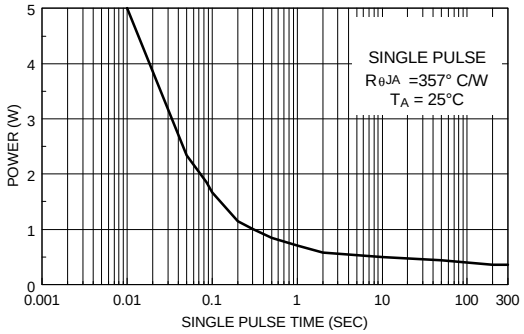


Figure 10. Single Pulse Maximum Power Dissipation.

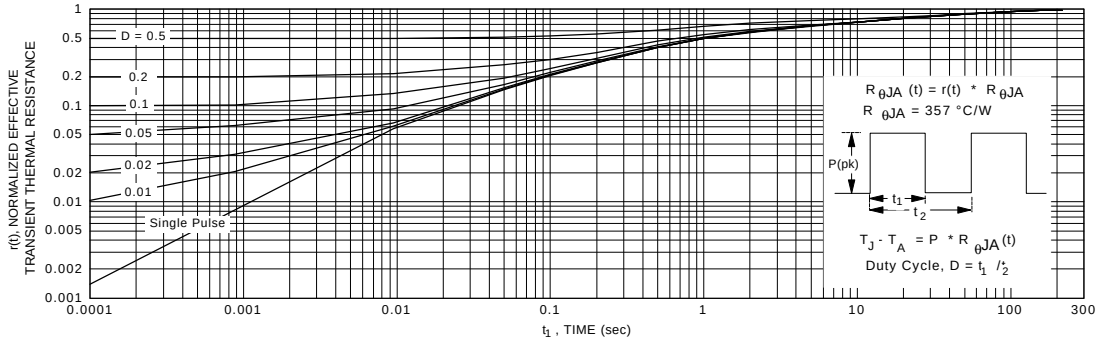
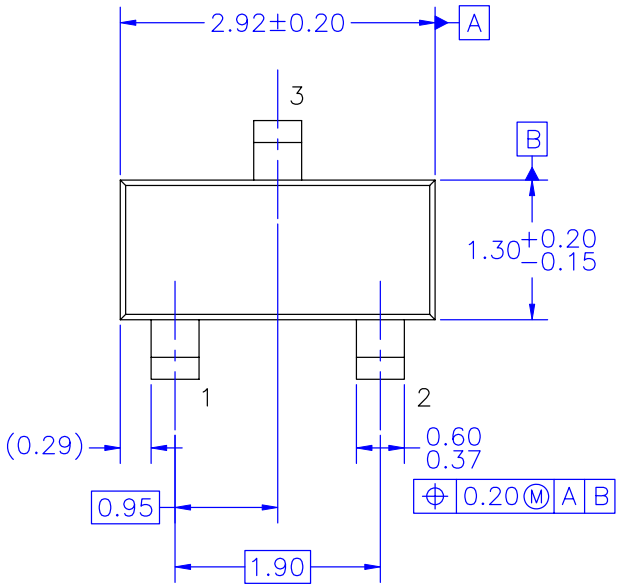


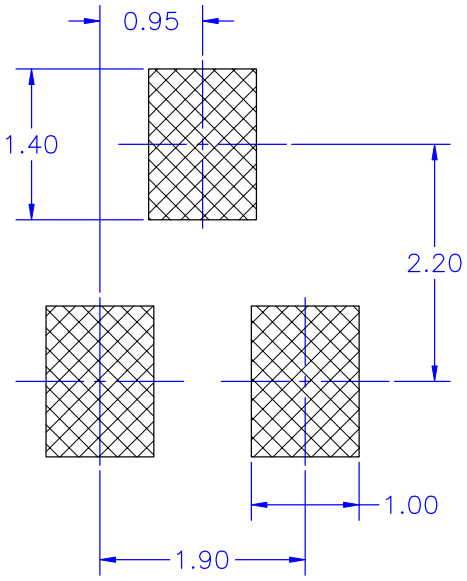
Figure 11. Transient Thermal Response Curve.

APPROVED
October 10, 2008

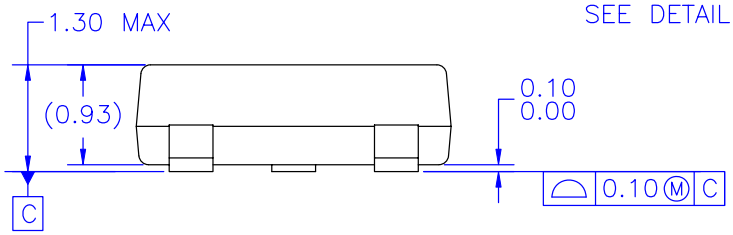
REVISIONS

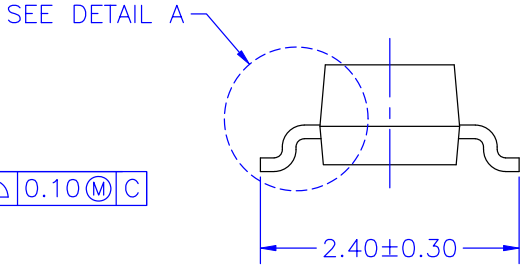
LTR	DESCRIPTION	DATE	NAME/SITE
F	REVISE & REDRAW PER CURRENT STDA; ADD LAND PATTERN	NOV.30,1995	TL
G	ADD 0.004 [0.10] COPLANARITY; NOTE 1: 200 WAS 150; 5.08 WAS 3.81.	FEB.23,1998	MS
H	CHG DWG TEMPL FR NSC TO FSC; CHG DIM STD FR DUAL TO SINGLE; CHG PKG LEN DIM FR 2.92+/-0.13 TO 2.92+/-0.20; CHG PKG WID FR 1.30+/-0.10 TO 1.30+0.20/-0.15; CHG TOT PKG THIC FR 0.88-1.08 TO 1.30 MAX; CHG PROFILE FR 0.013-0.103 TO 0.00-0.10; CHG LD THIC FR 0.13+/-0.05 TO 0.08-0.23; CHG LD WID FR 0.445+/-0.064 TO 0.37-0.60; CHG LD PITCH FR 0.953+/-0.064 TO 0.95 BSC; CHG TOT LD PITCH FR 1.91+/-0.13 TO 1.90 BSC; CHG LAND PATTERN DIM FR 0.762 TYP TO 1.00, FR 0.762 TYP TO 1.40, FR 2.286 TYP TO 2.20; ADDED DIM (0.29); CHG NOTE A FR "STD LD FINISH SPEC" TO "JEDEC REF"; CHG NOTE B FR "JEDEC REF" TO "DIM REF"; ADDED NOTE C&D; ADD LD POS TOL	12AUG2003	MRG
9	CHG DRW NO FR MKT-M03B TO MKT-MA03D.	28 JULY 2008	MRG/CB

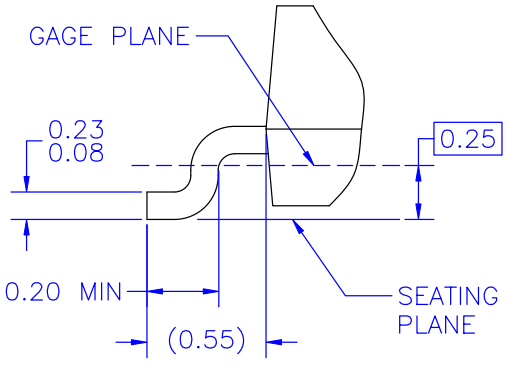




LAND PATTERN RECOMMENDATION







DETAIL A
SCALE: 2X

NOTES: UNLESS OTHERWISE SPECIFIED

A) REFERENCE JEDEC REGISTRATION TO-236, VARIATION AB, ISSUE H.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS ARE INCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR EXTRUSIONS.
D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M - 1994.
E) DRAWING FILE NAME: MA03DREV9

APPROVALS	DATE
DRAWN: J.U. COMPARATIVO JR.	07AUG2008
CHECKED: L. GALERA	
APPROVED: M. GESTOLE	
G.S. BAJE	

FAIRCHILD SEMICONDUCTOR TM

3LD, SOT23, JEDEC TO-236, LOW PROFILE

PROJECTION	SCALE	SIZE	DRAWING NUMBER	REV
INCH [MM]	1:1	NA	MKT-MA03D	9

FORMERLY: N/A | SHEET : 1 OF 1