25-05120

P-Channel 20-V (D-S) MOSFET

PRODUCT SUMMARY

V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)
- 20	0.039 at V_{GS} = - 4.5 V	- 4.7
	0.052 at V_{GS} = - 2.5 V	- 4.1
	0.068 at V_{GS} = - 1.8 V	- 3.5

FEATURES

- **Halogen-free According to IEC 61249-2-21 Available**
- TrenchFET® Power MOSFET

Pb-free Available

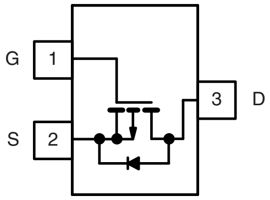
RoHS* COMPLIANT

HALOGEN FREE Available

APPLICATIONS

- Load Switch
- PA Switch

TO-236
(SOT-23)



Top View

Si2323DS (D3)*

* Marking Code

See Little Foot footprint below.

Ordering Information: Si2323DS-T1
Si2323DS-T1-E3 (Lead (Pb)-free)
Si2323DS-T1-GE3 (Lead (Pb)-free and Halogen-free)

ABSOLUTE MAXIMUM RATINGS T_A = 25 °C, unless otherwise noted

Parameter		Symbol	5 s	Steady State	Unit
Drain-Source Voltage		V_{DS}	- 20		V
Gate-Source Voltage		V_{GS}	± 8		
Continuous Drain Current (T_J = 150 °C)[a, b]	T_A = 25 °C	I_D	- 4.7	- 3.7	A
	T_A = 70 °C		- 3.8	- 2.9	
Pulsed Drain Current		I_{DM}	- 20		
Continuous Source Current (Diode Conduction)[a, b]		I_S	- 1.0	- 0.6	
Maximum Power Dissipation[a, b]	T_A = 25 °C	P_D	1.25	0.75	W
	T_A = 70 °C		0.8	0.48	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	- 55 to 150		°C

THERMAL RESISTANCE RATINGS

Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient[a]	t ≤ 5 s	R_{thJA}	75	100	°C/W
	Steady State		120	166	
Maximum Junction-to-Foot (Drain)	Steady State	R_{thJF}	40	50	

Notes:
a. Surface Mounted on 1" x 1" FR4 board.
b. Pulse width limited by maximum junction temperature.

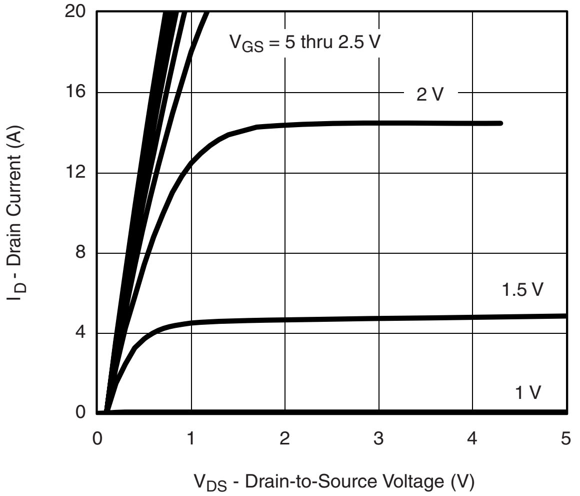
* Pb containing terminations are not RoHS compliant, exemptions may apply.

SPECIFICATIONS T_J = 25 °C, unless otherwise noted

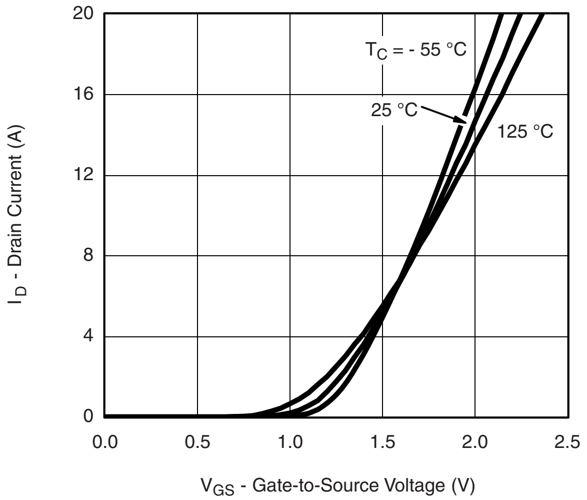
Parameter	Symbol	Test Conditions	Limits			Unit
			Min.	Typ.	Max.	
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = - 250 µA	- 20			V
Gate-Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = - 250 µA	- 0.40		- 1.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 8 V			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = - 16 V, V_{GS} = 0 V			- 1	µA
		V_{DS} = - 16 V, V_{GS} = 0 V, T_J = 55 °C			- 10	
On-State Drain Current[a]	$I_{D(on)}$	$V_{DS} \leq$ - 5 V, V_{GS} = - 4.5 V	- 20			A
Drain-Source On-Resistance[a]	$R_{DS(on)}$	V_{GS} = - 4.5 V, I_D = - 4.7 A		0.031	0.039	Ω
		V_{GS} = - 2.5 V, I_D = - 4.1 A		0.041	0.052	
		V_{GS} = - 1.8 V, I_D = - 2.0 A		0.054	0.068	
Forward Transconductance[a]	g_{fs}	V_{DS} = - 5 V, I_D = - 4.7 A		16		S
Diode Forward Voltage	V_{SD}	I_S = - 1.0 A, V_{GS} = 0 V		- 0.7	- 1.2	V
Dynamic[b]						
Total Gate Charge	Q_g	V_{DS} = - 10 V, V_{GS} = - 4.5 V $I_D \cong$ - 4.7 A		12.5	19	nC
Gate-Source Charge	Q_{gs}			1.7		
Gate-Drain Charge	Q_{gd}			3.3		
Input Capacitance	C_{iss}	V_{DS} = - 10 V, V_{GS} = 0 V, f = 1 MHz		1020		pF
Output Capacitance	C_{oss}			191		
Reverse Transfer Capacitance	C_{rss}			140		
Switching[c]						
Turn-On Time	$t_{d(on)}$	V_{DD} = - 10 V, R_L = 10 Ω $I_D \cong$ - 1.0 A, V_{GEN} = - 4.5 V R_G = 6 Ω		25	40	ns
	t_r			43	65	
Turn-Off Time	$t_{d(off)}$			71	110	
	t_f			48	75	

Notes:
a. Pulse test: PW ≤ 300 µs, duty cycle ≤ 2 %.
b. For DESIGN AID ONLY, not subject to production testing.
c. Switching time is essentially independent of operating temperature.

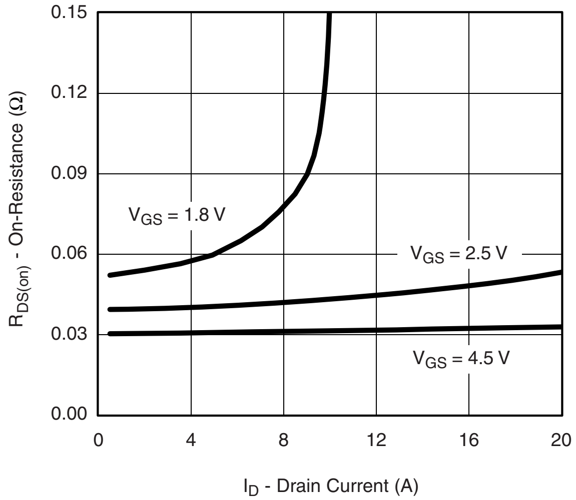
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



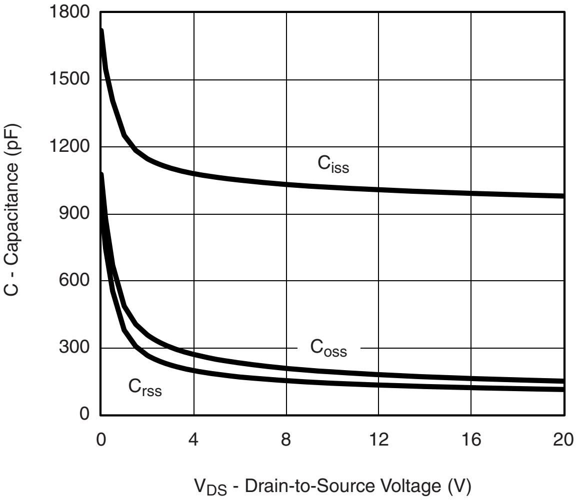
Output Characteristics



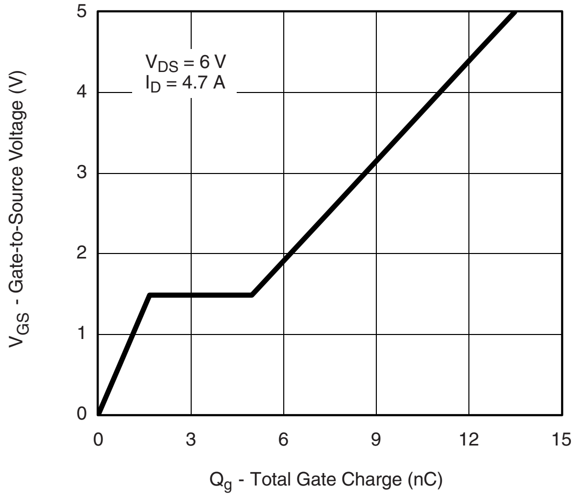
Transfer Characteristics



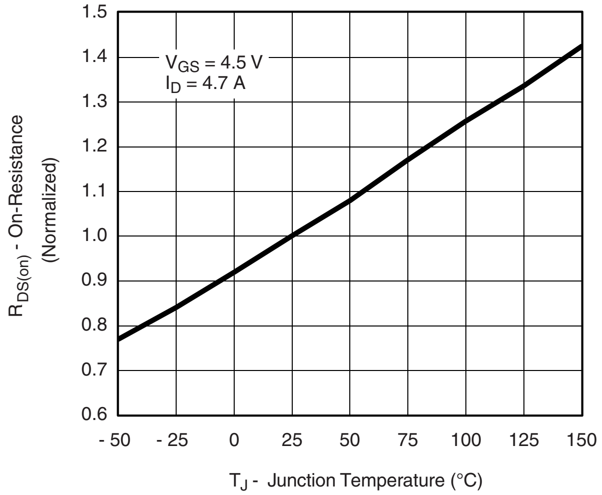
On-Resistance vs. Drain Current



Capacitance

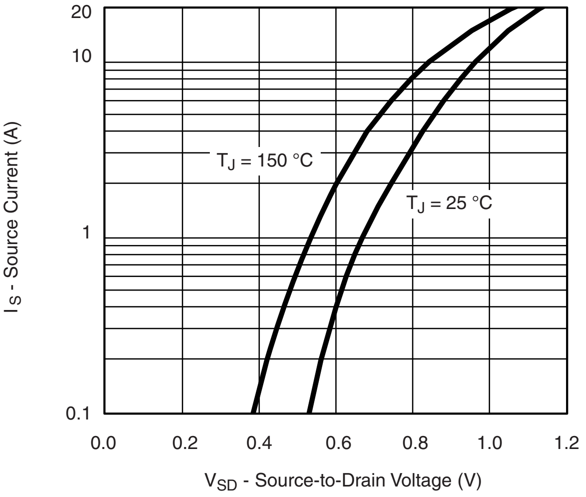


Gate Charge

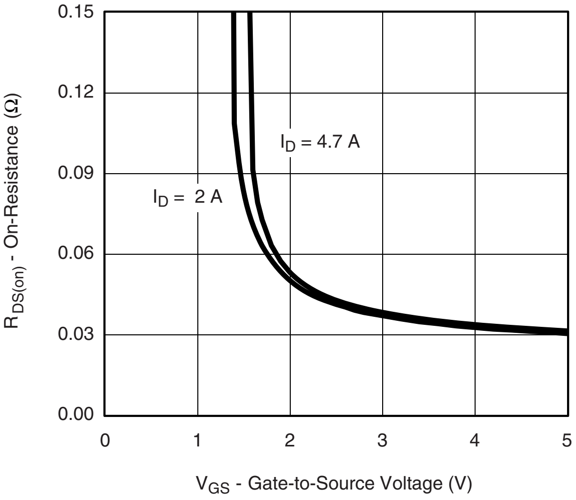


On-Resistance vs. Junction Temperature

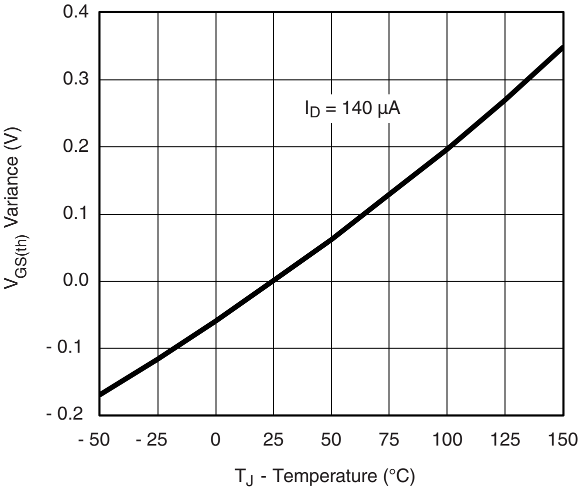
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



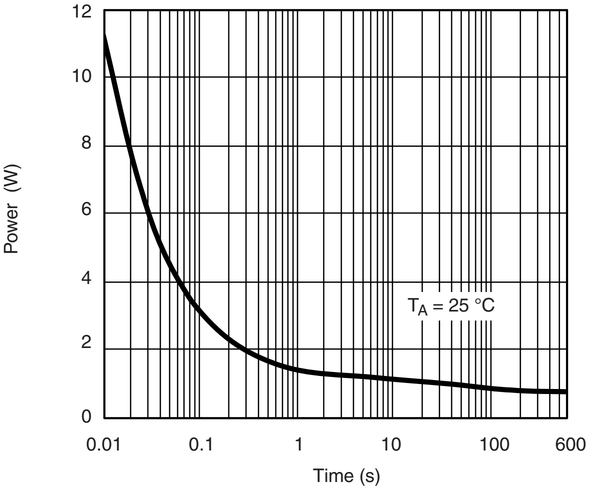
Source-Drain Diode Forward Voltage



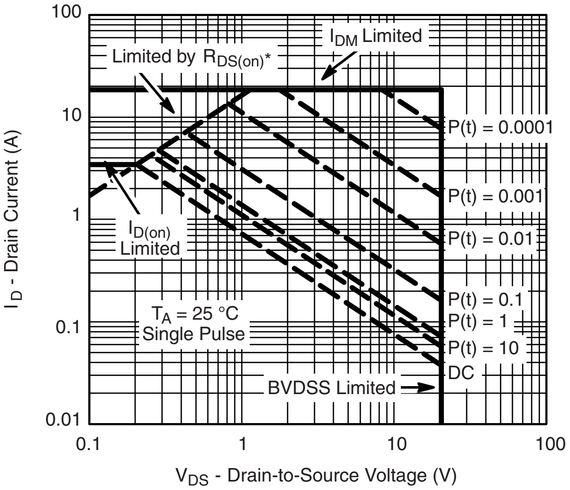
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



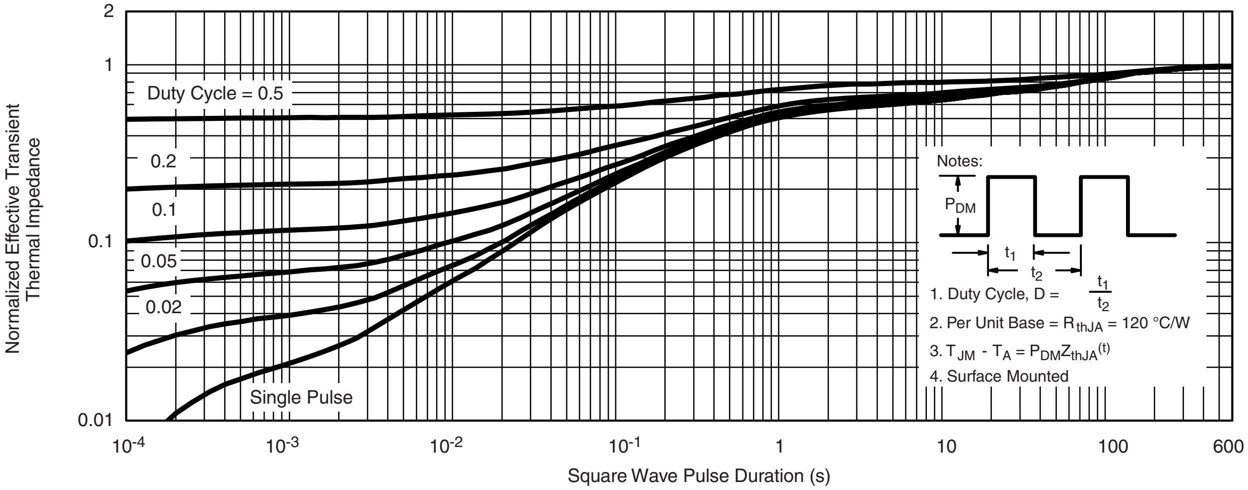
Single Pulse Power



* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Normalized Thermal Transient Impedance, Junction-to-Ambient

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Mounting LITTLE FOOT® SOT-23 Power MOSFETs

Wharton McDaniel

Surface-mounted LITTLE FOOT power MOSFETs use integrated circuit and small-signal packages which have been been modified to provide the heat transfer capabilities required by power devices. Leadframe materials and design, molding compounds, and die attach materials have been changed, while the footprint of the packages remains the same.

See part drawing below.

See Application Note 826, *Recommended Minimum Pad Patterns With Outline Drawing Access for Vishay Siliconix MOSFETs*, ~~(http://www.vishay.com/doc?72286)~~, for the basis of the pad design for a LITTLE FOOT SOT-23 power MOSFET footprint . In converting this footprint to the pad set for a power device, designers must make two connections: an electrical connection and a thermal connection, to draw heat away from the package.

The electrical connections for the SOT-23 are very simple. Pin 1 is the gate, pin 2 is the source, and pin 3 is the drain. As in the other LITTLE FOOT packages, the drain pin serves the additional function of providing the thermal connection from the package to the PC board. The total cross section of a copper trace connected to the drain may be adequate to carry the current required for the application, but it may be inadequate thermally. Also, heat spreads in a circular fashion from the heat source. In this case the drain pin is the heat source when looking at heat spread on the PC board.

Figure 1 shows the footprint with copper spreading for the SOT-23 package. This pattern shows the starting point for utilizing the board area available for the heat spreading copper. To create this pattern, a plane of copper overlies the drain pin and provides planar copper to draw heat from the drain lead and start the process of spreading the heat so it can be dissipated into the ambient air. This pattern uses all the available area underneath the body for this purpose.

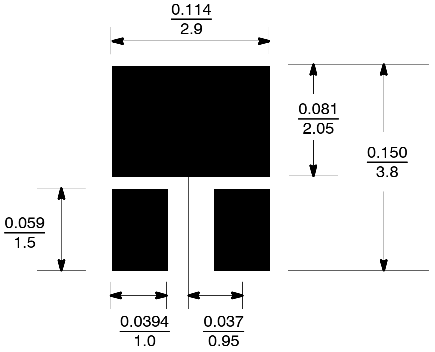
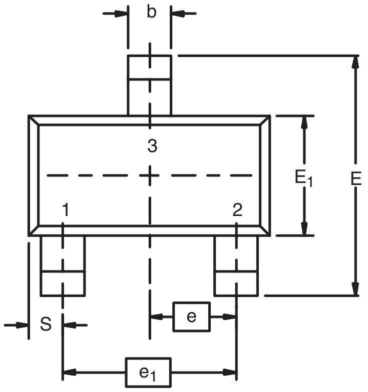


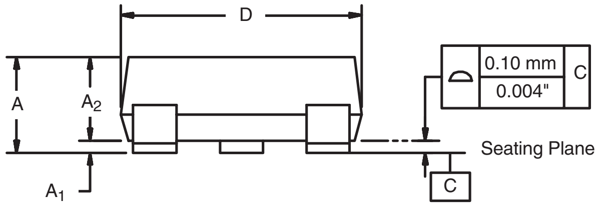
FIGURE 1. Footprint With Copper Spreading

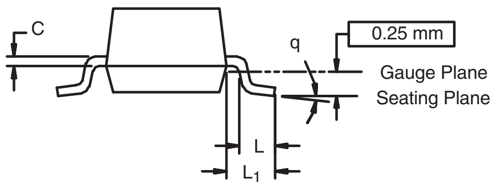
Since surface-mounted packages are small, and reflow soldering is the most common way in which these are affixed to the PC board, "thermal" connections from the planar copper to the pads have not been used. Even if additional planar copper area is used, there should be no problems in the soldering process. The actual solder connections are defined by the solder mask openings. By combining the basic footprint with the copper plane on the drain pins, the solder mask generation occurs automatically.

A final item to keep in mind is the width of the power traces. The absolute minimum power trace width must be determined by the amount of current it has to carry. For thermal reasons, this minimum width should be at least 0.020 inches. The use of wide traces connected to the drain plane provides a low-impedance path for heat to move away from the device.

SOT-23 (TO-236): 3-LEAD







Dim	MILLIMETERS		INCHES	
	Min	**Max**	**Min**	**Max**
A	0.89	1.12	0.035	0.044
A_1	0.01	0.10	0.0004	0.004
A_2	0.88	1.02	0.0346	0.040
b	0.35	0.50	0.014	0.020
c	0.085	0.18	0.003	0.007
D	2.80	3.04	0.110	0.120
E	2.10	2.64	0.083	0.104
E_1	1.20	1.40	0.047	0.055
e	0.95 BSC		0.0374 Ref	
e_1	1.90 BSC		0.0748 Ref	
L	0.40	0.60	0.016	0.024
L_1	0.64 Ref		0.025 Ref	
S	0.50 Ref		0.020 Ref	
q	3°	8°	3°	8°
ECN: S-03946-Rev. K, 09-Jul-01 DWG: 5479				